Supporting Information

Poly-4-vinylphenol (PVP) and poly(melamine-co-formaldehyde) (PMF)-based atomic switching device and its application to logic gate circuits with low operating voltage

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Accumulated *I–V* curves of PVP/PMF-based atomic switching devices with different PVP/PMF ratios

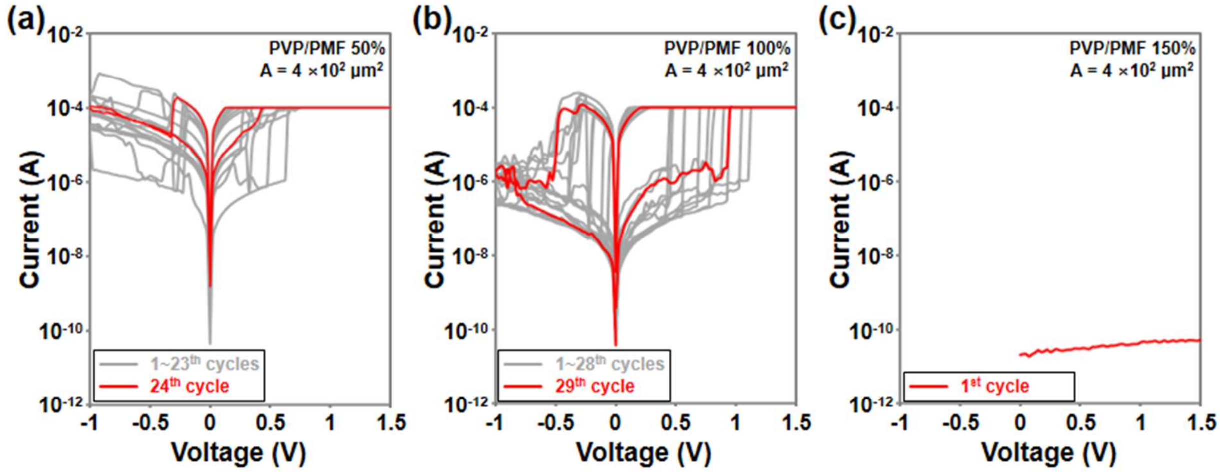

Figure S1. Current–voltage characteristics of PVP/PMF-based atomic switching devices with (a) 50%, (b) 100%, and (c) 150% PVP/PMF ratios. The cross-junction area of each PVP/PMF device is 4×10^2 μm^2.

Thicknesses of PVP/PMF electrolytes (50%, 100%, and 150%), as analyzed by AFM and SEM

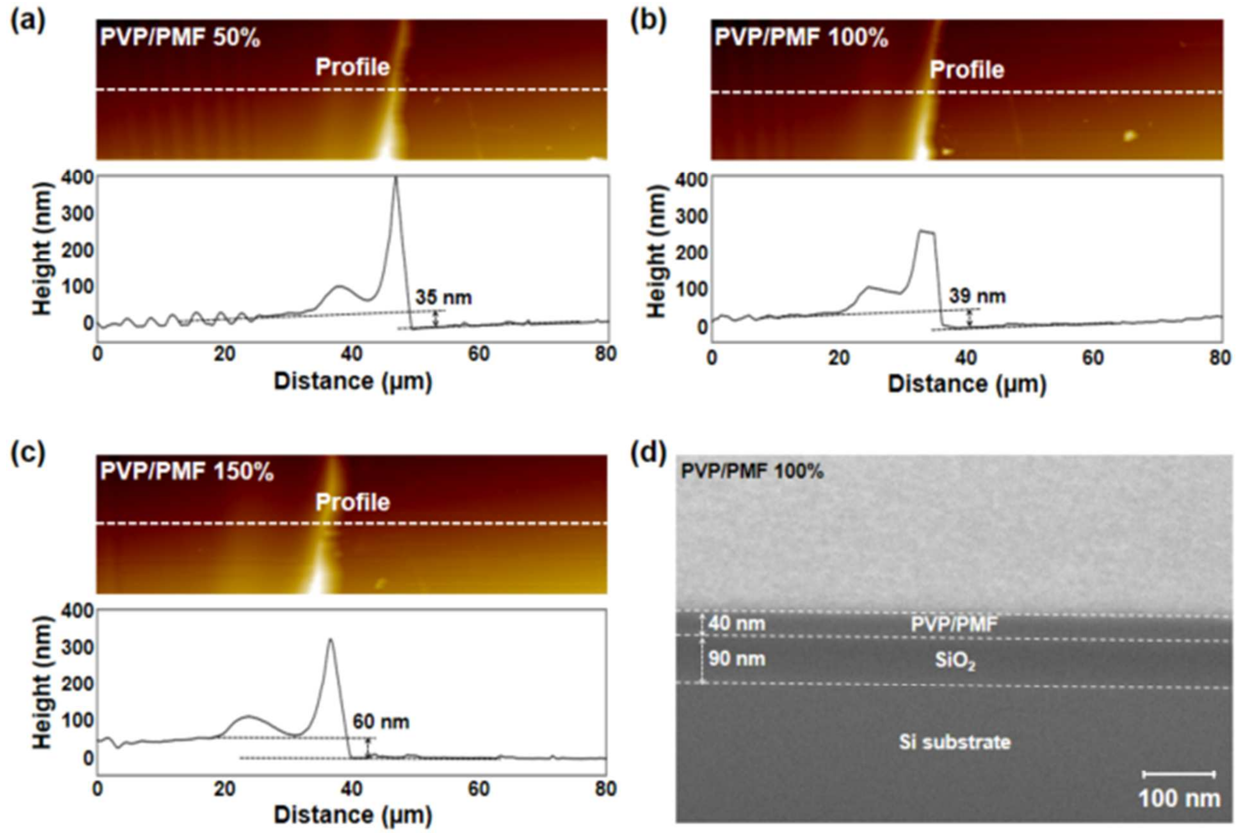

Figure S2. AFM analysis of PVP/PMF electrolytes with (a) 50%, (b) 100%, and (c) 150% PVP/PMF ratios. (d) SEM analysis of the 100% PVP/PMF electrolyte. The scale bar is 100 nm.

Figure S2 shows the thicknesses of PVP/PMF electrolytes with different PVP/PMF ratios. According to the AFM results, the thicknesses of 50%, 100%, and 150% PVP/PMF electrolytes were approximately 35, 39, and 60 nm, respectively. In addition, we confirmed the thickness of the 100% PVP/PMF electrolyte by SEM analysis. Once again, the thickness was approximately 40 nm.

Accumulated *I–V* curves of PVP/PMF-based atomic switching devices with/without a Ti buffer layer

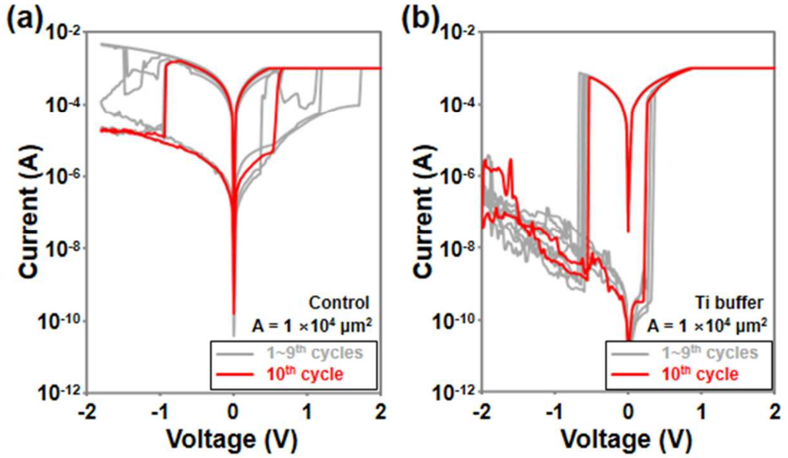

Figure S3. Current–voltage characteristics (1st–10th cycles) of PVP/PMF-based atomic switching devices (a) without and (b) with a Ti buffer layer. The cross-junction area of each PVP/PMF device is $1 \times 10^4\ \mu m^2$.

Applied pulse condition of AC pulse measurement

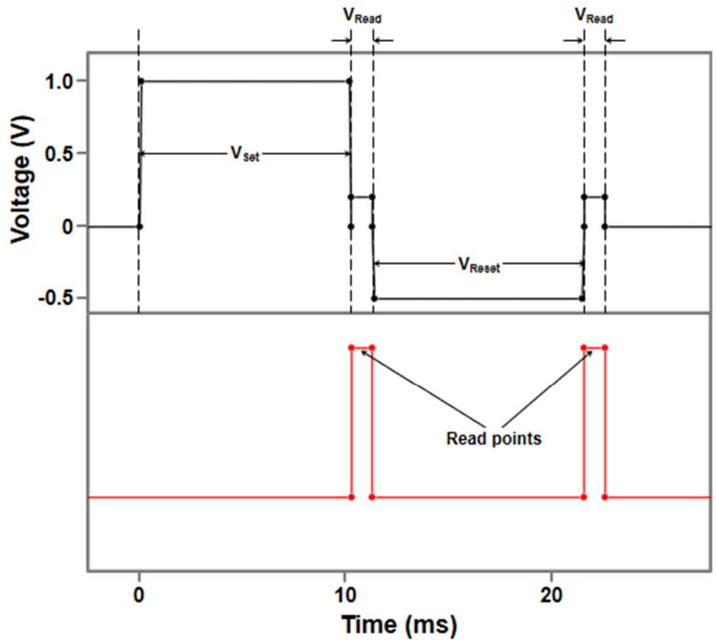

Figure S4. The applied pulse condition (black solid line) and read pulse condition (red solid line) of the AC pulse measurement used to determine the cyclic endurance characteristics of the PVP/PMF atomic switching devices.

Figure S4 shows the applied pulse condition of the AC pulse measurement for cyclic endurance determination. Here, the pulse width and rising/falling time are 10 ms and 10 μs, respectively (1.0 V of V_{Set} and –0.5 V of V_{Reset}). Moreover, the read voltages (0.2 V of V_{Read}) are set at 1 ms after applying the SET/RESET voltages.

Retention analysis of PVP/PMF-based atomic switching devices with/without a Ti buffer layer

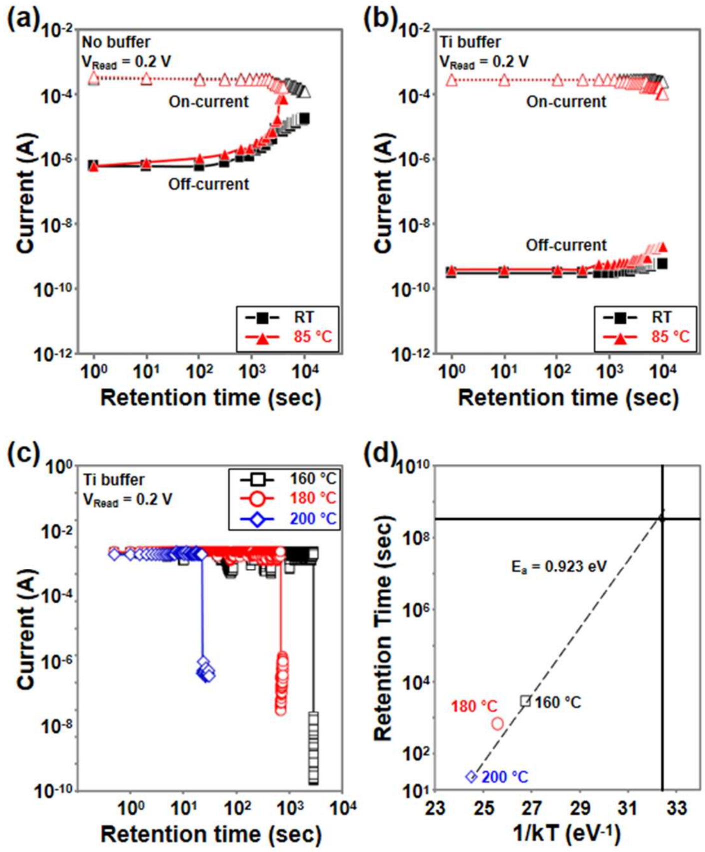

Figure S5. Retention analysis of PVP/PMF-based atomic switching devices with/without a Ti buffer layer. On-current (empty circle) and off-current (solid circle) distributions of (a) control and (b) Ti-buffer devices as a function of retention time at room temperature (RT, black circle) and 85 °C (red circle). (c) Retention failure time measurement of on-current at 160 (black), 180 (red), and 200 °C (blue) in the 100% PVP/PMF atomic switching device with a Ti buffer layer. Here, the read voltage (V_{Read}) is 0.2 V. (d) Extrapolation of the retention failure times measured at 160 (black), 180 (red), and 200 °C (blue).

As shown in Figures S5 (a) and (b), the retention failure time (the points at which LRS increases) of the Ti-buffer devices was 10^4 s at RT and 10^4 s at 85 °C, and that of the control device was 3×10^3 s at RT and 10^3 s at 85 °C. Thus, the Ti buffer layer can improve the retention time of PVP/PMF devices by donating additional electrons to the PVP/PMF electrolyte and thereby suppressing the oxidation (or decomposition) of the conduction filament. Figure S5 (c) shows the retention time of the on-current measured at different temperatures; the retention failure times were 2861 s, 686 s, and 23 s at 160 °C, 180 °C, and 200 °C, respectively. Therefore, we estimated an activation energy (E_a) of 0.923 eV using the Arrhenius plot shown in Figure S5 (d). In conclusion, our 100% PVP/PMF-based atomic switching device with a Ti buffer layer is expected to guarantee HRS/LRS data retention for approximately 10 years at 85 °C.

Current distribution and 3D CAFM images of 100% PVP/PMF electrolytes with/without a Ti buffer layer

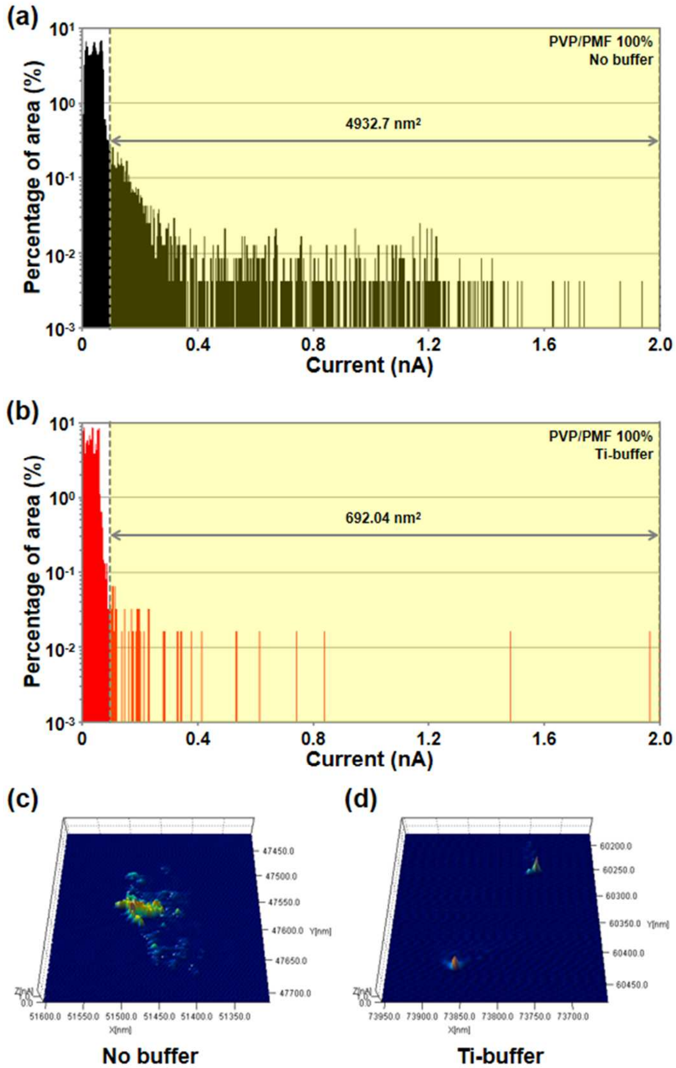

Figure S6. Current distributions in 100% PVP/PMF electrolytes (a) without and (b) with a Ti buffer layer. 3D CAFM images of 100 % PVP/PMF electrolytes (c) without and (d) with a Ti buffer layer (corresponding to Figure 3(f)). The size of the CAFM images is $0.4 \times 0.4\ \mu m^2$.

Figures S6 (a) and (b) show the current distributions in the 100% PVP/PMF electrolytes of control and Ti-buffer devices. According to the current distribution data, the conduction filament areas (> 0.1 nA) of control and Ti-buffer devices were 4932.7 nm^2 and 692.04 nm^2, respectively. Compared to the Ti-buffer device, the conduction filament area of the control device was larger by a factor of 7.1.

Forming voltage variation by PVP/PMF composition ratio and Ti buffer layer insertion

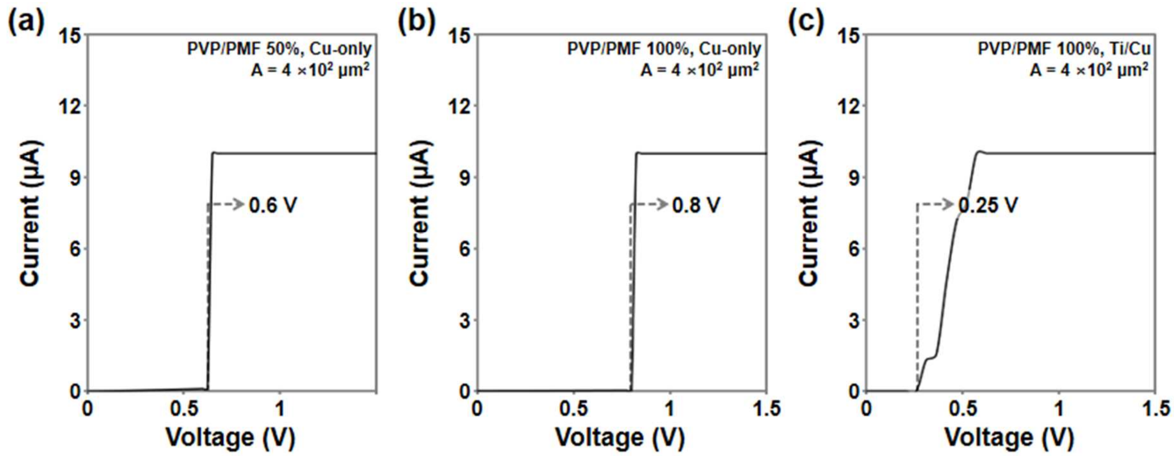

Figure S7. 1st-cycle I–V curves of (a) 50% and (b) 100% PVP/PMF devices using Cu-only electrodes, and (c) Ti-inserted 100% PVP/PMF devices

To investigate the influence of the PVP/PMF composition and Ti buffer layer on the forming voltage of the PVP/PMF atomic switching device, we compared the 1st-cycle I-V curves of 50%/100% PVP/PMF devices using Cu-only electrodes and a Ti-inserted 100% PVP/PMF device. As shown in Supporting Information Figure S7, the forming voltage of the 100% PVP/PMF device was slightly higher than that of the 50% device (50%: 0.6 V and 100%: 0.8 V). This is because increasing the number of cross-linked chains (PVP/PMF ratio ↑) reduced the number of sites for Cu ion diffusion, thereby raising the activation energy for the formation of conduction filament. In addition, the forming voltage could be reduced by inserting a Ti buffer layer. Compared to the 100% PVP/PMF device using Cu-only electrodes, the Ti-inserted 100% PVP/PMF device had the forming voltage reduced by a factor of approximately 3 (Cu-only: 0.8 V and Ti-inserted: 0.25 V), because the Ti buffer layer provided additional electrons and reduced the activation energy for the formation of conduction filaments.

Operation of PVP/PMF device-based AND/OR gate circuits

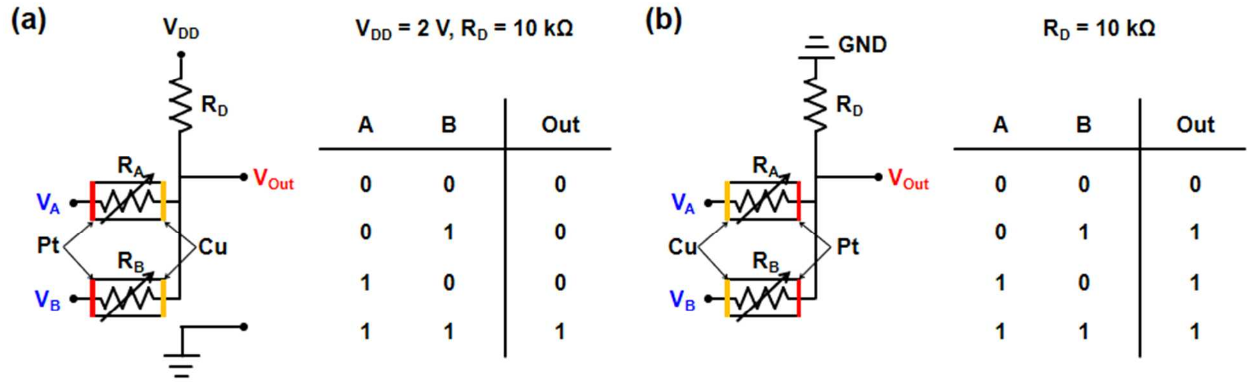

Figure S8. Schematic diagrams and truth tables of (a) AND and (b) OR gates. Here, V_A and V_B are applied as input bias voltages, and the constant voltage (V_{DD}) and resistor (R_D) were 2 V and 10 kΩ, respectively.

Figure S7 (a) shows the AND gate circuit based on two PVP/PMF-based atomic switching devices. Here, input voltages (V_A and V_B) and constant voltage (V_{DD}) were applied to the Pt and Cu electrodes of the atomic switches, respectively.

(i) input state 00 (initial state)

Because V_{DD} was applied to the Cu electrodes of two atomic switching devices, the resistances of both devices (R_A and R_B) have the LRS value (1 kΩ). As a result, most of V_{DD} was dropped in constant resistance (R_D), presenting 0 V of V_{out}.

(ii) input state 00 → 01

By applying 5 V to the Pt side of device B (input state 01), the B device was turned off, thus giving R_B the HRS value (10^5 kΩ). However, because the parallel resistance of R_A and R_B (1 kΩ) was still lower than R_D (10 kΩ), V_{out} was still 0 V.

(iii) input state 01 → 10

When the input state changed from 01 to 10, the resistance states of devices A and B remained LRS and HRS, respectively, thus increasing V_{out} instantaneously from 0 to 5 V (calculated by Kirchhoff's law). Because there is no potential difference (or very small potential difference) between the electrodes of device A, the resistance state of device A is not changed (R_A has LRS value). In contrast, this V_{out} is newly applied to the Cu side of device B, thus turning on device B (R_B now has LRS value).

$$\frac{2-V_{Out}}{10}+\frac{5-V_{Out}}{1}=\frac{V_{out}-0}{10^5}\,, \qquad V_{out}\approx\ 5\,V$$

In sequence, as device B is turned on, V_{out} decreases from 5 V to 2.5 V.

$$\frac{2-V_{Out}}{10}+\frac{5-V_{Out}}{1}=\frac{V_{out}-0}{1}\,, \qquad V_{out}\approx\ 2.5\,V$$

This indicates that the voltage applied to the Cu side of device A is stabilized from 5 V to 2.5 V, consequently turning off device A (R_A has HRS value). Now, because the voltages applied to the

Cu and Pt sides of device B are 2.5 V and 0 V, respectively, device B is still under on-state (R_B has LRS value). Therefore, V_{out} converges to 0 V.

$$\frac{2 - V_{out}}{10} + \frac{5 - V_{out}}{10^5} = \frac{V_{out} - 0}{1}, \qquad V_{out} \approx 0\,V$$

(iv) input state 10 → 11

By applying 5 V to the Pt side of device B (input state 11), device B is turned off (R_B has HRS value), thus increasing V_{out} from 0 V to 2 V.

$$\frac{5 - V_{out}}{10^5} + \frac{5 - V_{out}}{10^5} = \frac{V_{out} - 2}{10}, \qquad V_{out} \approx 2\,V$$

Figure S7 (b) shows the OR gate circuit based on two PVP/PMF-based atomic switching devices. In this case, the input voltages (V_A and V_B) and constant voltage (V_{DD}) were applied to the Cu and Pt electrodes of the atomic switches, respectively.

(i) input state 00 (initial state)

V_{out} is 0 V because all external voltages (V_A, V_B, and ground) are 0 V.

(ii) input state 00 → 01

By applying 2 V of V_B to the Cu side of device B (input state 01), the resistance state of device B is changed from HRS to LRS (R_B = 1 kΩ). Because the total resistance of R_A and R_D in parallel (10 kΩ) is higher than R_B, most of V_B is dropped in the resistance of $R_A \parallel R_D$. Therefore, V_{out} increases from 0 V to 2 V.

(iii) input state 01 → 10

When the input state changes from 01 to 10, R_A and R_B still have HRS and LRS values, respectively, thus decreasing V_{out} instantaneously from 2 V to 0 V. As a result, device A is turned on while 0 V is applied to the Pt side of device A (R_A has LRS). Because there is no potential difference (or small potential difference) between the Cu and Pt electrodes of device B, R_B still has its LRS value.

$$\frac{2 - V_{out}}{10^5} = \frac{V_{out} - 0}{1} + \frac{V_{out} - 0}{10}, \qquad V_{out} \approx 0\,V$$

In sequence, as device A is turned on, V_{out} increases from 0 V to 1 V.

$$\frac{2 - V_{out}}{1} = \frac{V_{out} - 0}{1} + \frac{V_{out} - 0}{10}, \qquad V_{out} \approx 1\,V$$

This result indicates that the voltage applied to the Pt side of device B is increased from 0 V to 1 V, thus turning off device B (R_B has HRS value). Meanwhile, device A is still under on-state (R_A has LRS value) because the voltages at the Cu and Pt sides of device A are 2 V and 1 V, respectively. As a result, most of V_A is dropped in the parallel resistance of $R_B \parallel R_D$ because $R_B \parallel R_D$ (10 kΩ) is higher than R_A (1 kΩ). Therefore, final V_{out} becomes 2 V.

(iv) input state 10 → 11

When 2 V is applied to the Cu side of device B (input state 11), device B can be turned on (R_B has LRS value) or maintained (R_B has HRS value), where V_{out} is still 2 V.

$$\frac{2-V_{out}}{1}+\frac{2-V_{out}}{1}=\frac{V_{out}-0}{10}, \qquad V_{out}\approx\ 2\,V$$

Here, we assume that the operating speed of the two atomic switching devices is slower than the change in the input state.