Supporting Information

Largely Improved Near-Infrared Silicon-Photosensing by the Piezo-Phototronic Effect

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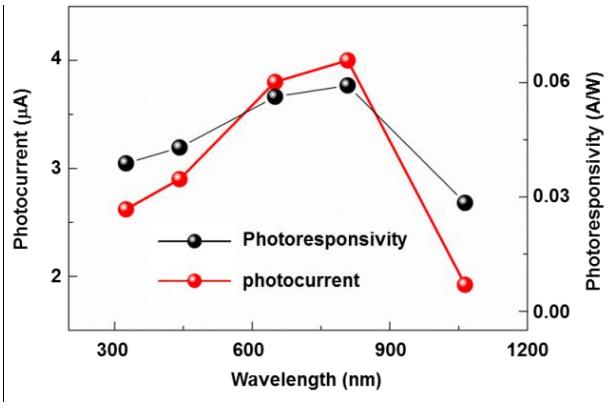

Figure S1. Photoresponsivity and photocurrent of p-Si/n-CdS NWs heterostructure PD under different incident wavelengths of 325, 442, 650, 808 and 1064 nm.

A. Performance enhancement in p-Si/n-CdS NWs heterostructure NIR PD induced by the external compressive strain.

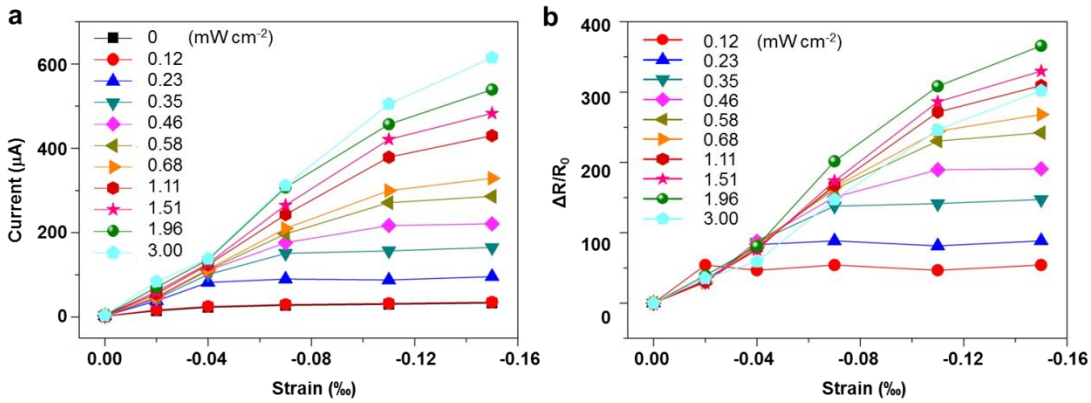

Figure S2. (a) Output currents and (b) relative changes of photoresponsivity in p-Si/n-CdS NWs heterostructure NIR PD under different strains and illumination conditions when the forward bias is 2 V.

B. Fabrication and the piezo-phototronic effect in p-Si/n-ZnO NWs heterostructure NIR PD with the pn junction formed by p-Si and −*c* end of n-ZnO.

First, the p-type (100) silicon wafer (B doped, 1−10 Ω cm, University Wafer) was etched by 5 wt. % KOH with 5 vol % isopropanol at 85 ^{o}C for 40 min. After then, the etched Si wafer with micropyramids was ultrasonically cleaned in acetone, distilled water, and isopropanol for 2 min, respectively. Next, the

etched Si wafer deposited 100 nm ZnO seed layer was placed into a mixed solution containing 35 mM zinc acetate (Alfa Aesar) and 35 mM hexamethylenetetramine (HMTA) (Alfa Aesar) to obtain ZnO NWs at 95 ^{o}C for 2 h in an oven. The obtained sample was cleaned with deionized water and dried at 60 °C. Hereafter, a top electrode (ITO) and bottom electrode (Al) were deposited by RF magnetron sputtering at room temperature (PVD75 system, system, Kurt. J. Lesker Company), respectively. Finally, a layer of polydimethylsiloxane (PDMS) was spin-coated onto the top electrode to package the device.

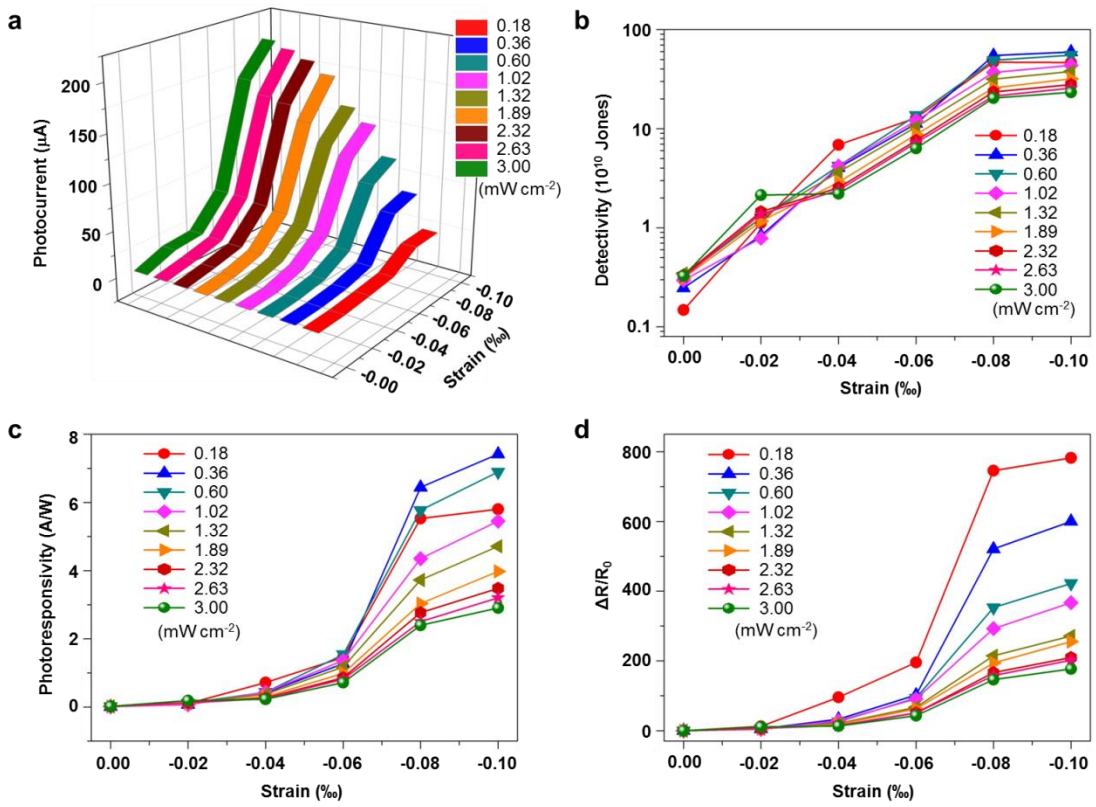

Figure S3. The piezo-phototronic effect on p-Si/n-ZnO NWs heterostructure NIR PDs. (a) Photocurrent, (b) detectivity, (c) photoresponsivity, and (d) $\Delta R/R_0$ of the NIR PD device under different strains and illumination conditions when the forward bias is 0.5 V.

C. Fabrication and the piezo-phototronic effect in p-Si/n-ZnO NWs heterostructure PD with the pn junction formed by p-Si and +*c* end of n-ZnO.

A layer of 100 nm ITO electrode followed by another 100 nm ZnO seed layer were deposited on a piece of glass substrate by RF magnetron sputtering at room temperature, and then the coated glass was placed into a mixed nutrient solutions (35 mM zinc acetate and 35 mM HMTA) for ZnO NWs growth

via a hydrothermal method in an oven at 95 ^{o}C for 2 h. A smooth p-type (100) silicon wafer was placed and covered on the top of ZnO NWs obtained from the last step to form pn junction between p-Si and +*c* end of the ZnO NWs. Finally, a layer of Al electrode was deposited on the back of the p-Si wafer by RF magnetron sputtering.

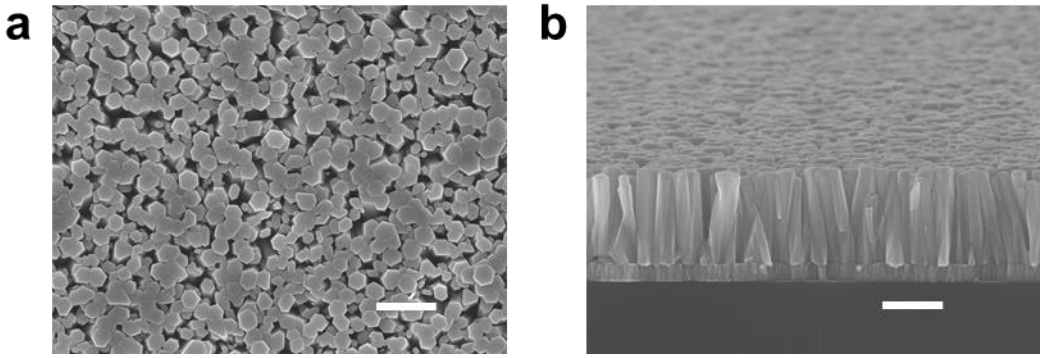

Figure S4. (a) Top and (b) side view SEM images of the ZnO NWs hydrothermally grown on ITO/glass substrate. The scale bars are 1 μm.

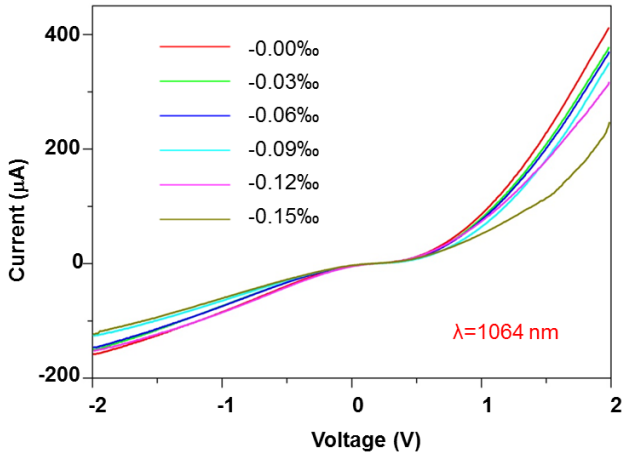

Figure S5. *I-V* characteristics of a p-Si/n-ZnO NWs heterostructure device under different compressive strains under 1064 nm illumination with a power density of 3 mW cm^{-2} when a 2 V bias is applied.

D. Fabrication of p-Si/n-TiO_2 NWs heterostructure device and transmission spectrum of TiO_2 NWs.

First, the p-type (100) silicon wafer (B doped, 1~10 Ωcm, University Wafer) was etched by 5 wt. % KOH with 5 vol % isopropanol at 85 ^{o}C for 40 min. After then, the etched Si wafer with micro-pyramids was ultrasonically cleaned in acetone, distilled water, and isopropanol for 2 min,

respectively. Then, 10 mL of ethanol, 740 μL of titanium butoxide, 10 μL of HCl (37 wt%), and 10 μL of deionized water and were mixed as a precursor solution.[1] The precursor solution was spin-coated at 1500 rpm onto the etched p-Si wafer substrate before annealed at 450 °C to form a layer of TiO_2 seed. Then, 30 mL of deionized water was mixed with 30 mL of HCl (37 wt %), and the mixture was stirred at room temperature for 5 min before the addition of 1 mL of titanium butoxide (97% Aldrich).[2] After stirring for another 5 min, the etched p-Si wafer was placed into this mixture with the growth surface facing down. The hydrothermal process was conducted at 200 ^{o}C for 8 h in an oven. The obtained sample (Figure S6) was cleaned with deionized water and dried at 60 °C. After that, a top electrode (ITO) and bottom electrode (Al) were deposited by RF magnetron sputtering at room temperature, respectively. Finally, a layer of polydimethylsiloxane (PDMS) was spin-coated onto the top electrode to package the device.

The transmittance characteristic of TiO_2 NWs array was obtained by measuring the transmittance spectrum of TiO_2 NW array grown on the glass substrate with the same method as that grown on p-Si wafer, shown in Figure S7.

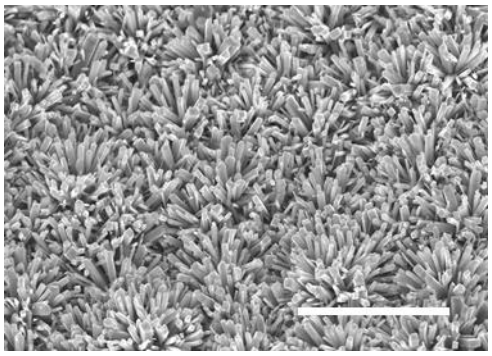

Figure S6. Typical SEM image of the as-grown n-TiO_2 NW array on textured Si substrate. The scale bar is 10 μm.

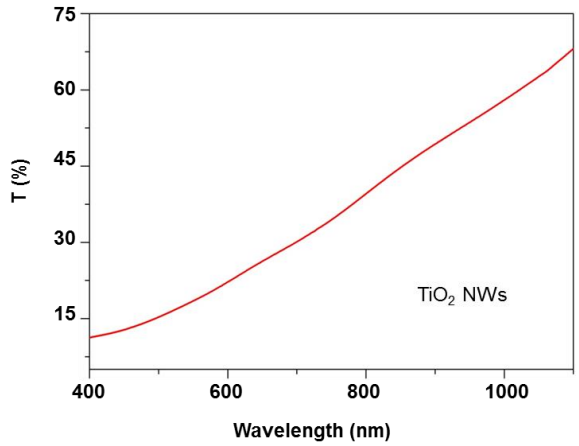

Figure S7. Transmission spectrum of TiO_2 NW array grown on the FTO/glass substrate.

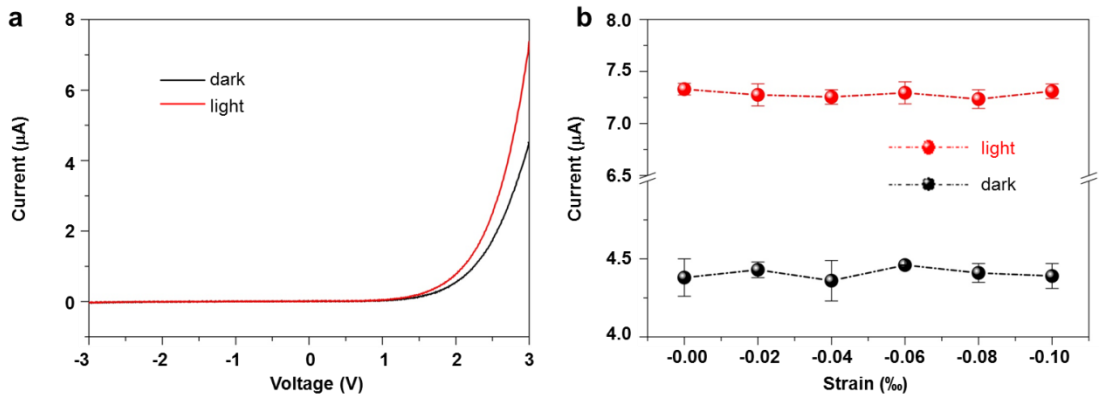

Figure S8. (a) *I-V* characteristics of the p-Si/n-TiO_2 NWs heterostructure device with and without 1064 nm illumination (3.00 mW cm^{-2}) when a 3 V bias is applied. (b) Light and dark currents change with the increase of compressive strains when the forward biased is 3 V.

E. Calculation of strains applied on CdS NWs and piezo-potential distribution in p-Si/n-CdS heterostructure.

Commercial finite element analysis (FEA) software COMSOL Multiphysics is utilized to conduct the theoretical simulation and calculate the applied strain and corresponding piezo-potential distribution in n-type CdS NWs under different compressive strains. An external compressive strain is applied onto the p-Si/n-CdS PD by uniformly pressing the surface of the device with a piece of transparent sapphire through a three dimensional (3D) stage (moving resolution ~10 μm). A schematic structure of the 3D model of the p-Si/n-CdS NIR PD is shown in Figure 1a in the main text. Considering that if we use the actual dimensions of the p-Si/n-CdS NWs NIR PD device as model, the stimulation and calculation would be very complicated. Therefore, the simplified 2D and 3D model of the device are built, respectively, as shown in Figures S9 and S10. The simulation dimensions are as follows: the bottom edge length and the height of the pyramids are 5 and 3.5 μm (Figure 1b), respectively. The diameter and length of CdS NWs, on average, are 50 and 600 nm, respectively. The thickness of PDMS layer is about 1.3 μm. Because the sapphire and silicon substrate are much stiffer than PDMS and their strains are negligible, and thus are ignored in this calculation. The PDMS and ITO layers are hided in all results.

The elastic coefficient, piezoelectric coefficient, and relative permittivity matrices of CdS material and all the other materials' parameters used in the simulation are concluded below in Tables S1 and S2, respectively. The bottom surface of the p-Si substrate is fixed, which means it has no displacements in

any directions at all. A downward displacement along the *z*-axis direction in the coordinate as a boundary condition is applied to the upper surface of the top sapphire substrate to describe the externally applied compressive forces in the experiments. An electric ground boundary condition is applied at infinite boundaries to serve as the reference for the calculation of the piezo-potential distribution. Finally, the piezoelectric constitutive equations are solved using the Solid Mechanics, Electrostatics and Piezoelectric Effect modules in COMSOL. After the computation, the average strains and piezo-potential distribution of the n-type CdS NWs under different compressive displacements could be derived and obtained by post-processing. The piezo-potential distributions for 2D and 3D models are shown in Figures S9 and S10.

Table S1. Physical parameters of CdS used in the stimulation.

<table>
<tr><th></th><th colspan="2">Elastic coefficient</th><th colspan="2">Piezoelectric coefficient</th><th colspan="2">Relative permittivity</th></tr>
<tr><td rowspan="6">CdS</td><td>c_{11}</td><td>90.68[GPa]</td><td rowspan="2">e_{31}</td><td rowspan="2">-0.219[C/m^2]</td><td rowspan="3">ε_{r11}</td><td rowspan="3">9.02</td></tr>
<tr><td>c_{12}</td><td>58.09[GPa]</td></tr>
<tr><td>c_{13}</td><td>50.94[GPa]</td><td rowspan="2">e_{33}</td><td rowspan="2">0.457[C/m^2]</td></tr>
<tr><td>c_{33}</td><td>93.81[GPa]</td><td rowspan="3">ε_{r33}</td><td rowspan="3">9.52</td></tr>
<tr><td>c_{44}</td><td>15.04[GPa]</td><td rowspan="2">e_{15}</td><td rowspan="2">-0.2105[C/m^2]</td></tr>
<tr><td>c_{66}</td><td>(c_{11}-c_{12})/2</td></tr>
</table>

Table S2. Physical parameters of sapphire, ITO, PDMS, and Si used in the stimulation.

Material	ε_r	Density	Young's modulus	Poisson's ratio
Sapphire	11.5	3.98[g/cm^3]	435[GPa]	0.29
ITO		6.8[g/cm^3]	116[GPa]	0.35
PDMS	2.75	0.97[g/cm^3]	923[psi]	0.49
Si	11.9	2.33[g/cm^3]	170[GPa]	0.28

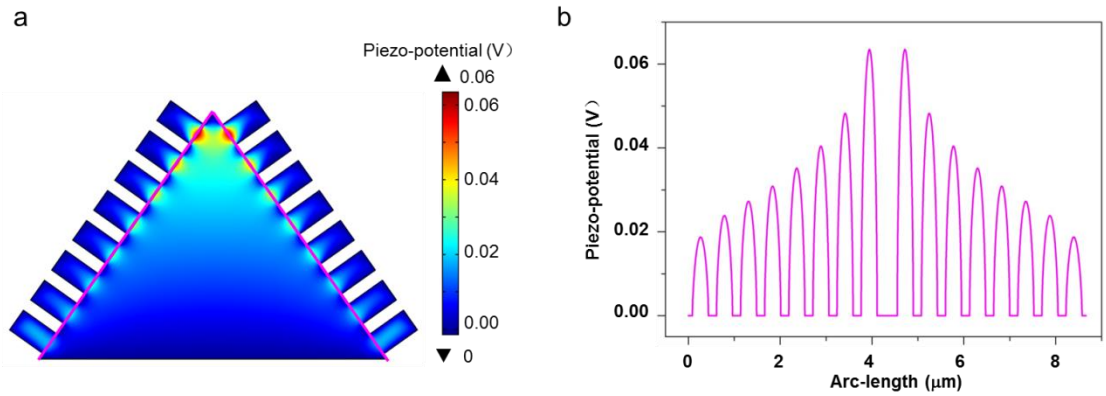

Figure S9. (a) Piezo-potential distribution of a simplified 2D model device under -0.15‰ compressive strain. (b) Piezo-potential distribution of a simplified 2D model device along arc-length (purple line) under -0.15‰ compressive strain.

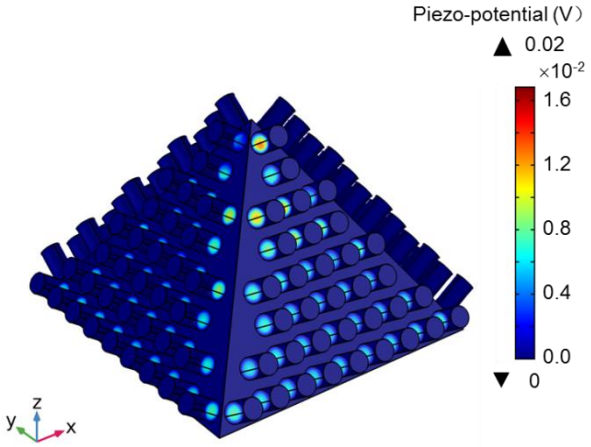

Figure S10. Piezo-potential distribution of a simplified 3D model device under -0.15‰ compressive strain.

F. Discussion of the force applied to the CdS NWs and its effect on the piezoelectric potential located at the p-Si/n-CdS interface.

In our p-Si/n-CdS heterojunction device, the silicon substrate's surface is first chemically modified as pyramids and then the CdS NWs are hydrothermally grown on the silicon's (111) plane. As a result, while applying a vertical compressive force on the device, the CdS NWs experience shearing force because the applied force is not parallel to the CdS NWs' growth axis, *i.e.* the *c*-axis. The deformation of the NWs under vertical compressive force in the simulation results are shown in Figure S11 clearly illustrate this point, and also indicate the piezoelectric potential (piezo-potential) located at the p-Si/n-CdS interface is positive.

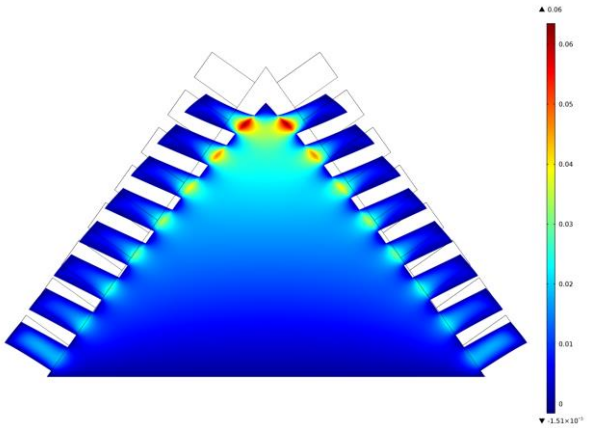

Figure S11. Two-dimensional electric potential distribution of the p-Si/n-CdS heterojunction device under vertical compressive force. The black lines are the frame of the p-Si/n-CdS heterojunction device without any forces. The deformations of the silicon pyramid and the CdS NWs have been scaled up to clearly illustrate the applied force induced deformations.

As the spin-coated PDMS is isotropic and very soft, whereas the deposited ITO electrode is very hard (with Young's modulus of 116 GPa) compared with the CdS NWs, the force that the CdS NWs experience can be approximately considered as along the vertical direction, the same as the applied force, as illustrated in Figure S12. Obviously, the vertical force applied to the CdS NWs can be split into two forces, with one along the *a*-axis of the CdS NWs and the other along the *c*-axis of the CdS NWs, respectively. Figure S13a shows the piezo-potential distribution of a CdS NW under applied force along its *a*-axis, indicating that the piezo-potential varies along the *a*-axis, not the *c*-axis. The profile of the piezo-potential at the bottom of the CdS NW is plotted in Figure S13b, showing that the pure piezo-potential of the whole bottom surface of the CdS NW is nearly zero and therefore negligible. However, as shown in Figure S14a, while the CdS NW experience a force along its *c*-axis, the piezo-potential distributes along the CdS NW's *c*-axis, not the *a*-axis. Furthermore, the profile of the piezo-potential at the bottom of the CdS NW plotted in Figure S14b indicates that, under this circumstance, the pure piezo-potential of the whole bottom surface of the CdS NW is positive. Therefore, considering the simulation results summarized in Figures S13 and S14 and the discussion about the applied vertical compressive force above, it is easily to conclude that, the split force along *a*-axis of CdS NW hardly contribute to the piezo-potential of the bottom surface of CdS NW, whereas the other split force along *c*-axis of CdS NW dominantly contributes to the piezo-potential of the bottom surface of CdS NW.

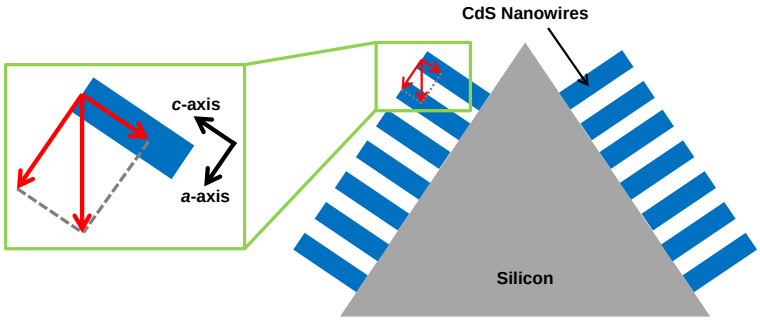

Figure S12. Distribution of the applied vertical force to the CdS NWs.

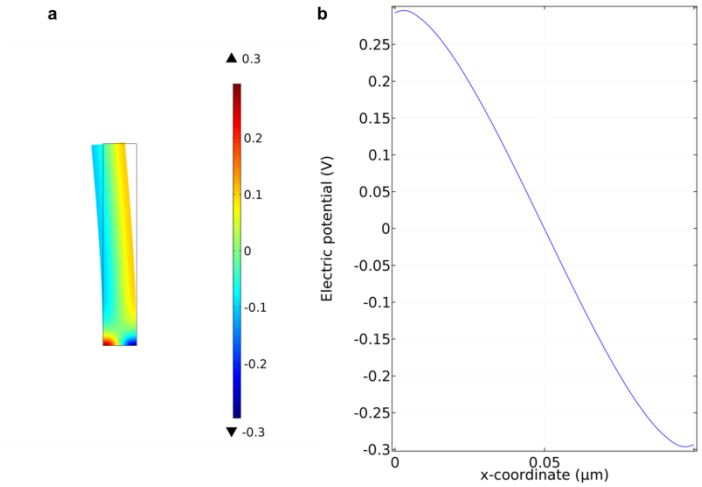

Figure S13. (a) Two-dimensional electric potential distribution of a CdS NW under applied force along its *a*-axis. (b) Electric potential profile along the *x*-coordinate at the bottom of the CdS NW.

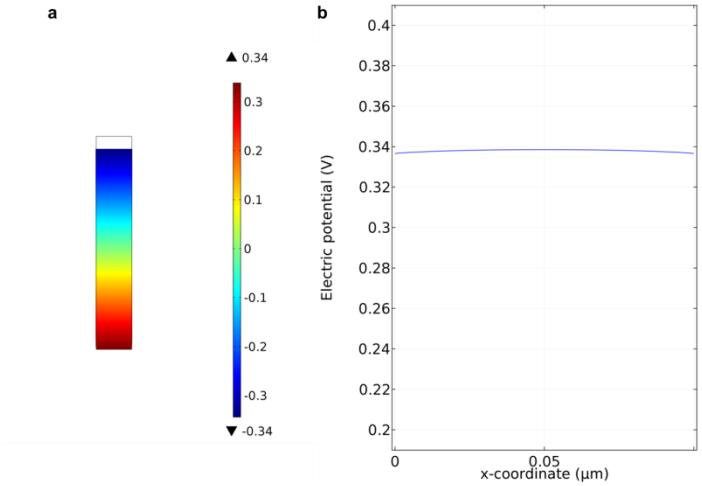

Figure S14. (a) Two-dimensional electric potential distribution of a CdS NW under applied force along its *c*-axis. (b) Electric potential profile along the *x*-coordinate at the bottom of the CdS NW.

G. Calculation of the external-strain-induced influence on the energy band diagrams for p-Si/n-CdS heterojunction.

COMSOL Multiphysics is also utilized to conduct the theoretical simulation and derive the energy band diagrams of p-Si/n-CdS heterojunction under different compressive strains. For simplification, a one-dimensional (1D) model is used here to investigate the effect of applied compressive strains on the energy band diagram of the p-Si/n-CdS heterojunction. The semiconductor parameters of Si and CdS used in the simulation are listed in Table S3. The "Analytic Doping Model" built inside the Semiconductor module of COMSOL is applied to describe the uniform doping and depletion regions of p-type Si and n-type CdS. The doping concentrations of p-Si and n-CdS are 1×10^{16} cm^{-3} and 1×10^{15} cm^{-3}, respectively, and the depletion widths are calculated through the abrupt junction approximation.[3] Two Ohmic contacts are then applied to the ends of p-Si and n-CdS to describe the externally applied bias voltage. Next, a surface charge density boundary condition is applied to the interface of p-Si/n-CdS heterojunction to introduce the piezo-charge density for the investigation of effects of the applied compressive strains. Finally, the conventional drift-diffusion approach is solved and computed using partial differential equations available internally within the Semiconductor module in COMSOL. After the computation, the energy band diagrams of p-Si/n-CdS heterojunction under different compressive strains and bias voltages could be derived and obtained by post-processing.

Table S3 Physical parameters of n-CdS and p-Si used in the stimulation.

Material	ε_r	Band gap	Electron affinity
Si	11.9	1.12[eV]	4.05[eV]
CdS	8.9	2.42[eV]	4.40[eV]

References

(1) Li, X.; Dai, S.-M.; Zhu, P.; Deng, L.-L.; Xie, S.-Y.; Cui, Q.; Chen H.; Wang, N.; Lin, H. Efficient Perovskite Solar Cells Depending on TiO_2 Nanorod Arrays. *ACS Appl. Mater. Interfaces* **2016**, *8*, 21358–21365.

(2) Wang, C.; Jiang, Z.; Wei, L.; Chen, Y.; Jiao, J.; Eastman, M.; Liu, H. Photosensitization of TiO_2 Nanorods with CdS Quantum Dots for Photovoltaic Applications: a Wet-Chemical Approach. *Nano Energy* **2012**, *1*, 440-447.

(3) Sze, S. M. Physics of Semiconductor-Devices. *CC/Eng. Tech. Appl. Sci.* **1982**, *27*, 28.