# Supporting Information

Manuscript title:

**Solution-based Fabrication of Poly-crystalline Si Thin Film Transistors from Recycled Polysilanes**

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Number of SI pages: 3

Number of SI figures: 4

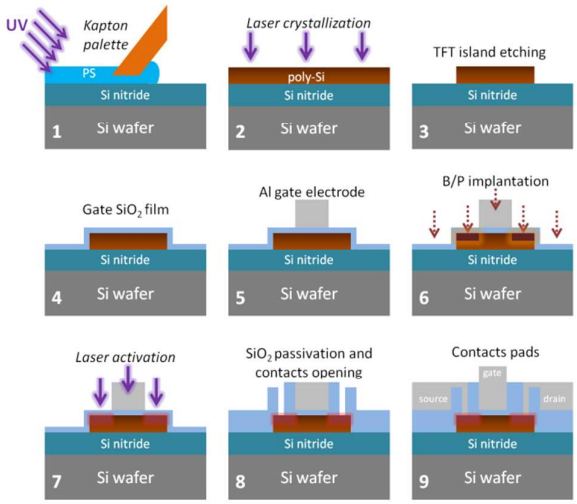


Figure SI 1. TFT fabrication steps. 1) PS spreading by soft palette on substrate under UV irradiation; 2) RT excimer laser crystallization; 3) poly-Si island photolithographic definition and dry etching; 4) 60 nm $SiO_2$ PE-CVD deposition for gate dielectric; 5) 900 nm Al gate electrode deposition and dry etching; 6) boron (for p-channel) and phosphorus (for n-channel) ion

implantation; 7) RT excimer laser dopants electrical activation; 8) 800 nm $SiO_2$ PE-CVD deposition and contacts opening by oxide dry and wet etching; 9) Al deposition for contact pads.

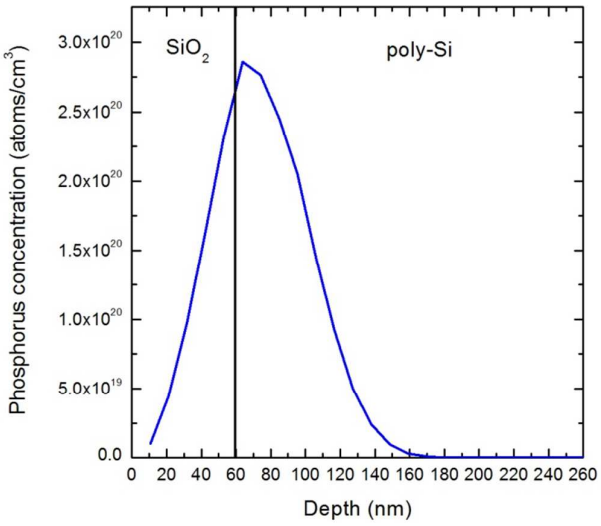


Figure SI 2. Phosphorus ions concentration profile calculated by SRIM-2008 (P ions energy = 50 keV, dose = $2 \cdot 10^{15}$ atoms/cm$^2$, incidence angle = 7°, $SiO_2$ density = 2.33 cm$^{-3}$, poly-Si density = 2.32 cm$^{-3}$.

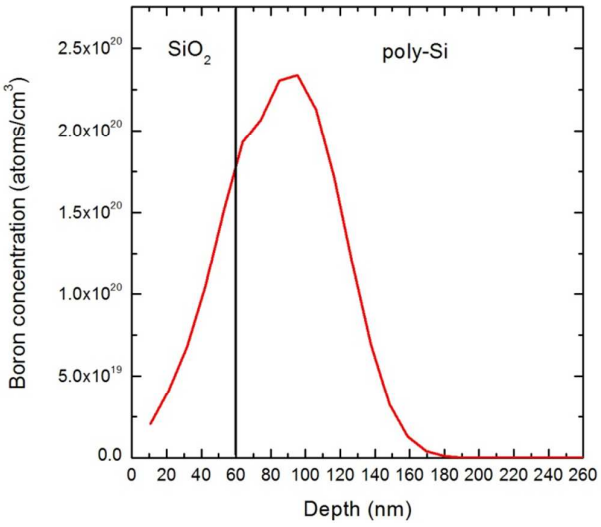

Figure SI 3. Boron ions concentration profile calculated by SRIM-2008 (B ions energy = 20 keV, dose = $2 \cdot 10^{15}$ atoms/cm$^2$, incidence angle = 7°, $SiO_2$ density = 2.33 cm$^{-3}$, poly-Si density = 2.32 cm$^{-3}$.

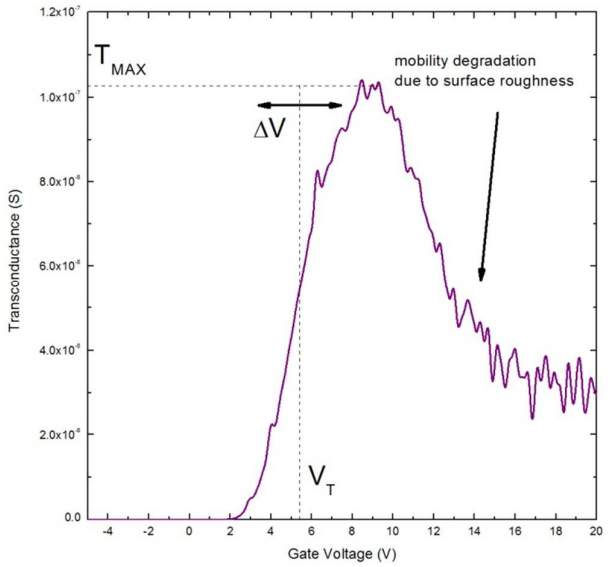


Figure SI 4. Transconductance T as a function of gate voltage $V_g$ for n-channel TFT with W/L=2.

According to Sameshima et al.[13], the threshold voltage $V_T$ is defined as $V_g$ at $T = T_{MAX}$. $\Delta V$ is defined as $T_{MAX} (\partial T/\partial V_g|_{V_g=V_T})^{-1}$. Moreover, the areal density of defects states N, which are occupied when $V_g = V_T$, is equal to $C/e \cdot (V_T - \Delta V/8)$, where C and e are respectively the gate oxide capacitance per unit area and the elementary charge.

In this work, the lower bound of the density of defects states have been assumed equal to N, while their position within the band-gap have been guessed from the simulations of Sameshima et al.[13]