Supporting Information

Control of Multilevel Resistance in Vanadium Dioxide by Electric Field using Hybrid Dielectrics

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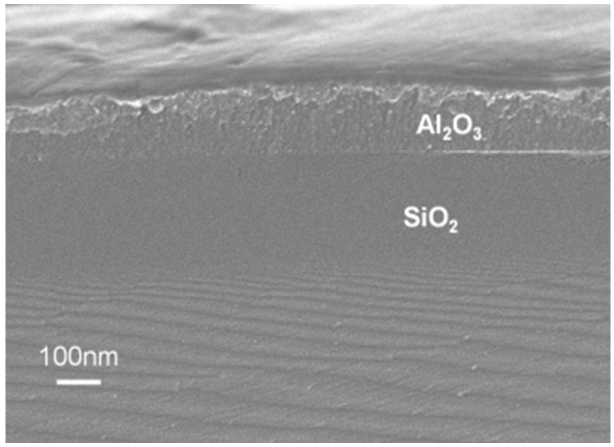

Figure S1, Cross-sectional SEM image of SiO_2 and Al_2O_3 hybrid dielectric layer. SEM image shows that Al_2O_3 of 200 nm thickness was deposited on SiO_2 layer of 300 nm. Then VO_2 film was doposited and FET-VO_2 device was fabricated on hybrid dielectric of 500 nm thickness. Cross-sectional image shows a good interface quality between the two dielectric layers.

Table S1; Summary of VO2 devices fabricated of different dielectric layer thickness.

No	Device structure	VO2 thickness ~(nm)	Dielectric layer	Dielectric thickness ~(nm)	leakage
1	$VO_2/SiO_2/Si^+$	100	SiO_2	100	High
2	$VO_2/SiO_2/Si^+$	100	SiO_2	200	High
3	$VO_2/SiO_2/Si^+$	100	SiO_2	300	small
4	$VO_2/Al_2O_3/SiO_2/S^+$	100	Al_2O_3/SiO_2	200/300	Very small

It should be noted that the thickness of the VO_2 film was kept constant (~100nm) for all devices. Instead, we vary the thickness of the dielectric layer as shown in the Table S1. The main purpose of varying the thickness of the dielectric layer was to choose the optimized layer thickness in order to minimize the leakage current while observing a clear gate effect on VO_2 devices as evident in Figure 5b. We found that both 100 nm and 200 nm thick SiO_2 dielectric layers showed a very high leakage current. Further, we showed that the SiO_2 layer of 300 nm thickness and Al_2O_3/SiO_2 hybrid dielectric layer of 200/300 nm thickness were thick enough to show pronounced gate effects on VO_2 devices. We believe that further increase in the thickness would not change its electrical transport characteristics much especially in the case of hybrid dielectric layer.