Supporting Information

One-Step Interface Engineering for All-Inkjet-Printed All-Organic Components in Transparent, Flexible Transistors and Inverters: Polymer Binding

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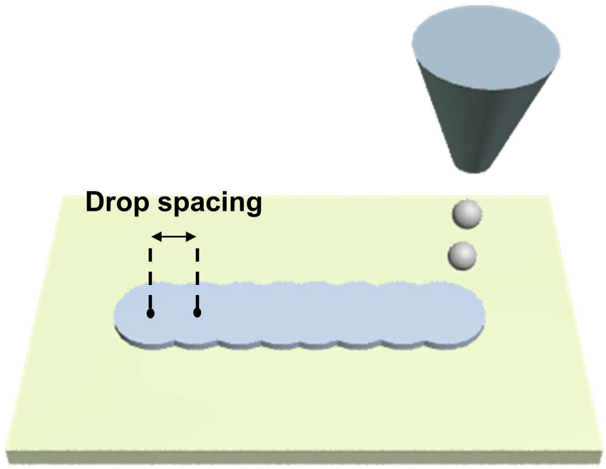

Figure S1. Definition of a drop spacing in the inkjet-printing procedure.

Table S1. The detailed jetting parameters to inkjet-print each layer in this study. Note that a piezoelectric inkjet head contains 16 jetting nozzles, with a diameter of 21 μm, which jet individual ink drops of 10 pL volume.

Jetting parameter	Layer			
	PEDOT:PSS	PVP	PS-Si(CH_3)$_2$Cl	TIPS pentacene
# of nozzles	4	8	16	16
drop velocity [m s^{-1}]	12	8	5	5
frequency [kHz]	5	5	5	5
drop spacing [μm]	25	25	5	5
substrate temperature [°C]	RT	RT	RT	RT

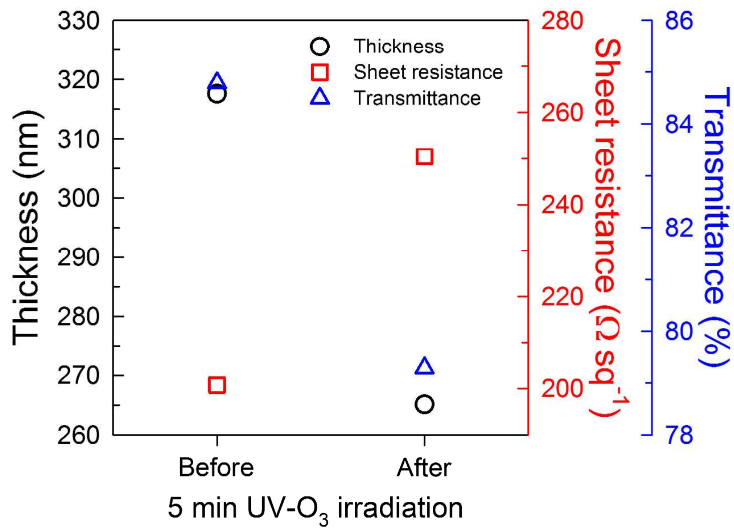

Figure S2. Variations in transmittance and sheet resistance of inkjet-printed PEDOT:PSS layer before and after UV-O_3 irradiation for 5 min.

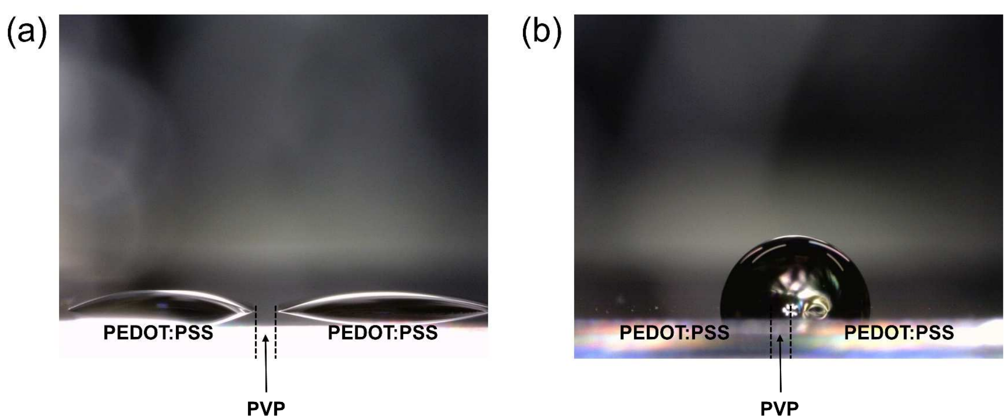

Figure S3. Discernible wetting behaviors of water droplets located on (a) untreated and (b) treated PEDOT:PSS and PVP surfaces.

As shown in Figure S3a, a water droplet was split and preferentially located to hydrophilic PEDOT:PSS sides. In contrast, a similar volume of water formed a singular water droplet with a contact angle of approximately 91° on the polymer-treated PEDOT:PSS and PVP surfaces (Figure S3b).

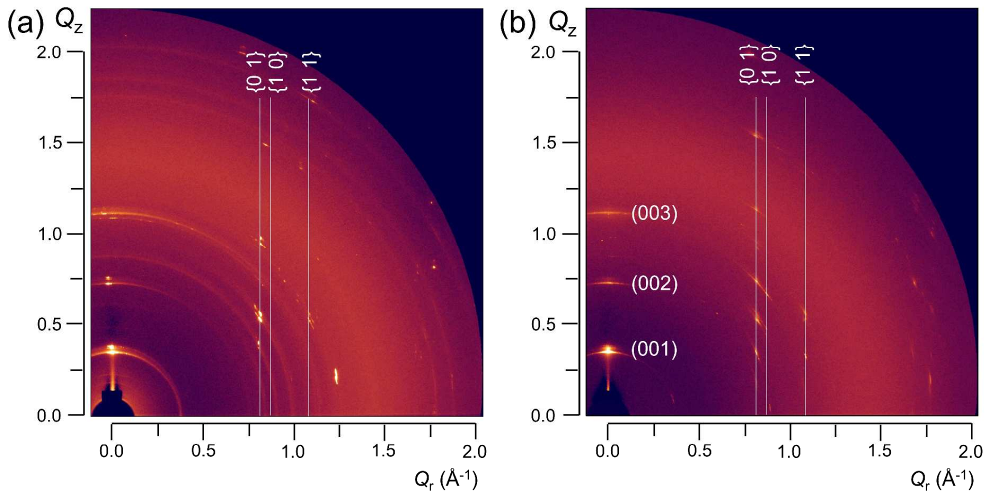

Figure S4. 2D GIXD patterns of TIPS pentacene films inkjet-printed on (a) untreated and (b) PS-Si$(CH_3)_2$Cl-treated surfaces.

Synchrotron-based 2D GIXD (Pohang Accelerator Laboratory, 9A, Korea) was conducted on TIPS pentacene films inkjet-printed onto the untreated and PS-Si$(CH_3)_2$Cl-treated surfaces. Typical area of a TIPS pentacene layer inkjet-printed on a single TFT was approximately 1,500 × 1,500 μm^2, which was hard to be aligned using the GIXD mode with an incident angle of X-ray. Due to this reason, we inkjet-printed 3,000 × 5,000 μm^2 patterned layers of TIPS pentacene on both the untreated and PS-Si$(CH_3)_2$Cl-treated surfaces, which had the same geometry with TFTs used in this study. As shown in Figure S4, TIPS pentacene films on the PS-Si$(CH_3)_2$Cl-treated surface showed highly ordered crystal structure (Figure S4b), in comparison to the untreated system containing less-ordered crystals, as determined by the broad X-ray reflection along the Debye rings (Figure S4a).

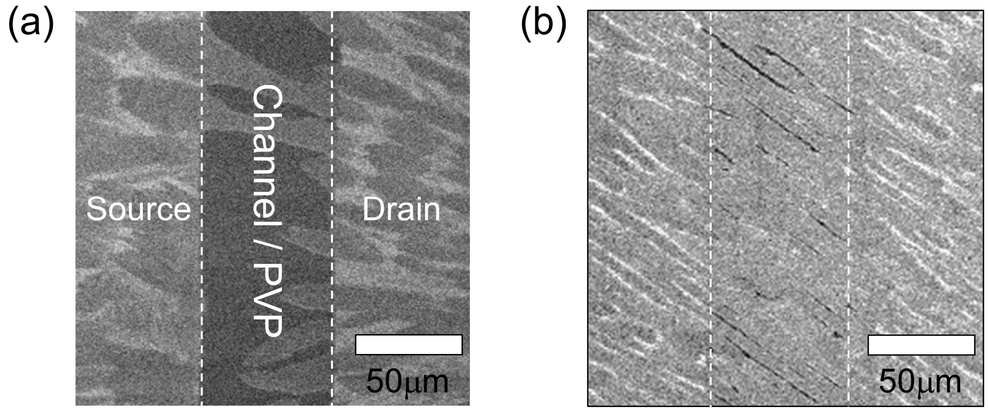

Figure S5. SEM images of the TIPS pentacene channel layers near the contact region inkjet-printed on (a) without and (b) with PS-treated surfaces.

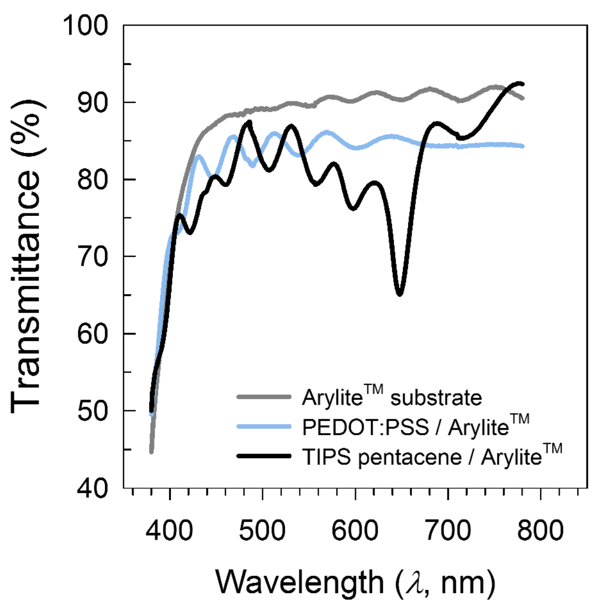

Figure S6. Transmittances of bare Arylite™ film, inkjet-printed PEDOT:PSS, and TIPS pentacene films on the Arylite™ substrate.

Calculation of E_r

From the unloading curve in Figure 4d, the elastic stiffness (S) can be defined as the slope of the tangential line at the uppermost portion of the unloading curve:[R1]

$$S = \frac{dP}{dH} \tag{S1}$$

where P and H are the load force and displacement, respectively.

The loading-unloading process is illustrated schematically in Figure S7. Note that the depth at a final unloaded state (H_f) usually shows a non-zero value due to a plastic deformation observed during the previous loading cycle. The unloading curve can be modeled using a power law relation:

$$P = \alpha (H - H_f)^m \tag{S2}$$

where α and m are power law fitting parameters.

Sink-in depth (H_s) is expressed as follows:

$$H_s = \varepsilon \frac{P_{\max}}{S} \tag{S3}$$

where ε is a parameter related to the indenter geometry.

The vertical displacement of the contact depth (H_c) can be calculated from H_s and the maximum depth (H_{max}):

$$H_c = H_{\max} - H_s = H_{\max} - \varepsilon \frac{P_{\max}}{S} \tag{S4}$$

Finally, E_r can be calculated by the following equation:

$$E_r = \frac{S}{2\beta} \sqrt{\frac{\pi}{A_p(H_c)}} \tag{S5}$$

where β and $A_p(H_c)$ represent a geometrical constant and the projected area at the H_c during loading, respectively.

The measured and extracted parameters of the inkjet-printed PEDOT:PSS and Ag electrodes are summarized in Table S2.

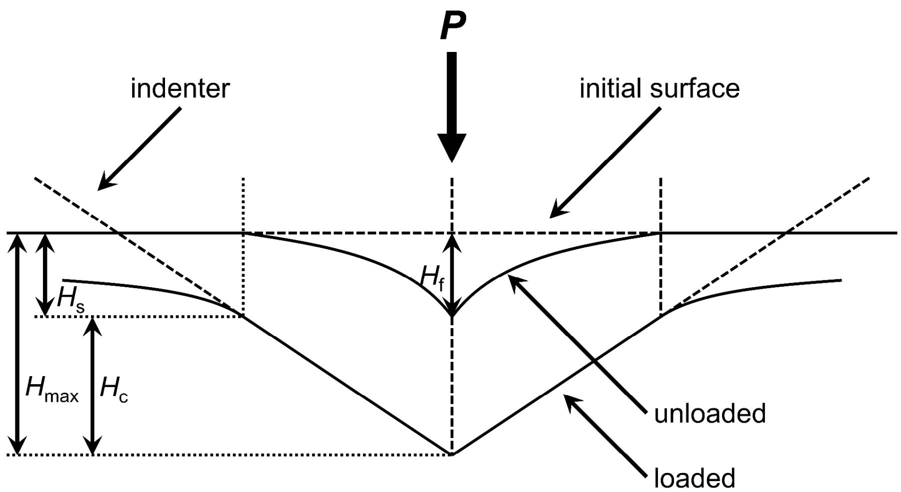

Figure S7. Schematic illustration of the loading-unloading process during a nano-indentation.

Table S2. E_r values of the inkjet-printed PEDOT:PSS and Ag electrodes based on the measured parameters

Parameters	Inkjet-printed PEDOT:PSS	Inkjet-printed Ag
E_r (Gpa)	0.61	47.5
H_c (nm)	193.3	298.24
S (μN nm^{-1})	0.8	156.15
P_{max} (mN)	0.1	6.0
H_{max} (nm)	287.6	405.83
$A_p(H_c)$ (μm^2)	1.25	5.03

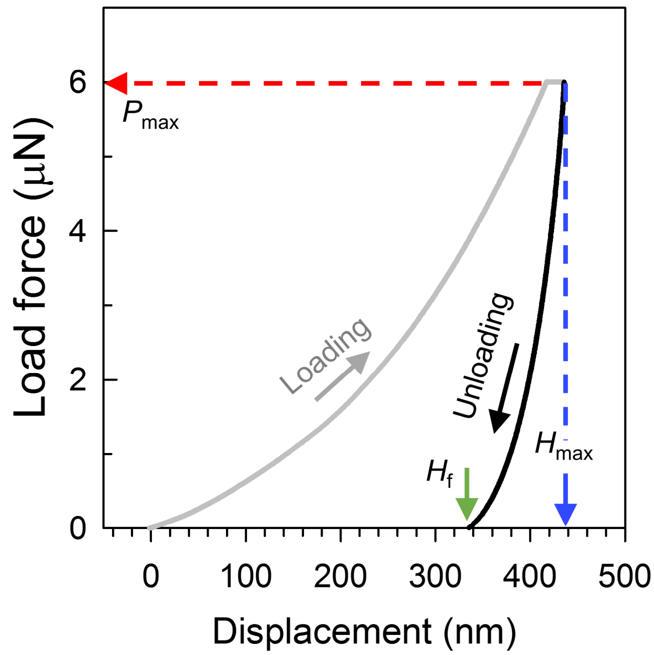

Figure S8. Force – displacement curve of an approximately 400-nm-thick Ag layer on the Arylite™ film during a nano-indenting cycle of loading-unloading.

Calculation of N_{SS}^{max}

From an amorphous silicon transistor model, N_{SS}^{max} can be estimated from the following equation:[R2]

$$N_{SS}^{max} = \left(\frac{SS \log e}{kT / q}\right)\frac{C_{ins}}{q^2} \qquad \text{(S6)}$$

where k, T, q, and C_{ins} represent the Boltzmann constant, the absolute temperature, the electron charge, and the capacitance of the gate dielectric, respectively. From the measured SS and the N_{SS}^{max} values of OTFTs on the untreated and treated surfaces were calculated to be 2.03×10^{12} and 5.12×10^{11} cm^{-2} eV^{-1}, respectively.

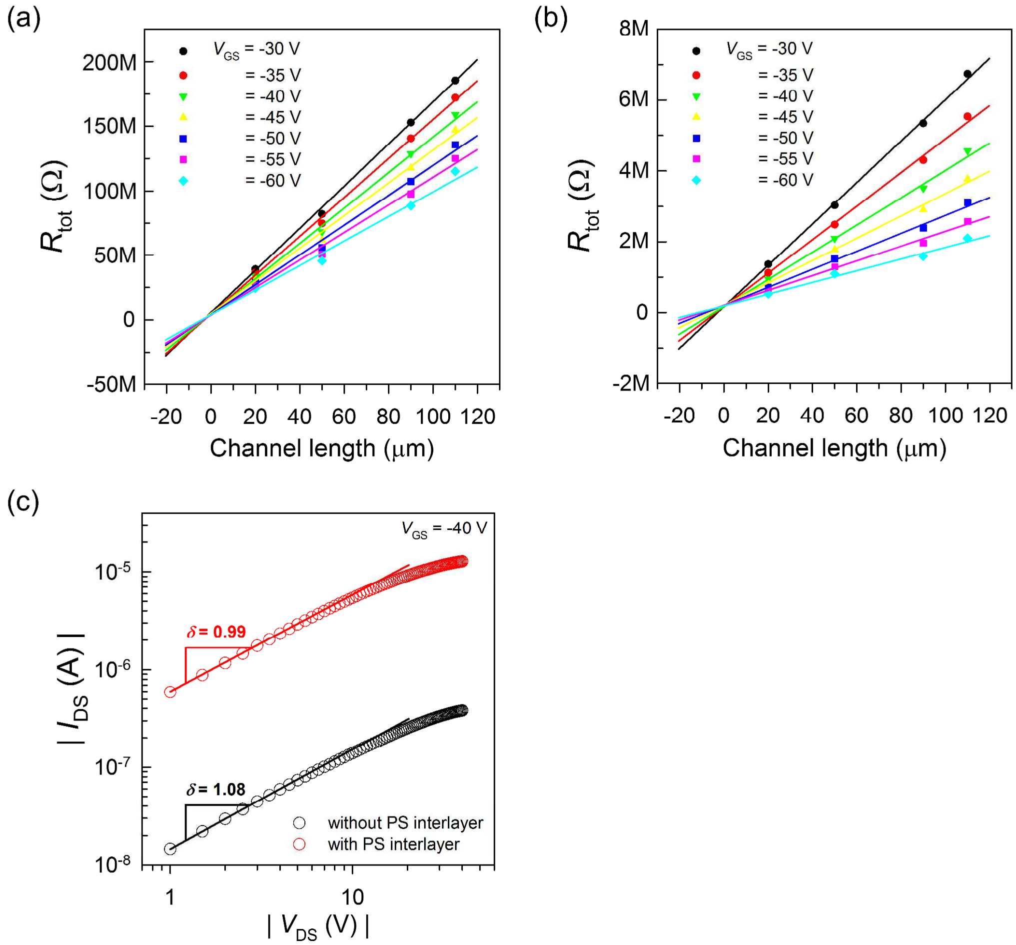

Figure S9. (a, b) TLM results for OTFTs on (a) untreated and (b) treated surfaces. (c) $I_{DS} - V_{DS}$ relationship in log scale of OTFTs.

The R_c values between the PEDOT:PSS *S*/*D* electrodes and TIPS pentacene semiconductor layer were extracted using TLM. In a linear regime, the total resistance (R_{tot}) is expressed as a summation of the channel resistance (R_{ch}) and the R_c:[R3]

$$R_{tot} = R_{ch} + R_c = \frac{1}{\mu_{FET} W C_{ins} (V_{GS} - V_{th} - V_{DS}/2)} L + R_c \qquad \text{(S7)}$$

Based on Equation S7, R_c can be extracted from the y-intercept of the $R_{tot} - L$ graph. Figures S9a and S9b show the $R_{tot} - L$ graphs of the OTFTs on untreated and treated surfaces at V_{DS} = -5

V, respectively. The resulting R_c values of the OTFTs on the untreated and treated surfaces were extracted to be 208 and 16.2 kΩ cm, respectively. The observed R_c values were comparable to those of bottom-contact and top-contact OTFTs with evaporated Au electrodes, respectively.[R4]

Additionally, the $I_{DS} - V_{DS}$ relationship (Figure S9c) strongly supports that the PS interlayer enhanced the contact property between the *S*/*D* electrodes and the semiconductor layer. Assuming $I_{DS} \propto V_{DS}^{\delta}$, a δ value close to 1 indicates that the output characteristic shows good linearity in the low V_{DS} regime. From the graph, δ values of the OTFTs changed from 1.07 to 0.99 by introducing the PS interlayer.

Table S3. Comparative electrical characteristics of previously reported transparent OTFTs

Substrate	Electrode	Semiconductor	μ_{FET} [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	R_c [kΩ cm]	Reference
Arylite™	PEDOT:PSS	TIPS pentacene	0.27	$> 10^6$	16.2	This work
Arylite™	PEDOT:PSS	Pentacene	0.035	$\sim 10^6$	~ 1000	R5
PES	PEDOT:PSS	TIPS pentacene	0.05	$\sim 10^4$	N/A	R6
PET	PEDOT:PSS	TIPS pentacene	0.0078	$\sim 10^4$	N/A	R7
Arylite™	Graphene	Pentacene	0.12	$\sim 10^4$	8 ~ 20	R8
Glass	ITO	P3HT	0.01	$\sim 10^4$	N/A	R9
Glass	ITO	Pentacene	0.226	N/A	260	R10
Glass	Sb_2O_3/Ag/Sb_2O_3	Pentacene	0.3	$\sim 10^3$	N/A	R11
Glass	WO_3/Ag/WO_3	PSeTPTI	0.038	$\sim 2 \times 10^6$	N/A	R12
Glass	WO_3/Ag/WO_3	Pentacene	0.0844	1.2×10^6	252000	R13
Glass	Ag network	DNTT	0.12	$> 10^7$	N/A	R14

Noise Margin

The terminology 'noise' in logic circuits means unwanted variations in voltage or current at logic nodes. If the magnitude of noise is larger than a critical value, known as the noise margin (*NM*) of the logic circiut, it will cause logic errors. When the noise value is smaller than *NM*, the noise will be attenuated as it passes from input to output. As a result, *NM* is used as a factor to specify the range over which the logic circuits will function properly.

For a noiseless system, we can write the equation for an inverter as:

$$V_{out} = f(V_{in}) \tag{S8}$$

With noise v_n added, a noisy output is produced as

$$V_{out}^{'} = f(V_{in} + v_n) \tag{S9}$$

A Taylor series expansion of the output function allows us to examine the important factors determining V_{out} in the presence of noise:

$$V_{out}^{'} = f(V_{in}) + v_n \frac{\partial V_{out}}{\partial V_{in}} + v_n \frac{\partial^2 V_{out}}{\partial V_{in}^2} + \cdots \tag{S10}$$

Because the noise is small, higher-order terms could be ignored. Then, the noisy output could be simplified by the noiseless output plus the noise mulitiplied by A_v of the inverter. Therefore, if the inverter is operated in the region where $| A_v | < 1$, the circuit will attenuate the noise and hold the output in the desired range.

There are two unity gain points, where $A_v = -1$ (Figure S10). The two points are defined as voltage input low (V_{IL}) and voltage input high (V_{IH}). These two unity gain points, the voltage output high (V_{OH}), and the voltage output low (V_{OL}) can be used to define the *NM*s as follows:

$$NM_H = V_{OH} - V_{IH} \tag{S11}$$

$$NM_L = V_{IL} - V_{OL} \tag{S12}$$

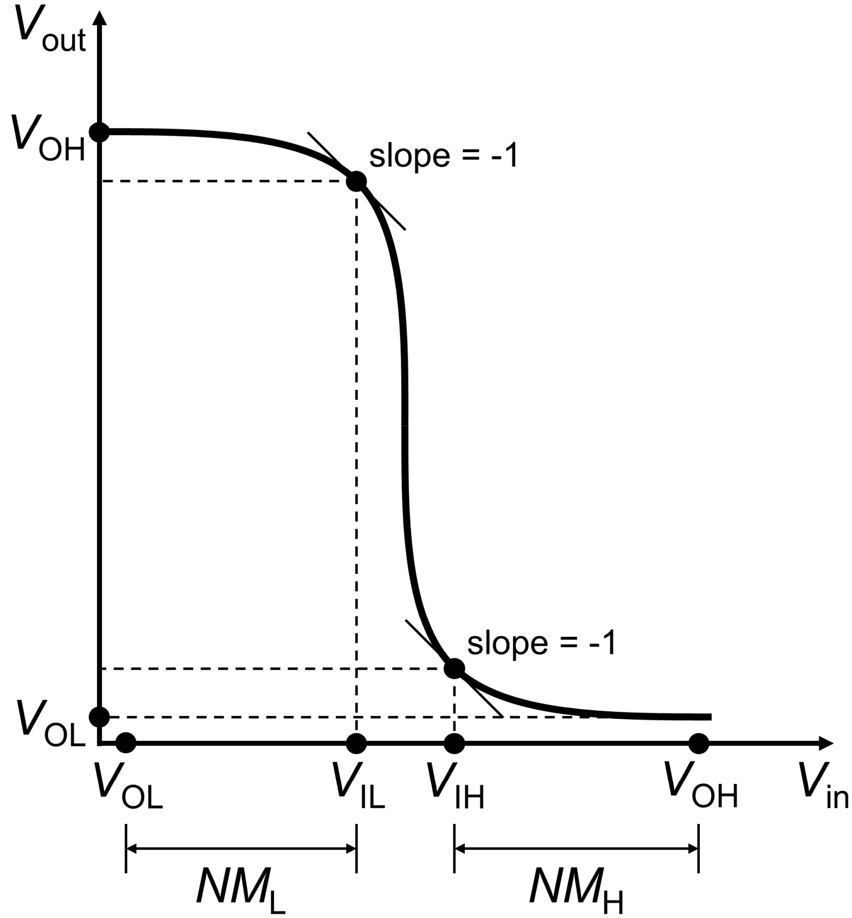

Figure S10. Definition of *NM* in a voltage – transfer curve.

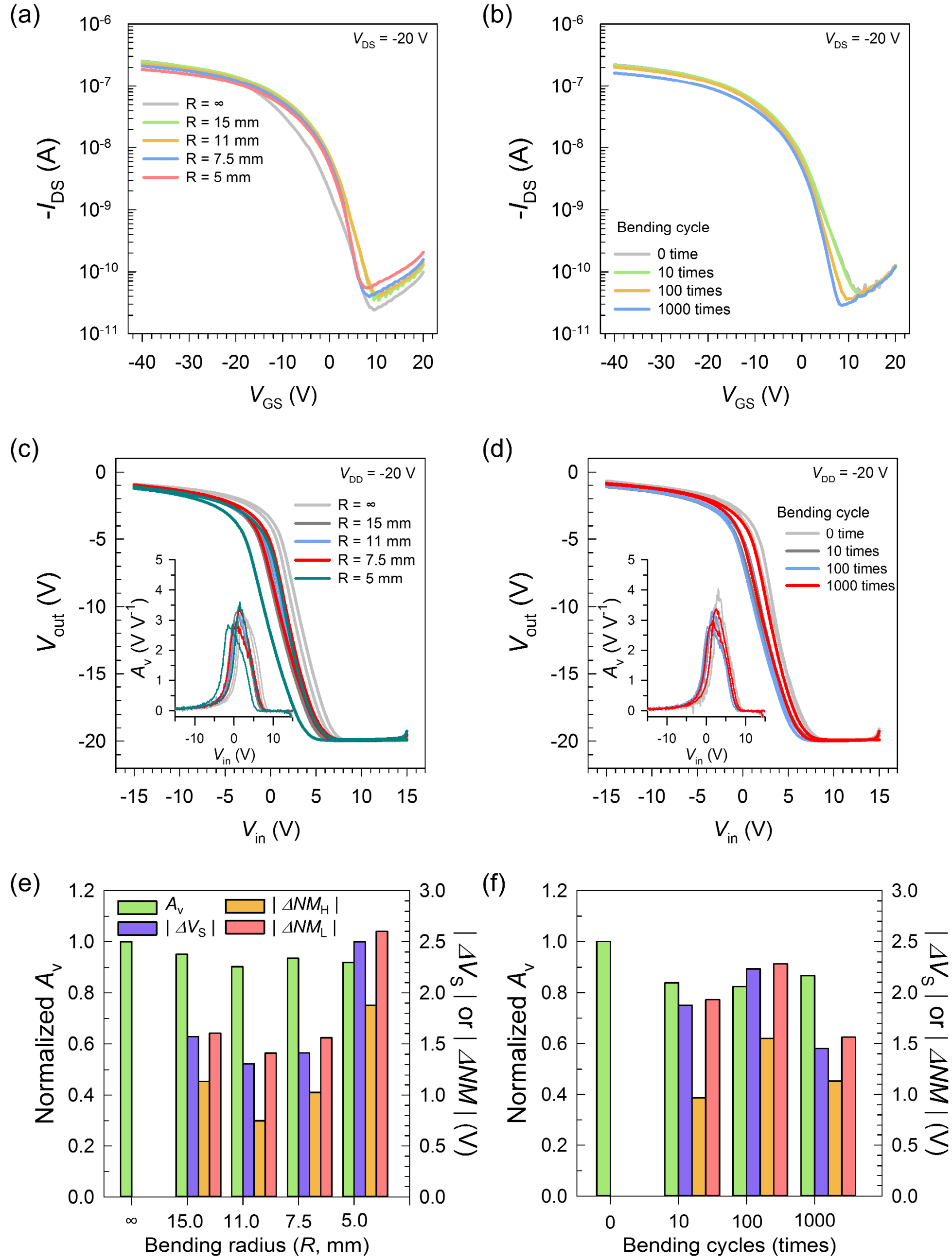

Figure S11. (a, b) $I_{DS} - V_{GS}$ transfer curves of OTFTs and (c, d) $V_{out} - V_{in}$ voltage-transfer curves of organic inverters on the untreated surfaces (a, c) in a bent state with various R values, and (b, d) after different bending cycles at R = 5 mm (the insets in (c) and (d) represent the corresponding $A_v - V_{in}$ curves). (e, f) Subsequent relative changes in the electrical characteristics of the inverters.

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