Supporting Information

to the manuscript

Enabling Energy Efficiency and Polarity-Control in Germanium Nanowire Transistors by Individually Gated Nano-Junctions

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Table of Content

1. Pulsed Measurement Setup

In order to eliminate hysteresis and noise caused by interface defects and border traps a pulsed measurement scheme as proposed by Mattmann *et al*. was applied.[1] Thereto, each individual measurement pulse is followed by a detrapping pulse of the same magnitude in the opposite direction. Figure S1 shows a schematic comparison of the applied voltage scheme at the controlling gate for continuous (red) and pulsed (blue) measurements. In contrast to continuous sweep, in the pulsed regime the gate bias is always switched to its negated value after each pulse. The voltages applied between source and drain contacts are kept constant. It can be seen in Figure 1(c) in the main-paper (in this case, the controlling gate is the back-gate) that this methodology effectively reduced the hysteresis and thus gives access to the intrinsic device properties.

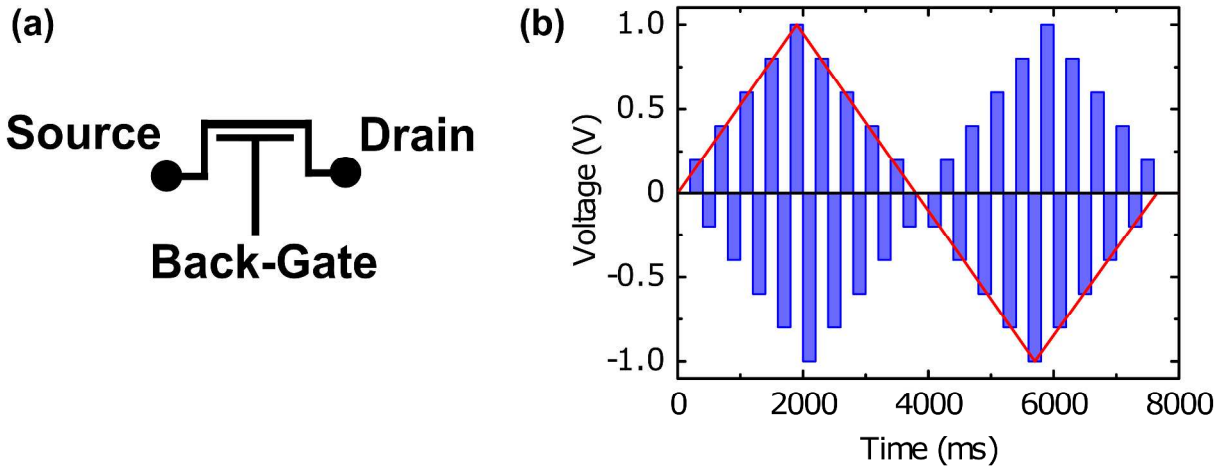

Figure S1: (a) Schematic device layout corresponding to the back-gated characteristics shown in Figure 1. (b) Applied pulse gate sweep method (blue) as compared to the continuous sweep (red) at the gate contact in order to reduce the influence of hysteresis and noise. All measurements are carried out in a common source scheme. Measurement data is shown in Figure 1 within the main paper.

2. XPS results on planar Al_2O_3/GeO_x/Ge Reference samples

The in-situ formation of a GeO_x interface passivation layer during the ALD process was analyzed on planar reference samples using XPS techniques. Thereto, a silicon wafer with a 100 nm thick metal-organic CVD epitaxial grown germanium layer (GeOnSi p-doped with 10^{18} atoms/cm³) were etched in 5% HF solution for 5 min and immediately covered with 24 cycles of Al_2O_3 employing the same process as for the nanowire devices. The XPS analysis was carried out using the $Al_{K\alpha}$ line with energy of 1486.6 eV as X-ray source. Prior to measurement the surface was cleaned for 2 min by Ar sputtering with 500 eV in order to remove surface contamination. As the O1s binding energies of Al_2O_3 and GeO_2 overlap (compare Table StI and Figure S2) the stoichiometry of the interface layer was analyzed based on the Ge3d and Ge2p3 peak positions and compared with database values for GeO_2 and GeO. For both binding energies a distinct oxide peak is present next to the peak assigned with pure Ge-Ge bonds. This is a clear hint on the formation of the intended germanium oxide interface. However, as both positions are located between the literature values of GeO_2 and GeO they could not be unambiguously assigned to one of the oxidation states. Consequently, it can be inferred that the in-situ interface is not pure stoichiometric but rather a mixture of GeO_2 and GeO. Angle resolved X-ray photoelectron spectroscopy (ARXPS) as described in detail by Paynter[2] and Kozlowska[3] was applied in order to estimate the thickness of this interfacial layer to be less than 1 nm. This is in accordance with the cross sectional TEM images of a fully process device shown in Figure 2(c) in the main paper where a formation of a sub-nanometer amorphous interlayer below the Al_2O_3 shell is indicated.

TABLE STI
COMPARISON OF XPS PEAK POSITIONS MEASURED ON A PLANAR Al_2O_3/Ge STACK WITH DATABASE VALUES

EMISSION LINE	Material	NOMINAL BINDING ENERGY (EV)	MEASURED ENERGY VALUES (EV)
O1s	GeO_2	531.6 … 532.3	531.8
	Al_2O_3	531.0 … 532.0	
Ge3d	Ge	28.6 … 29.6	29.7
	GeO	30.9	31.8
	GeO_2	32.5 … 33.1	
Ge2p3	Ge	1217.2 … 1217.6	1217.6
	GeO	1218	1219.9
	GeO_2	1220.2 … 1220.6	

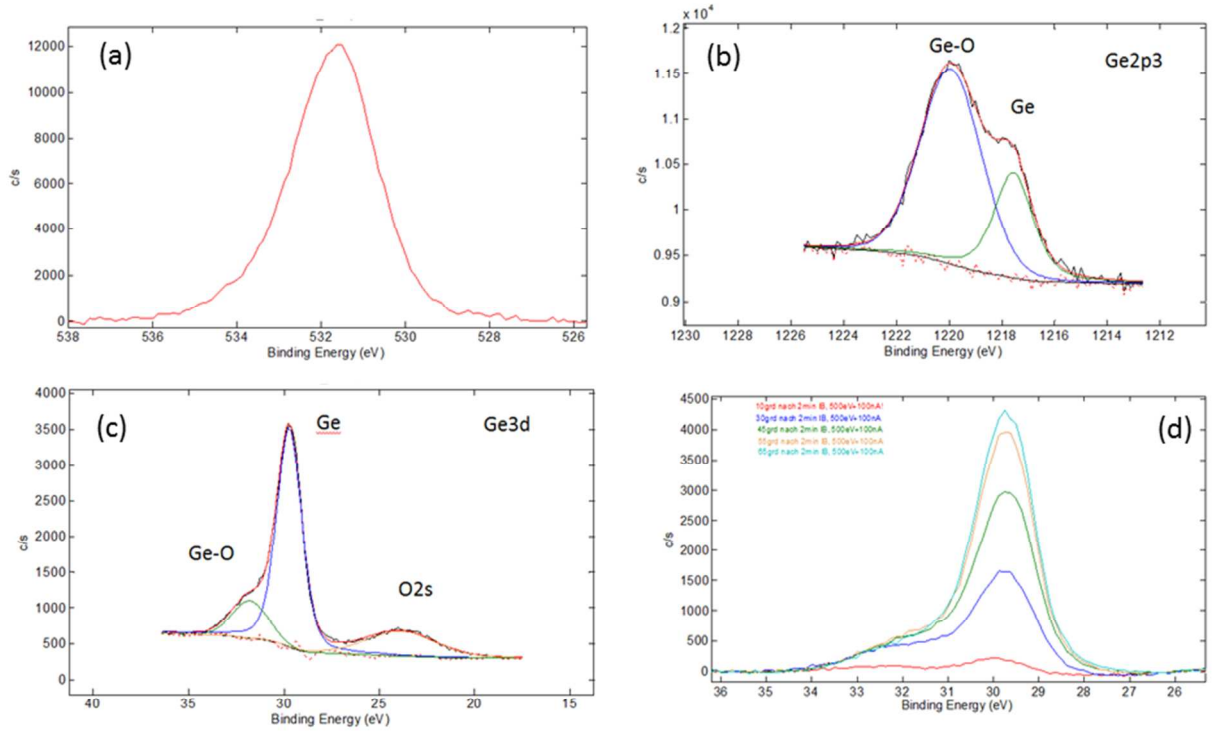

Figure S2: XPS spectra taken from a planar reference sample of the $Al_2O_3/GeO_x/Ge$ stack. (a) Oxide peak, (b) Ge2p3 peak, (c) Ge3d peak (d), evolution of Ge3d peak during ARXPS used for interface thickness determination.

3. Review of Reconfigurable Circuit Design Possibilities

The idea of reconfigurable electronics is to provide a flexible platform, where the end user is able to respond to recent technological developments and adapt the digital circuits through updates without having to directly change the underlying hardware. Reconfigurable electronics thus provide an increased functionality and higher flexibility in the design of circuits and systems as compared to classical CMOS technology. Basically, there are two different methodologies to realize reconfigurable circuits: The redirection of data paths to predefined areas with specific functionalities on the one hand, and the reprogramming of single devices and gates on the other hand. The first approach, known as *coarse-grained* systems, has been already studied since 1984 in the form of Field Programmable Gate Arrays (FPGA), where typically either a multiplexer-tree (MUX-tree) or static random access memory (SRAM) based look-up table (LUTs) is facilitated to provide multiple functions in a user-accessible fashion. In contrast the research in the area of *fine-grained* reconfigurability has just started to evolve in the last few years, mainly due to the earlier lack of an efficient physical concept providing a dynamic reconfiguration on the device level. This changed with the discovery of polarity-control in doping-free nanoscale Schottky barrier transistors.[4,5] The first designs of fine-grain reconfigurable circuits employing polarity-controllable devices were described in 2006 by Ian O'Conner *et al*.,[6,7] who demonstrated the possibility to produce user-configurable dynamic logic blocks out of double-gated carbon nanotube field effect transistors (CNTFETs). The proposed reconfigurable logic blocks had the

possibility to provide up to 8 functions with as little as 9 transistors. However, one drawback of those gates was, that they were not operating completely complementary for every possible combination of input and select signals and thus suffered from output swing degradation. Also, being dynamic logic gates, the need for having two independent clocking signals in order to pre-charge the individual branches limited their applicability in FPGAs. Nonetheless, the cell designs have been improved over the last years by introducing transmission gates.[8] Another versatile approach is resulting out of the transformation rules given by DeMorgan's law. Exploiting the feature of polarity-control, an arbitrary logic gate can be switched to its logical complement simply by reversing all programming voltages and inverting the supply potentials.[9,10] A simple example is given by a six transistor cell that provides not-and (NAND), not-or (NOR) and majority (MAJ) function, which compares to a logic gate with at least 10 transistors in standard CMOS technology. The concept can be extended to exclusive-or (XOR), exclusive-not-or (XNOR) and and-or-invert (AOI) gates.[10] Importantly, the cells always operate in a complementary mode and deliver a full swing output. Different to CMOS, complemental functions exhibit the same delay, which origins from the electrical symmetric underlying device technology.[11] First FPGA architectures have been proposed employing ultrafine-grain reconfigurable logic cells based on such Schottky barrier nanowire field effect transistors.[8,12] In a different approach the increased expressive capability of the polarity-controllable devices is utilized internally in order to yield a higher functional density as compared to classical technologies.[13] As one example Michele DeMarchi *et al*.[14] showed that dual-gated silicon nanowire field effect transistors intrinsically support the XOR function. First measured demonstrator circuits have shown that one and the same cell built from those devices can be operated either as XOR or as NAND gate, depending on the wiring conditions.[15] Dense regular arrays of such cells can consecutively be hard-programmed by the connecting metal layers to the desired functionality. Employing these so called uncommitted logic-gate patters it is possible to design logic circuits in a more compact memory-array-like style, increasing the layout regularity.[16] Further optimization can take place when transistors with three or more independent gates are applied.[12,17] These so-called multiple-independent-gate field effect transistors (MIGFETs) can be used to merge several transistors in series into a single device. As a result more compact circuit designs can be achieved despite the larger individual footprint of the devices themselves. We have recently calculated that an 8-bit full adder circuit can be built from roughly half the number of transistors.[18] Indeed a high number of junctions and isolations are saved, reducing the overall size, even if the individual device is larger. First assessments have indicated that those fine-grain reconfigurable circuits have benefits in terms of performance and energy consumption, while also needing less area than a comparable CMOS FinFET or fully-depleted silicon-on-insulator (FDSOI) technology.[12,16,18–20]

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