Supporting Information

Low-Voltage and High Performance Multilayer MoS_2 Field-effect Transistors with Graphene Electrodes

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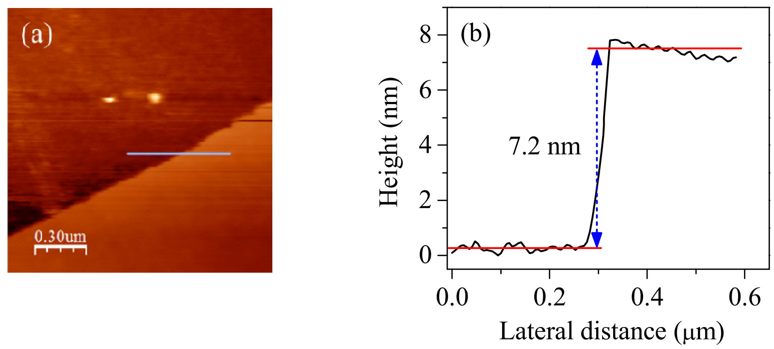

Figure S1. Atomic force microscopic image of a) ML MoS_2 and b) corresponding height profile for ML MoS_2 films. The thickness is about 7.2 nm, indicating 10 MoS_2 layers.

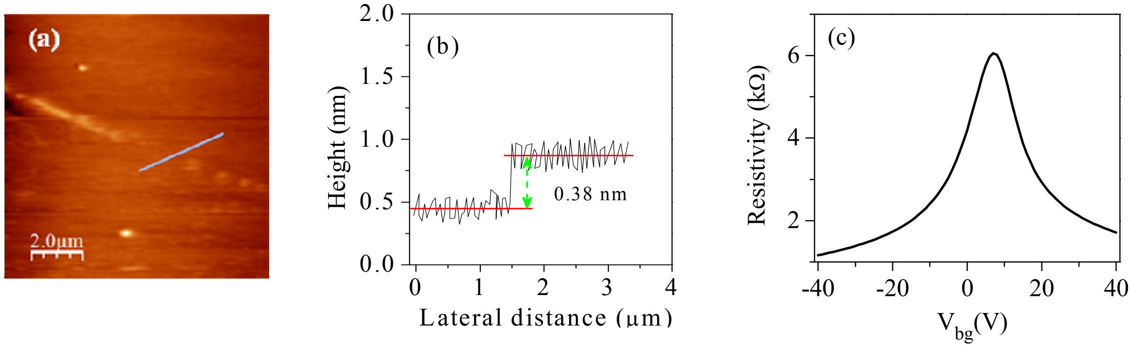

Figure S2. Atomic force microscopic image of a) CVD-grown SLG and b) corresponding height profile. The thickness is about 0.38 nm, indicating SLG. c) Resistivity as a function of back gate voltage (V_{bg}) for CVD grown SLG

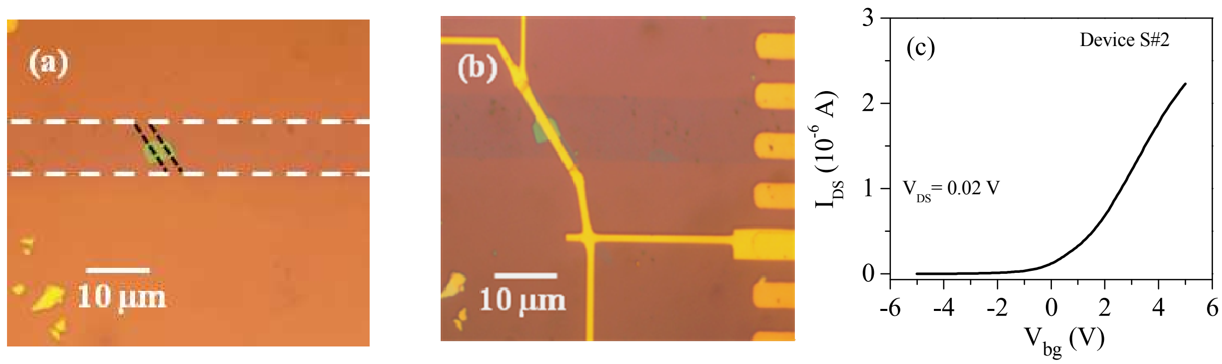

Figure S3. a) Optical image of the fabricated device (device S#2), CVD-grown SLG as the source–drain electrode, and ML MoS_2 as the channel material. b) Optical image of the fabricated top-gated ML MoS_2 transistor. The ML MoS_2 is covered with 15-nm-thick film of ALD-deposited Al_2O_3 acting as a gate dielectric and Cr/Au with 5/80 nm for the top-gated electrodes. c) Plot of I_{DS}–V_{bg} of the ML MoS_2 transistor after Al_2O_3 deposition at V_{DS} = 0.02 V. Mobility of device S#2 is estimated found to be 466 cm^2/Vs.