## **Supporting Information**

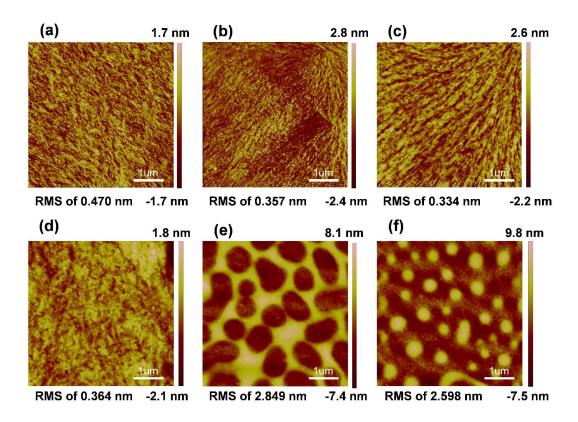
## Non-volatile Transistor Memory with Self-assembled Semiconducting Polymer Nanodomain Floating-Gates

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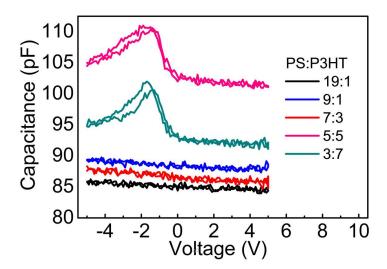
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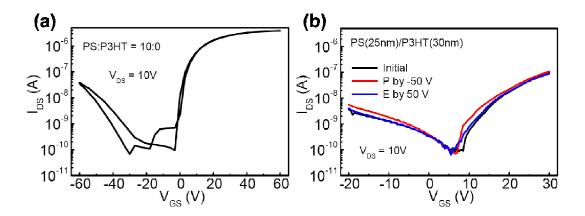
E-mail: cmpark@yonsei.ac.kr



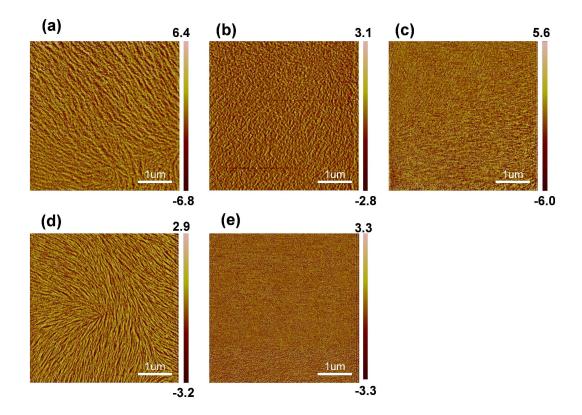
**Figure S1.** TM-AFM images in height contrast of (a) a thin P(NDI2OD-T2) film on the surface of a SiO<sub>2</sub>/Si substrate and (b–f) all-in-one tunneling:floating-gate layers comprising PS:P3HT at different proportions of 19:1, 9:1, 7:3, 5:5, and 3:7, respectively. The area size is  $5 \mu m \times 5 \mu m$ .



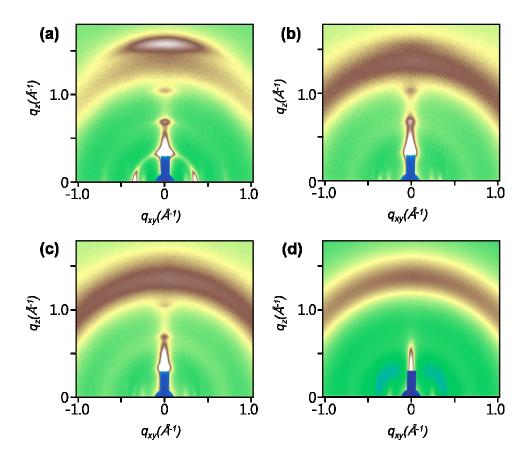
**Figure S2.** The measured capacitance vs. voltage of the capacitors containing blend films of PS and P3HT with different blend compositions. Si++ and Al were used as bottom and top electrode, respectively.



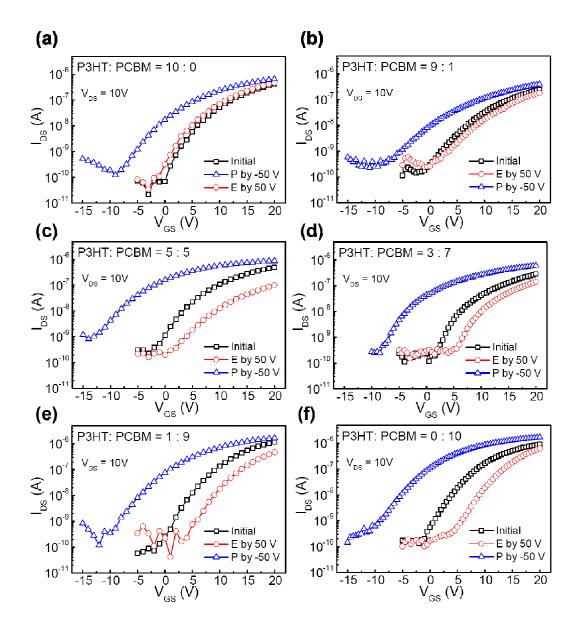
**Figure S3.** Transfer characteristics of (a) an OFET without P3HT floating-gate and (b) an OFET memory with a continuous planar P3HT floating-gate sandwiched between the PS and PMMA layers.



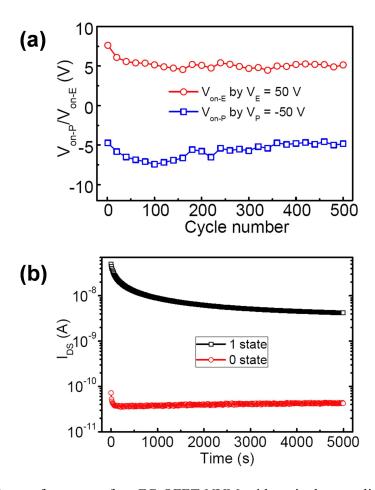
**Figure S4.** TM-AFM images in phase contrast of the ternary blended films of PS:[P3HT:PCBM] tunneling:double floating-gate spin-coated on the surface of P(NDI2OD-T2) at different proportions of P3HT:PCBM: (a) 1:9, (b) 3:7, (c) 5:5, (d) 9:1, and (e) 0:10. The area size is 5  $\mu$ m × 5  $\mu$ m.



**Figure S5.** 2D GIXD images of the ternary blended films of PS:[P3HT:PCBM] tunneling:double floating-gate at different proportions of P3HT:PCBM: (a) 9:1, (b) 5:5, (c) 3:7, and (d) 1:9.



**Figure S6.** Transfer characteristics of FG-OFET-NVMs with single tunneling:double floating-gate (PS:[P3HT:PCBM]) layers at the different proportions: (a) 10:0, (b) 9:1, (c) 5:5, (d) 3:7, (e) 1:9, and (f) 0:10.



**Figure S7.** Device performance of an FG-OFET-NVM with a single tunneling:floating-gate layer of PS:PCBM (7:3). (a) Switching endurance and (b) retention properties.