

Supporting Information

InSb Nanowires with Built-In $\text{Ga}_x\text{In}_{1-x}\text{Sb}$ Tunnel

Barriers for Majorana Devices

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Section 1 (S1): Growth of InSb/Ga_xIn_{1-x}Sb/InSb nanowires

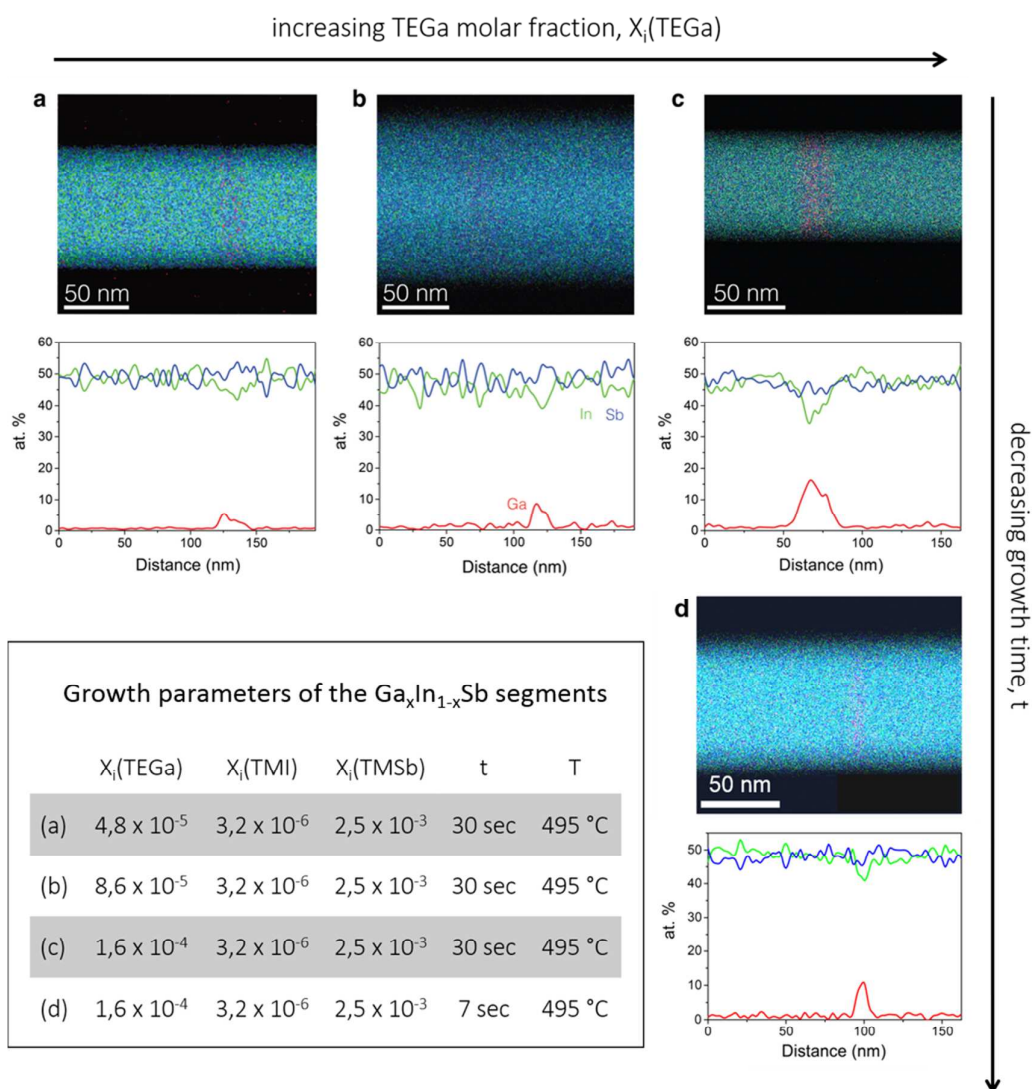


Figure S1. Tuning the composition and length of Ga_xIn_{1-x}Sb segments. From the EDX maps and line scans shown in (a)–(d) we can extract the composition and length of respective Ga_xIn_{1-x}Sb segments. (a)–(c) By increasing the TEGa source flow while keeping the growth time fixed, we increase the Gallium content in the Ga_xIn_{1-x}Sb segments while keeping the segment length fixed: (a) Ga_{0.1}In_{0.9}Sb, 20 nm (b) Ga_{0.15}In_{0.85}Sb, 20 nm (c) Ga_{0.28}In_{0.72}Sb, 20 nm. By reducing the growth time from (c) 30 sec to (d) 7 sec, we reduce the length of the barrier from 20 nm to 7 nm. The chemical composition of the segment shown in (d) is Ga_{0.21}In_{0.79}Sb. The table in the inset shows the growth parameters used to synthesize the Ga_xIn_{1-x}Sb segments of different samples.

InSb/Ga_xIn_{1-x}Sb/InSb nanowire heterostructures have been synthesized by Au-catalyzed Vapor-Liquid-Solid (VLS) growth mechanism in an Aixtron Metal Organic Vapor Phase Epitaxy (MOVPE) machine. The growth was catalyzed by 30 nm Au colloids dispersed on an (001) InP

substrate. InP nanowires are used as stems for InSb nanowire growth (see D.Car et al. *Adv. Mater.* **2014**, 26 (28), 4875–4879). For all samples, the InSb bottom and top nanowire segments were grown at 495 °C using tri-methyl-indium (TMI) and tri-methyl-antimony (TMSb) with precursor molar fractions $X_i(\text{TMI}) = 1.1 \times 10^{-5}$ and $X_i(\text{TMSb}) = 1.7 \times 10^{-3}$, for 8 (6) minutes for the bottom (top) segment. The growth parameters used for the growth of the intermediate $\text{Ga}_x\text{In}_{1-x}\text{Sb}$ segments of different samples are listed in the inset of **FigureS1**. In all the runs, the growth was interrupted for 2 min before and after the growth of the $\text{Ga}_x\text{In}_{1-x}\text{Sb}$ segments to adjust the flow in the gas lines and ensure the abruptness of the interfaces.

Section 2 (S2): Extracting the length of the barriers from HRTEM images

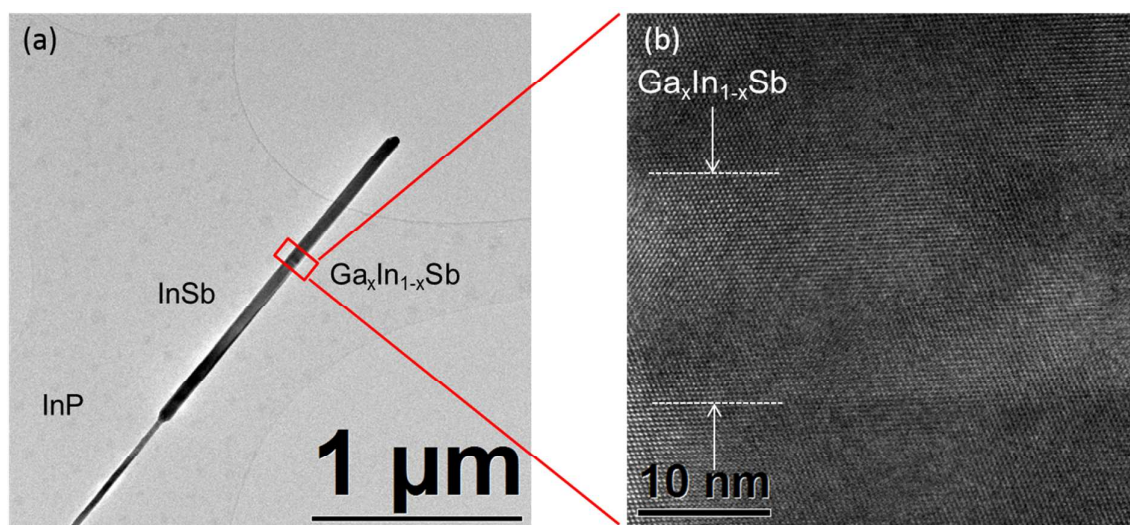


Figure S2. The length of the barrier as extracted from HRTEM image. (a) Bright-field, low-magnification TEM image of a nanowire from sample grown with the highest Ga molar fraction for 30 sec ($\text{Ga}_{0.28}\text{In}_{0.72}\text{Sb}$, 20 nm; Figure S1c). The nanowire is uniform in diameter and non-tapered. (b) A HRTEM image of a nanowire segment containing the barrier. The $\text{Ga}_x\text{In}_{1-x}\text{Sb}$ segment appears brighter in contrast in HRTEM images. Measured barrier length is 18 nm, which is in good agreement with the value obtained from EDX line scan (~20 nm). In addition, from HRTEM image we can see that there are no misfit dislocations present.

Section 3 (S3): Transverse EDX line scan shows no radial overgrowth

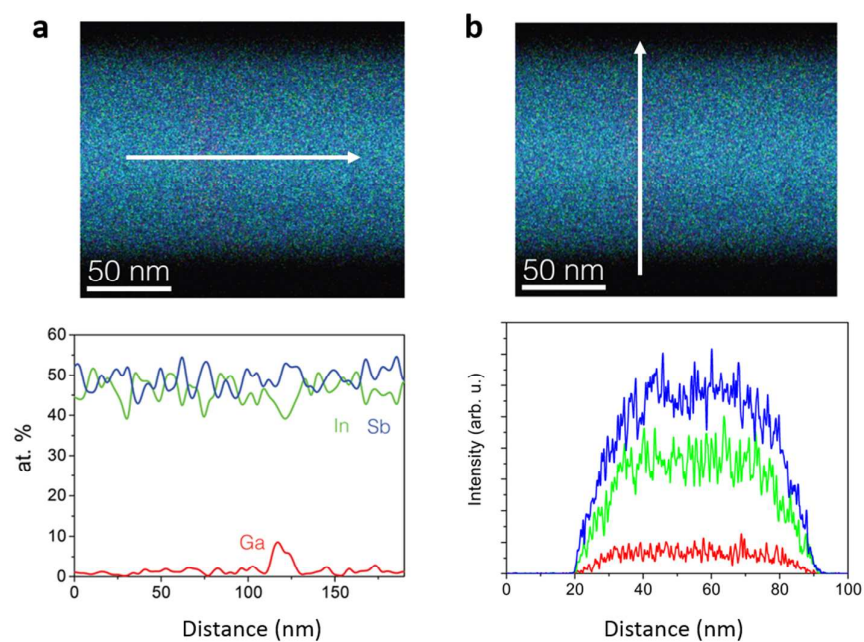


Figure S3. (a) Lower panel: EDX line scan taken along the axial direction (indicated by a white arrow in the XEDS map in the upper panel), revealing the barrier composition $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ and thickness 20 nm. (b) Lower panel: EDX line scan taken along the radial direction (indicated by a white arrow in the EDX map in the upper panel) of the same $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ segment. The barrier spans the full diameter of the nanowire.

Section 4 (S4): Strain quantification of a $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ segment

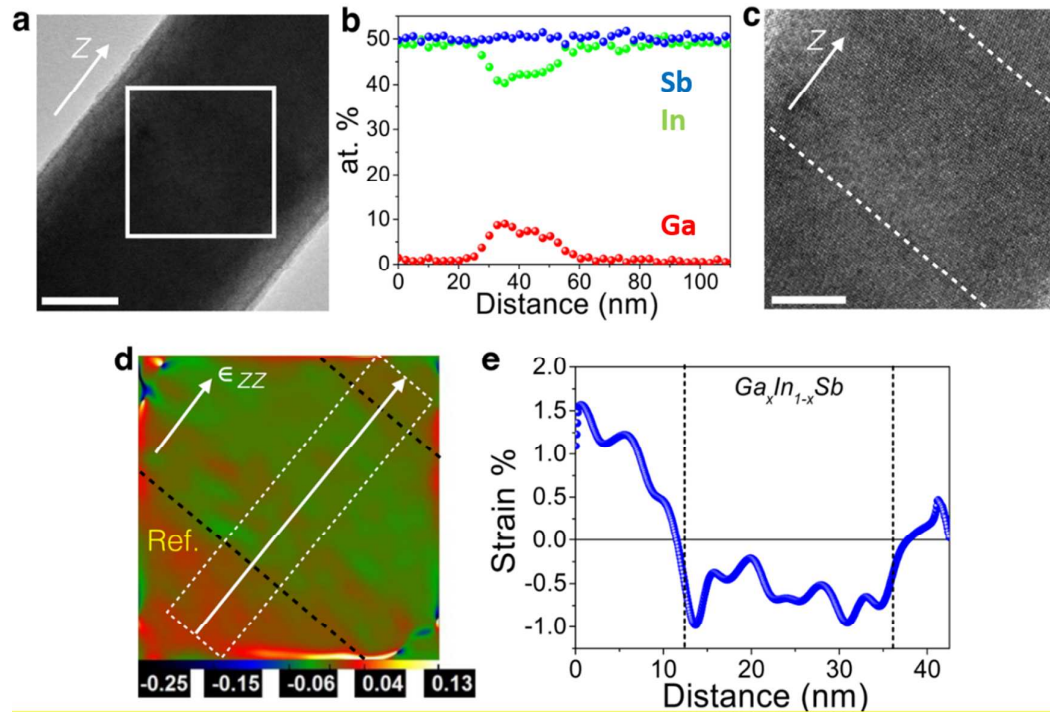


Figure S4. Strain in the InSb- $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ -InSb axial nanowire heterostructure. (a) Bright field TEM image of the nanowire segment containing the barrier. The arrow indicates the nanowire growth direction. Scale bar corresponds to 20 nm. (b) EDX line scan taken along the nanowire growth direction shows the presence of a 20 nm thick $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ barrier. (c) High resolution TEM image of the region indicated by a square in (a). Scale bar corresponds to 10 nm. (d) Geometrical phase analysis applied to the (1-11) planes of the HRTEM image shown in (c). The $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ segment is compressively strained with respect to the InSb reference (Ref.) region. (e) The strain profile integrated along the direction indicated by a white arrow in (d). The average value of strain in the barrier is around $\sim -0.8\%$.

Section 5 (S5): Statistics on the position of the barrier within the nanowire

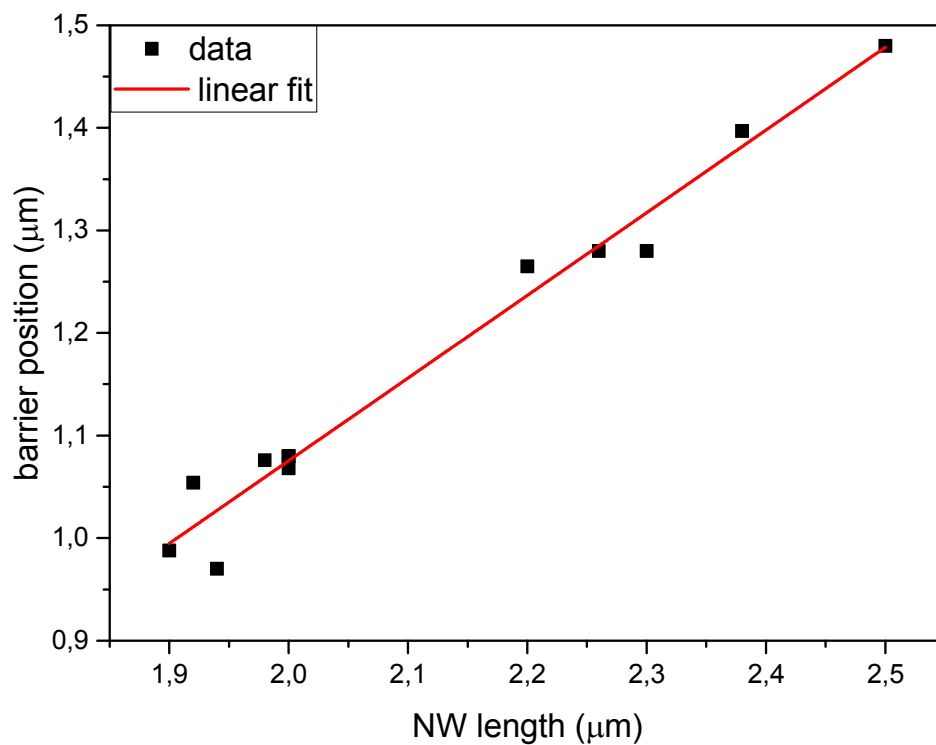


Figure S5. Statistical analysis of the sample containing the highest amount of Gallium ($\text{Ga}_{0.28}\text{In}_{0.72}\text{Sb}$) incorporated in a 20 nm thick barrier. The analysis was done to facilitate device fabrication by determining the position of the built-in barrier within the nanowire. The position of the barriers depends on the total length of the InSb wire. The spread in InSb NW growth rate is probably induced by fluctuations in Au catalyst density. The plot of barrier position (distance from the bottom of the InSb nanowire to the barrier) vs InSb nanowire length follows a linear law ($y=a+bx$; $a=(-0.54\pm0.09)\mu\text{m}$; $b=0.81\pm0.04$; the coefficient of determination (R-square value) is 0.97) and enables accurate prediction of the barrier position. A total of 11 nanowires was analyzed.

Section 6 (S6): Detailed device fabrication recipe

Substrate Cleaning

Acetone (10 minutes), IPA (10 minutes), Oxygen plasma (10 minutes, pressure: 1mbar, power 600 watts).

Fabrication of Local Gates

Spin PMMA 950KA2 at 3000 rpm, bake at 175 °C for 15 minutes

Write local gate patterns (50 nm wide gates, 50 nm spacing) using e-beam lithography (dose: 1400 $\mu\text{C}/\text{cm}^2$)

Developing for 60 seconds in MIBK (4-Methyl-2-pentanone): IPA, ratio 1:3

Rinse in IPA for 60 sec, blow dry

Evaporation of 5 nm Ti and 10nm Au

Lift-off in acetone overnight (with ultrasound for the first hour).

Mechanical Exfoliation of Hexagonal Boron Nitride Flakes, Deterministic Transfer of the Flakes onto the Fine Bottom Gates

Nanowire Deposition

Nanowires are transferred from the growth chip deterministically using a micromanipulator in SEM at 3 kV to the Si/SiO₂ chip between the alignment markers.

Contact Deposition

Spin PMMA 950(K) – A4 at 4000 rpm, bake at 175 C for 15 min

Writing contact patterns using e-beam lithography (dose: 1500 $\mu\text{C}/\text{cm}^2$)

Developing for 60 sec in MIBK (4-Methylpentanon-2-one): IPA, ratio 1:3

Descum PMMA residues with oxygen plasma (60 sec, 1 mBar, 600 W)

Sulfur passivation:¹ Diluted ammonium polysulfide (NH₄)₂S_x solution (3 ml of (NH₄)₂S mixed with 290 mg sulfur powder then diluted with DI-water at a ratio of (1 : 200) for 30 min at 60 °C.

He Ion etching with a Kauffman ion source for 30 sec at 1.5-1.6 x 10⁻² mbar

Evaporation of 10 nm Cr and 100nm Au

Lift-off in acetone overnight at room temperature.

(1) Suyatin, D. B.; Thelander, C.; Björk, M. T.; Maximov, I.; Samuelson, L.; Björk, M. T.; Maximov, I.; Samuelson, L. *Nanotechnology* **2007**, 18 (10), 105307.

Section 7 (S7): Detailed explanation of the I-V fitting model

The height and width of the barrier are extracted from a least-square non-linear fit of the experimental I-V traces. The least-square non-linear fit is based on a simple theoretical model: When a voltage bias is applied, the bias drops linearly across the barrier width, resulting in a tilted barrier (**Figure S7c**). Then the tunneling transmission probability as a function of energy, $T(E)$, is calculated using WKB approximation:

$$T(E, V_{bias}) = \exp\left(-\int_{x_L}^{x_R} 2\sqrt{2m(V(x) - E)/\hbar^2} dx\right)$$

where x_L and x_R are the classical turning points, V is the barrier potential energy and \hbar is the reduced Planck constant.

As illustrated in **Figure S7** two different barrier potential profiles are used: rectangular and Gaussian.

Rectangular barrier:

$$V(x) = V_{barr} \left[H\left(x + \frac{L}{2}\right) - H\left(x - \frac{L}{2}\right) \right] + eV_{bias} \left(\frac{1}{2} - \frac{x}{L} \right)$$

Gaussian barrier:

$$V(x) = V_{barr} \exp\left(-\frac{x^2}{(2\sigma)^2}\right) + eV_{bias} \left(\frac{1}{2} - \frac{x}{L} \right)$$

Where $H(x)$ is the Heaviside step function, $x_L = \min(x | V(x) = E_F)$, $x_R = \max(x | V(x) = E_F)$

The width of the rectangular barrier is defined with respect to the shape at zero bias (**Figure S7a**) and is equal to the separation of the classical turning points ($x_L - x_R$) for an electron at the Fermi level and the barrier height equals the difference between the top of the barrier and the Fermi level, $V - E_F$. The width of the Gaussian barrier (**Figure S7b**) is defined as 2 standard deviations (2σ) of a Gaussian at zero bias and the height as the difference between the peak height of the Gaussian and the Fermi level, $V_{barr} - E_F$

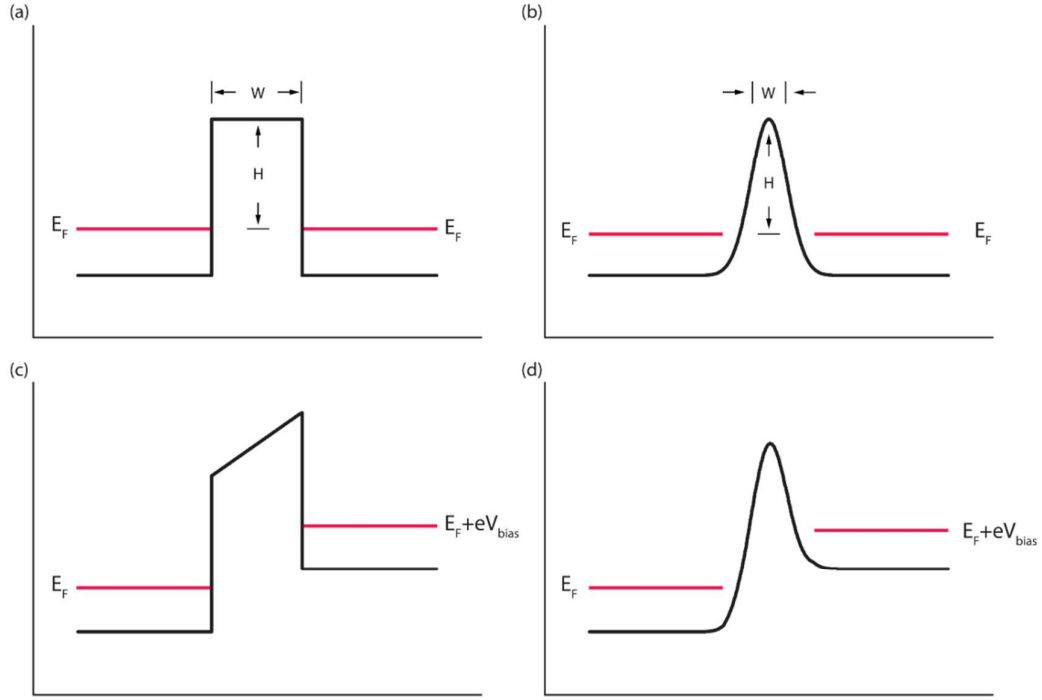


Figure S7. Schematics showing the potential landscape of the barrier region for the rectangular and Gaussian barriers assumed in the calculation of the transmission for the WKB fittings. Panel (a) and (b) show the barrier at zero bias voltage with the Fermi level indicated by red lines. Panel (c) and (d) show how the potential profile is modified at finite bias with a linear voltage drop across the barrier width.

After the transmission probability $T(E)$ is calculated, the current I is obtained from the Landauer–Buttiker formula at zero temperature.

$$I(V_{bias}) = \frac{2e^2}{h} \int_{E_F}^{E_F + eV_{bias}} T(E, V_{bias}) dE$$

The assumption of zero temperature is valid due to the fact that the barrier height energy scale ($>20\text{meV}$) is much larger than the thermal energy scale ($<1\text{meV}$ at 2 Kelvin).

Section 8 (S8): Additional WKB fits of I-V traces

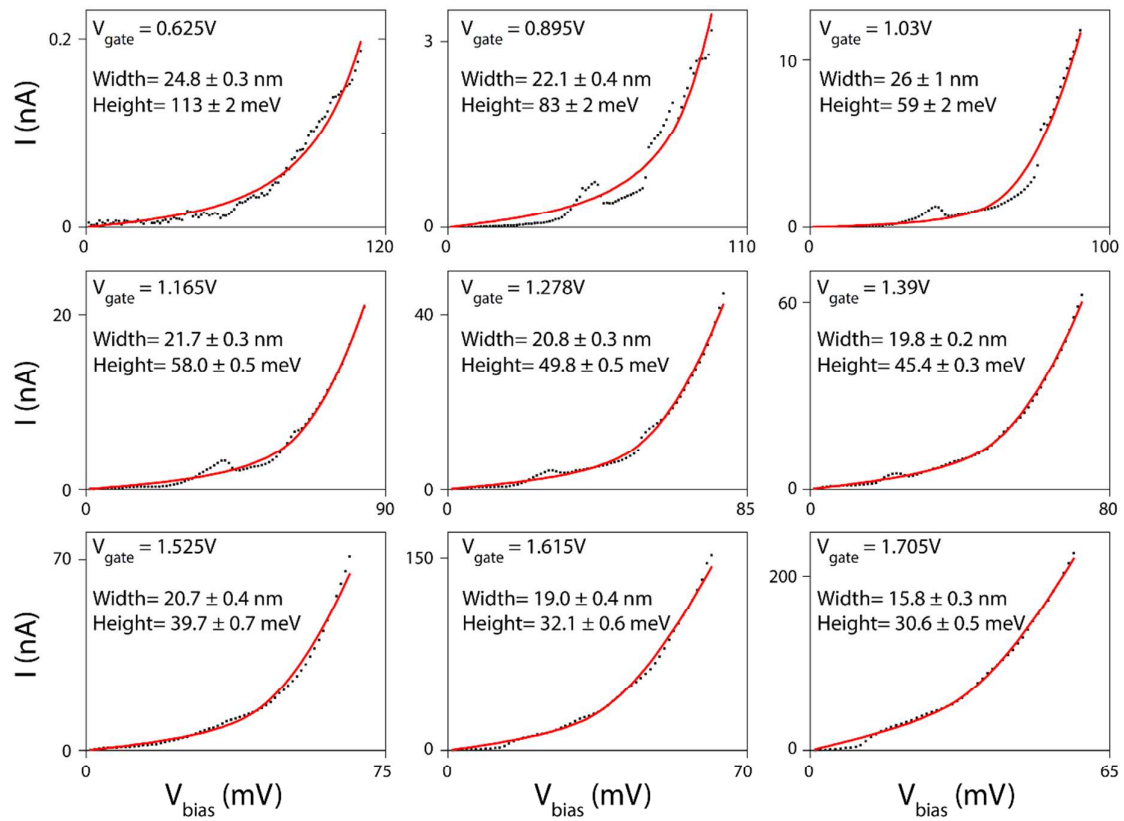


Figure S8. Representative WKB fitting curves, for I-V traces taken at gate-voltage values from 0.6 V to 1.7 V. As can be seen, the WKB model based on a simple, square-shaped potential profile shows excellent fit with experimental data for gate voltage values in the range from 0.625 V to 1.705 V. As the gate voltage increases from 0.625 V to 1.705 V, the current changes from 0.2 nA to 200 nA, *i.e.* by 3 orders of magnitude.

Section 9 (S9): A possible explanation of the asymmetric I-V characteristics

The asymmetry of the I-V traces between positive bias and negative bias is more pronounced at low gate voltage values. We draw a possible explanation for this observation based on device asymmetry when the Fermi level lies below the conduction band. **Figure S9a** shows the potential landscape for zero bias voltage. **Figure S9b** depicts the case for negative bias. The bias voltage drops over the built-in barrier as well as the resistive nanowire section for which the Fermi level is below the conduction band. **Figure S9c** depicts the case for positive bias. There is an additional barrier apart from the built-in one which electrons have to tunnel through, causing an asymmetry for positive bias.

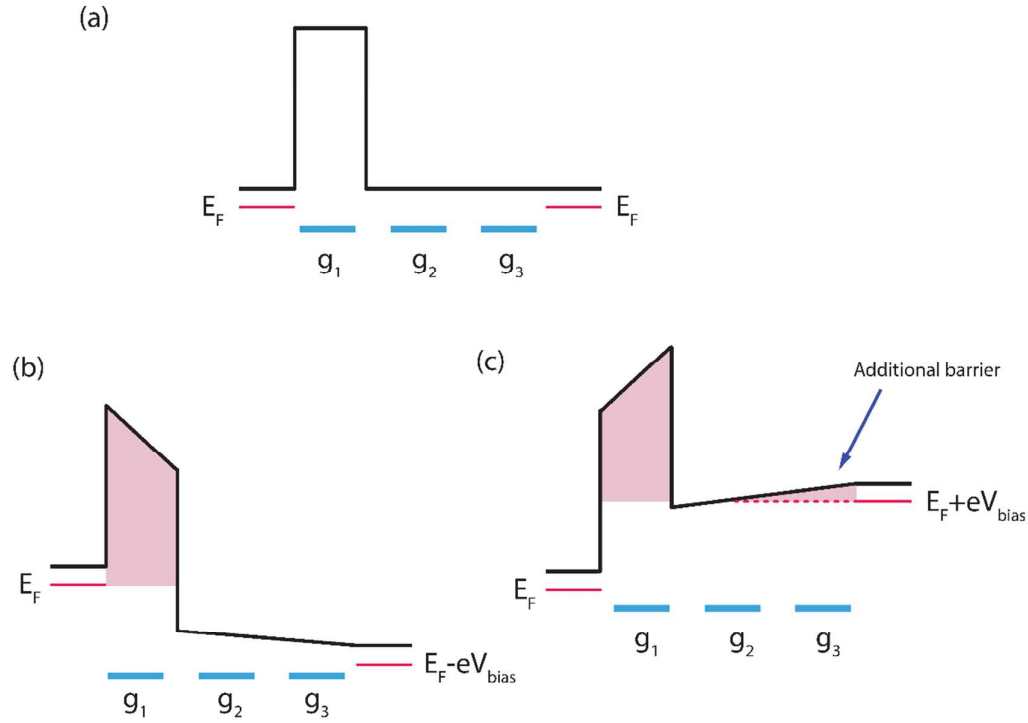


Figure S9. Potential landscape for less positive gate voltages. (a), (b) and (c) are for 0, negative and positive bias voltages, respectively. The three local back-gates are denoted as g_1 , g_2 and g_3 .

We point out that this is a simplified model: In the vicinity of the conduction band bottom, the potential fluctuations due the local gates are more pronounced (e.g. the nanowire part in-between g_1 and g_2 is less capacitively coupled to the gates than the nanowire part right above the g_1 or g_2). Thus it is expected that our simple square-shaped barrier model no longer holds in this regime.

These effects (asymmetric biasing and potential fluctuations) can be minimized by applying more positive gate voltage to drag the conduction band bottom way below the Fermi level. In this case, the transport (which mainly happens near the Fermi level) is not sensitive to the details of the conduction band bottom, and our theory model fits to the data very well (**Figure 4** in the maintext).

Section 10 (S10): Transport measurements of an InSb/Ga_{0.15}In_{0.85}Sb/InSb nanowire device.

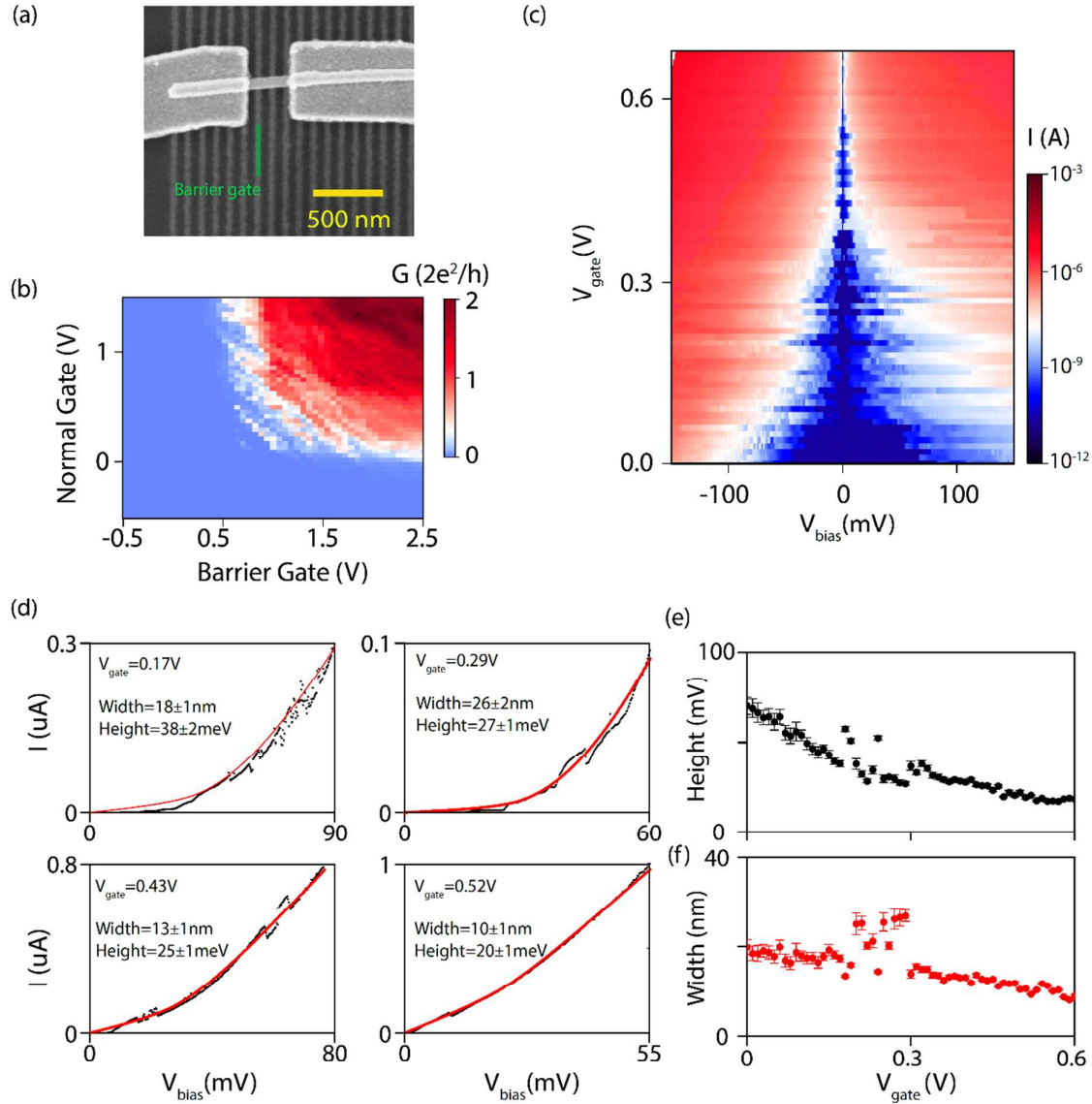


Figure S10: Transport measurements of an InSb/Ga_{0.15}In_{0.85}Sb/InSb nanowire device. The Ga_{0.15}In_{0.85}Sb segment is expected to be 20 nm wide, as determined by TEM/EDX (Figure 1e in the main text). (a) Top-view SEM image of the device. The barrier gate is indicated by a green line. The normal gate is the local gate right next to the barrier gate (on the right-hand side). (b) Color plot of conductance G as a function of barrier gate and normal gate voltage, at 0 bias voltage (lock-in measurement). The threshold voltage difference between the barrier gate and the normal gate is 0.5 V, which is smaller than the threshold voltage difference between the barrier gate and the normal gate of the device in the main text Figure 3d (1.8V). This is expected because the device reported here has a barrier with lower Gallium content, *i.e.* the built-in tunnel barrier is lower in this case. (c) Color plot of current I as a function of bias voltage V_{bias} and gate voltage V_{gate} (barrier gate and normal gate connected and act as a single local gate). (d) Representative WKB-model-fits of experimental I - V traces at four different values of gate voltage V_{gate} . Square-shaped barrier potential is used for the WKB-model-fits. (e) The

barrier height as a function of gate voltage, V_{gate} . The effective barrier height at 0 V corresponds to the actual conduction band offset between the InSb and $\text{Ga}_{0.15}\text{In}_{0.85}\text{Sb}$ nanowire segments and equals 75 meV. (f) The barrier width as a function of gate voltage, V_{gate} . The extracted barrier width is between 10 nm and 20 nm, which agrees with the value extracted from TEM/EDX.