Supplementary Information

Role of remote interfacial phonon (RIP) scattering in heat transport across graphene/SiO_2 interfaces

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S1. Fabrication process

Dual-gated graphene field-effect transistors were prepared by nano-fabrication processes as shown in Supplementary Fig. 1.

(a) Graphene flakes were mechanically exfoliated on a SiO_2/Si substrate and a graphene flake is located by an optical microscope.

(b) A PMMA (Polymethyl methacrylate) layer was coated on the substrate at 6000 rpm and baked at 200 ^{o}C for 2 minutes. Two regions of the selected graphene were exposed to the air after e-beam lithography and development processes.

(c) Ti (10 nm) and Au (40 nm) were successively deposited by a thermal e-beam evaporation.

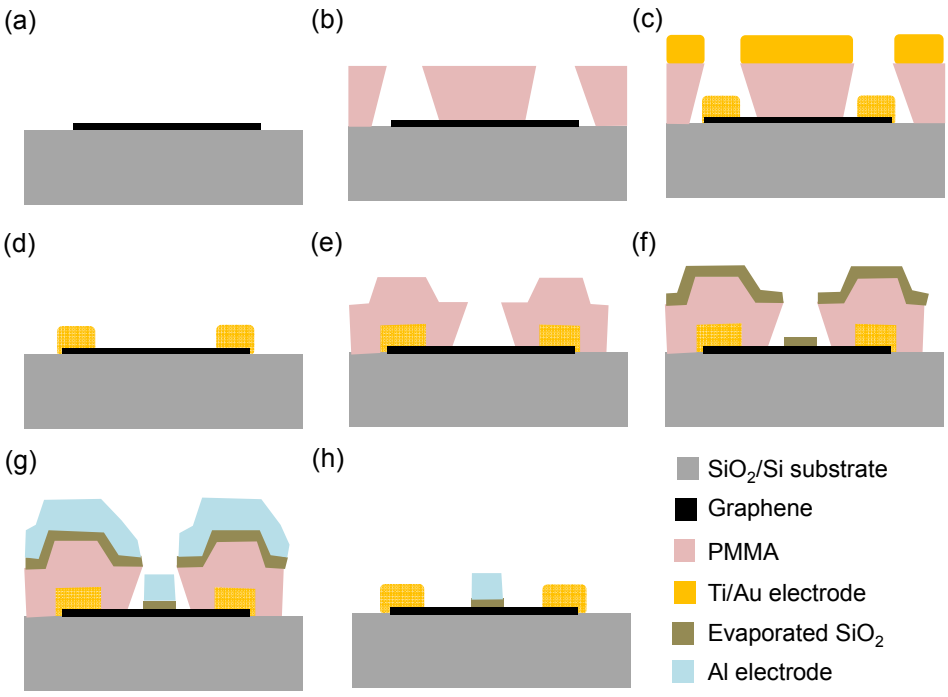
(d) A lift-off process with acetone left a graphene with source and drain electrodes.

(e) With the same recipe of (b) for the PMMA coating and e-beam lithography process, a region between the source and drain was developed.

(f) SiO_2 (~24 nm) was thermally evaporated by an e-beam evaporator at ~8 × 10^{-7} Torr.

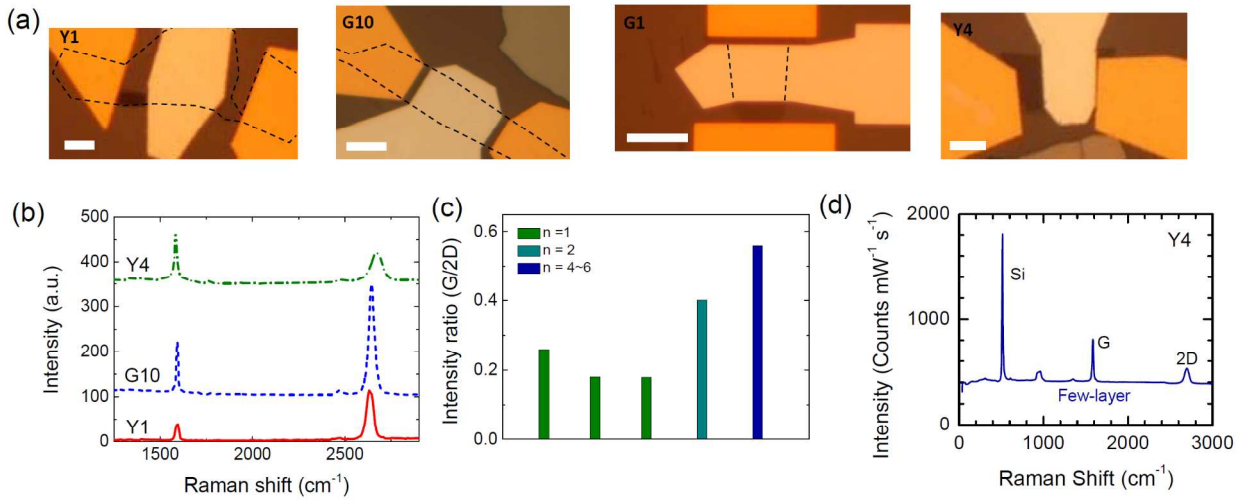
(g) After transferring the substrate to another e-beam evaporator, a Al (90 nm) were deposited.

(h) After a lift-off process in acetone, a top-gated graphene field-effect transistor was completed.



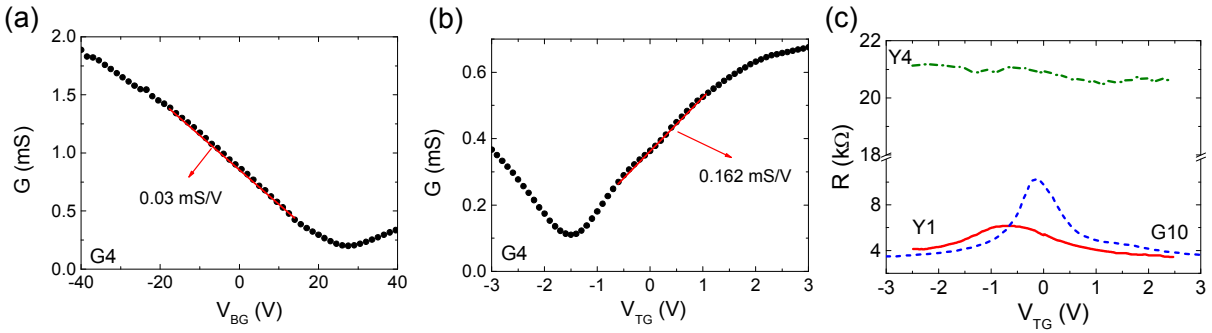
Supplementary Fig. S1 Schematic of fabrication process of a graphene dual-gated field-effect transistor.

S2. Sample images and Raman spectra



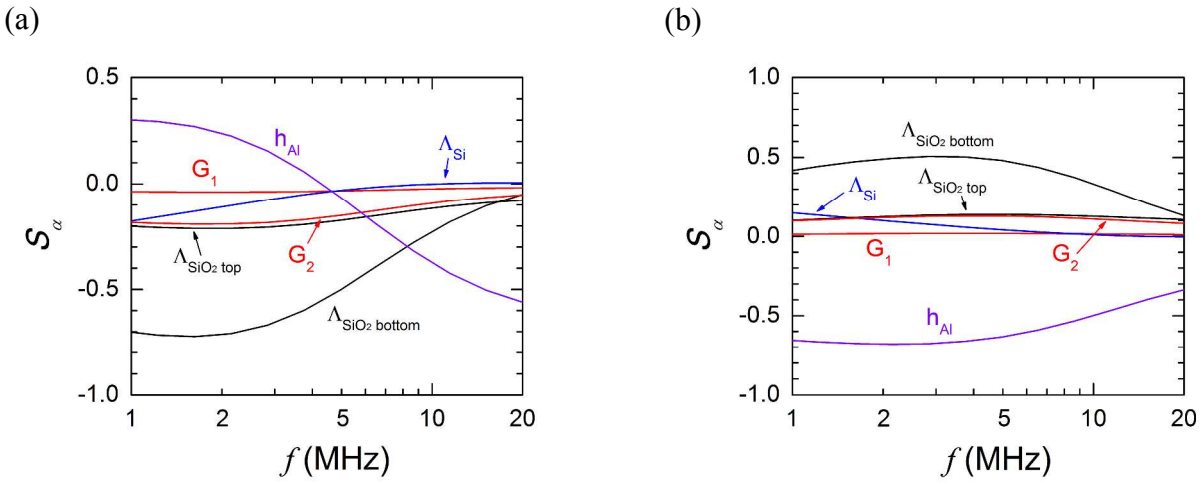
Supplementary Fig. S2 (a) Optical microscope images of samples, Y1, G10, G1 and Y4. Scale bar are 10 μm. (b) Raman spectra of Y1, G10 and Y4. (c) Intensity ratio of G and 2D peak (G/2D) of G4, Y1, G10, G1 and Y4. In Ref. [S1], it has been shown that the G/2D intensity ratio gives the number of graphene layer (n): 0.2~0.3, 0.35~0.41, 0.45~0.55, 0.53~0.71 and 0.6~0.8 for n = 1, 2, 3, 4 and 6, respectively. Following this report, we assigned n as shown in the figure. (d) Raman spectrum of Y4. For the sample Y4, the intensity ratio of G and Si peaks, 0.49 was additionally considered and we confirmed n = 6 for Y4 [2].

S3. Electrical characterization



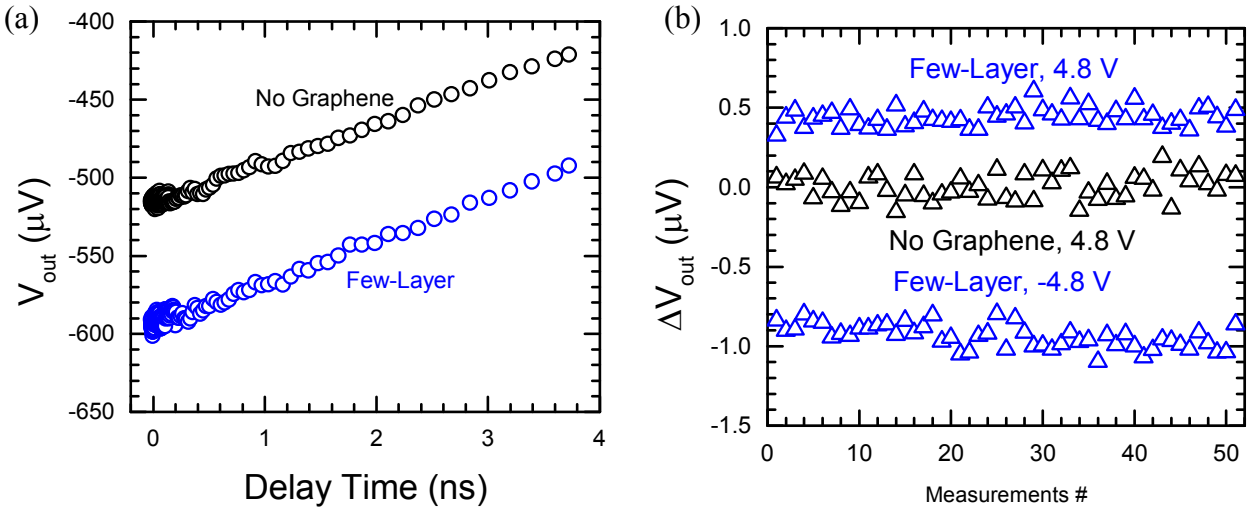
Supplementary Fig. S3 Electrical conductance as a function of (a) back-gate voltage (G-V_{BG}) and (b) top-gate voltage (G-V_{TG}) of G4. Here G-V_{BG} was obtained before defining the top gate. We estimated a low-field mobility from the transfer curve based on a relation of $\boldsymbol{\mu = \frac{L}{W}\frac{1}{C_{ox}}\frac{dG}{dV_G}}$, where C_{ox} is the gate capacitance per unit area and V_G is the gate voltage. The back-gate channel length is L_{BG} = 33.7 μm, top-gate channel length, L_{TG} = 25 μm and channel width, W = 14 μm. With slopes of linear regions in the transfer curves of (a) and (b), indicated by red solid lines, we get mobility of μ_{BG} = 1820 $cm^2V^{-1}S^{-1}$ and μ_{TG} = 1950 $cm^2V^{-1}S^{-1}$, respectively. Here, we used the dielectric constant for both of back- and top-gate SiO_2 layers as 3.9. Since the both mobility for the back- and top-gate effect is the similar value with the same dielectric constant, we confirmed that the thermally evaporated 24 nm thick top-SiO_2 shows the dielectric constant as ~3.9 as a usual value. (c) Resistance vs. top-gate voltage (R-V_{TG}) curves for Y1, G10 and Y4.

S4. Sensitivity plots



Supplementary Fig. S4 (a) Sensitivity of V_{out} signals and (b) V_{in}/V_{out} signals to various parameters used in the thermal model, as a function of modulation frequency f. We used the structure of sample G1 for the calculation, which is a multilayered structure consisting of 84 nm Al / 25 nm SiO_2 / exfoliated graphene / 90 nm SiO_2 / Si substrate. The parameters are thermal conductance of Al/SiO_2 interface G_1, thermal conductance of SiO_2/G/SiO_2 interface G_2, thermal conductivity of Si substrate Λ_{Si}, thermal conductivity of top SiO_2 layer $\Lambda_{SiO2\ top}$, thermal conductivity of bottom SiO_2 layer $\Lambda_{SiO2\ bottom}$ and thickness of Al Λ_{Al}. We fix the delay time at -40 ps and 100 ps for (a) and (b) respectively and assume a laser spot $1/e^2$ radii of 4 μm. As illustrated in the figures, we choose to use V_{out} and $f \approx 10$ MHz in our VMTR measurements, to achieve the highest sensitivity to G_2 and lowest sensitivity to other parameters.

S5. Comparison of raw data of TDTR and VMTR



Supplementary Fig. S5 (a) Out-of-phase components of TDTR measurements (V_{out}) on the few-layer graphene sample and a region without graphene on a sample, as labeled. In these measurements, we used a modulation frequency of 10 MHz, a total laser power of ~62 mW and laser spot sizes of ~4 μm. The noise, usually on the order of 2% of the signals (~10 μV), originates from the noise in laser intensity, the variation of phase in the rf lock-in amplifier, etc. From measurements to measurements, the precision of TDTR measurements is on the order of 1% (~5 μV), usually limited by phrase drift in the rf lock-in amplifier. (b) VMTR measurements on the same sample as in (a), using the same laser power and laser spot size as in (a). The "on"-state gate voltages that we applied are as labeled. By averaging 40-100 VMTR measurements as in the figure, we are able to reduce the uncertainty of VMTR measurements to ~0.012 μV, more than 100 times better than the uncertainty of TDTR measurements.

References for Supplementary information

[1] D. Graf et al., Nano Letters **7**, 238 (2007)

[2] Y.K. Koh, M.-H. Bae, D.G. Cahill, E. Pop, ACS Nano **5**, 269 (2011).