Supporting Information

Flexible Opto-fluidic Fluorescence Sensors Based on Heterogeneously Integrated Micro-VCSELs and Silicon Photodiodes

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1. Supplementary Methods

1.1. Processing scheme for releasable micro-VCSELs

Top contact (p^+) metallization

1. Clean a 12 x 12-mm^2 piece of 850 nm VCSEL source wafer with acetone, isopropyl alcohol (IPA), and deinoized (DI) water.
2. Dehydrate at 110^{o}C for 10 min.
3. Spin-coat photoresist (PR; AZ5214 (Clariant); 500 rpm/5 s, 3000 rpm/30 s) and soft-bake PR at 110^{o}C for 1 min.
4. Expose PR with i-line (365 nm, 80 mJ/cm^2) mask aligner (Karl Suss MJB3).
5. Develop PR in tetramethyl ammonium hydroxide (TMAH)-based developer (AZ300MIF (Clariant) for 40 s.
6. Descum the exposed GaAs top contact layer by oxygen reactive-ion etching (O_2-RIE; Plasmalab; 10 W, 100 mTorr, 1 min).
7. Remove a native oxide layer in a diluted HCl solution (HCl (38 wt%, EMD):DI water = 1:1, by volume) for 1 min.
8. Deposit Pt (10 nm)/Ti (40 nm)/Pt (10 nm)/Au (80 nm) by electron beam evaporation (Temescal).
9. Lift-off PR in warm acetone for 1 hr.

Top-mesa etching

10. Clean the processed wafer in step 9 using acetone, IPA, and DI water.
11. Deposit Si_3N_4 (~1.3 μm) by plasma-enhanced chemical vapor deposition (PECVD; Plasmalab; SiH_4: NH_3: N_2 = 40: 20: 60 in standard cubic centimeters (sccm), 500 mTorr, 38 W, 300^{o}C).
12. Clean the sample using acetone, IPA, and DI water and dehydrate at 110^{o}C for 5 min.

13. Treat hexamethyldisilazane (HMDS (98%, Acros Organics)) for 5 min as an adhesion promoter and pattern PR (AZ5214) (step 3 - 5).
14. Etch Si_3N_4 using CF_4/O_2-RIE (CF_4/O_2 =50.9/5.1 in a. u., 100 mTorr, 100 W) until the GaAs contact layer is exposed.
15. Strip PR with acetone.
16. Descum the exposed surface of GaAs contact layer by oxygen reactive-ion etching (O_2-RIE; Plasmalab; 100 W, 100 mTorr, 1 min).
17. Etch top-mesa structure with inductively coupled plasma reactive ion etching (ICP-RIE; STS; BCl_3:N_2 = 1.5:9 in sccm, 5 mTorr, platen/coil = 100W/500W, 100ºC).

Wet oxidation for current confinement aperture

18. Load the processed wafer in step 17 into a furnace pre-heated at 430ºC for 50 min and filled with water steam vapor that is generated from a water bath heated at 90ºC and carried by 3.5 slpm of N_2 gas.
19. Strip remaining Si_3N_4 by CF_4/O_2-RIE for 1 min (step 14).

Bottom-contact (n^+) metallization

20. Clean the processed wafer in step 19 using acetone, IPA, and DI water and dehydrate at 110ºC for 5 min.
21. Treat HMDS for 10 min.
22. Spin-coat PR (AZ4620 (Clariant); 500 rpm/5 s, 3000 rpm/60 s).
23. Soft-bake at room temperature for 30 min and then at 110ºC for 5 min.
24. Expose PR with i-line (365 nm, 600 mJ/cm^2) mask aligner (Karl Suss MJB3).
25. Develop PR in aqueous base developer (AZ400K (Clariant):DI water = 1:4, by volume) for 4 min.
26. Post-bake PR at 110ºC for 5 min.
27. Etch an oxidized surface with developer (AZ400K:DI water = 1:4, by volume) for 5 min, followed by diluted NH_4OH solution (NH_4OH (28-30%, Fisher Scientific):DI = 1:10, by volume) for 1 min.
28. Etch a layer of $Al_{0.9}Ga_{0.1}As$ in diluted HF solution (HF (48%, EMD):DI = 1:10, by volume) for 20 s.

29. Etch a layer of $Al_{0.15}Ga_{0.85}As$ in a mixture of citric acid solution (100 g of citric acid monohydrate (Sigma-Aldrich) in 83 ml of DI water) and H_2O_2 (30%, Fisher Scientific) (20:1, by volume) for 2 min.
30. Etch a layer of $Al_{0.9}Ga_{0.1}As$ in diluted HF solution (HF:DI = 1:10, by volume) for 20 s.
31. Strip PR using acetone.
32. Clean the processed wafer in step 31 using acetone, IPA, and DI water and dehydrate at 110^{o}C for 5 min.
33. Pattern PR (AZ5214), descum, and remove an oxide layer (step 3-7).
34. Deposit AuGe (100 nm)/Ni (30 nm)/Au (100 nm) by electron beam evaporation.
35. Lift-off PR in warm acetone for 1 hr.
36. Anneal the sample at 400^{o}C for 1 min under H_2 (2%)/N_2 atmosphere by rapid thermal annealing.

Bottom-mesa etching

37. Clean the processed wafer in step 38 using acetone, IPA, and DI water.
38. Deposit Si_3N_4 (1.3 μm) by PECVD (step 11).
39. Clean the sample, treat HMDS, and pattern PR (AZ4620) (step 20 – 25).
40. Etch a Si_3N_4 mask, strip PR, and descum the exposed surface (step 14 - 16).
41. Etch bottom-mesa structure by ICP-RIE such that the etch stops at the base layer (step 17)
42. Strip Si_3N_4 by CF_4/O_2-RIE for 1 min (step 19).

Base-mesa and sacrificial layer partial etching

43. Clean the processed wafer in step 42 using acetone, IPA, and DI water and dehydrate at 110^{o}C for 5 min.
44. Treat HMDS and pattern PR (AZ4620) (step 21 - 26).
45. Remove oxide in a diluted HCl solution (HCl:DI water = 1:1, by volume) for 1 min.
46. Etch the base-mesa structure in a mixture of citric acid solution (step 29) and H_2O_2 (20:1, by volume) for 6 min.
47. Partially etch the $Al_{0.95}Ga_{0.05}As$ sacrificial layer in a diluted HF solution (HF:DI = 1:10, by volume) for 25 s.
48. Strip PR using acetone.

PR anchoring and undercut etching

49. Clean the processed wafer in step 48 using acetone, IPA, and DI water and dehydrate at 110^{o}C for 10 min.

50. Treat HMDS for 10 min.

51. Spin-coat PR (SPR 220-7 (Rohm and Hass), 500 rpm/5 s, 2000 rpm/60 s).

52. Soft-bake at room temperature for 30 min, at 90^{o}C for 5 min, and subsequently at 115^{o}C for 5 min.

53. Expose PR with i-line (365 nm, 650 mJ/cm^2) mask aligner (Karl Suss MJB3).

54. Develop PR in aqueous base developer (MF-24A (Microchem Corp.)) for 3 min.

55. Post-bake PR at 90^{o}C for 1 min and 110^{o}C for 3 min.

56. Remove oxide in a diluted HCl solution (HCl:DI water = 1:1, by volume) for 30 s.

57. Etch etch-holes through the base-mesa in a mixture of phosphoric acid, DI water and H_2O_2 (H_3PO_4 (85%, Fisher Scientific):DI water:H_2O_2 = 1:12:13, by volume) for 1 min.

58. Etch $Al_{0.95}Ga_{0.05}As$ sacrificial layer in a diluted HCl solution (HCl:DI = 3:1, by volume) for 70 min.

Preparation of featured elastomeric polydimethylsiloxane (PDMS) stamps

59. Clean a 10 x 10-mm^2 piece of Si (100) wafer with acetone, IPA, DI water, and then RCA1 solution (NH_4OH:H_2O_2:H_2O = 1:1:6, by volume, 75^{o}C) for 10 min, followed by strip of a natural oxide with buffered oxide etchant (BOE (6:1, Transene)).

60. Dehydrate at 200^{o}C for 5 min.

61. Spin-coat PR (SU-8 50 (Microchem Corp.); 500 rpm/5 s, 2000 rpm/30 s).

62. Soft-bake at room temperature for 30 min, at 65^{o}C for 80 min, and then at 95^{o}C for 110 min.

63. Expose PR with i-line (365 nm, 360 mJ/cm^2) mask aligner (Karl Suss MJB3).

64. Post-exposure-bake (PEB) PR at 65^{o}C for 1 min and 95^{o}C for 7 min.

65. Develop PR in SU-8 developer (Microchem Corp.) for 9 min.

66. Hard-bake PR at 150^{o}C for 1 hr.

67. Clean the prepared mold in step 66 with acetone, IPA, and DI water and dehydrate at 110^{o}C for 10 min.

68. Treat under the atmosphere of tridecafluoroctyltrichlorosilane (United Chemical Technology) for 30 min.

69. Cast PDMS pre-polymer (Sylgard 184, Dow Corning; pre-polymer:curing agent = 10:1, by weight).

70. Cure PDMS pre-polymer at room temperature for 1 day and at 65^{o}C for 1 hr.

71. Slowly peel cured PDMS off from the mold

1.2. Processing scheme for thin (~3 μm) silicon photodetectors

n^{+}-doping

1. Clean a silicon-on-insulator (SOI) wafer (3 μm-thick top Si on 1 μm-thick buried SiO_2, n-type, 1-10 Ω·cm, Soitec) with RCA1 cleaning ($NH_4OH:H_2O_2:H_2O$ = 1:1:6, by volume, 75^{o}C) for 10 min, followed by strip of natural oxide with buffered oxide etchant (BOE, 6:1, Transene).

2. Deposit Si_3N_4 (0.6 μm) by plasma-enhanced chemical vapor deposition (PECVD, Plasmalab) (SiH_4: NH_3: N_2 = 15: 45: 60 in sccm, 500 mTorr, 38 W, 275^{o}C).

3. Clean by RCA1 and dehydrate at 200° C for 5 min.

4. Spin-coat PR (AZ5214, 3000 rpm/30 s) and soft-bake at 110° C for 1 min.

7. Expose PR with i-line (365 nm, 80 mJ/cm^2) mask aligner (Karl Suss MJB3).

8. Develop PR in aqueous base developer (AZ400K:DI water = 1:4, by volume).

9. Post-bake PR at 110° C for 3 min.

10. Etch a Si_3N_4 layer using BOE (6:1) for 3 min.

11. Remove PR with acetone and clean by RCA1 for 10 min.

12. Dope the exposed Si with a solid-state phosphorous source (PH-1000N, Saint Gobain) in N_2 atmosphere at 1000^{o}C for 10 min.

13. Clean the doped wafer with HF, RCA1, and BOE.

p^{+}-doping

14. Deposit Si_3N_4 (0.6 μm) by PECVD (step 2).

15. Open the doping window for p^{+}-doping (step 3-11).

16. Dope the exposed Si with a solid-state boron source (BN-1250, Saint Gobain) in N_2 atmosphere at 1000^{o}C for 10 min.

17. Clean the doped wafer with HF, RCA1, and BOE.

Isolation and partial etching

18. Clean by RCA1 and dehydrate at 200° C for 5 min.

19. Pattern PR (AZ5214) for isolation (step4-9).

20. Etch the exposed Si with BOE (6:1) for 30 s.

21. Etch Si by ICP-RIE (Plasmalab system 100, Oxford) (Bosch process: 15 loops of etch (SF_6: 100 sccm, 30 mTorr, 5 s, RF/ICP = 40W/700W) and passivation (C_4F_8: 100 sccm, 30 mTorr, 7 s, RF/ICP = 10W/700W)).

22. Etch the buried oxide layer for 5 min in HF (49%, J.T. Baker).

23. Remove PR with acetone and clean by RCA1 for 10 min.

Undercut etching

24. Pattern PR (AZ5214) to define etch holes (step 4-9).

25. Etch Si by ICP-RIE (step 21).

26. Etch buried SiO_2 in HF for 90 min.

1.3. Processing scheme for flexible fluorescence sensors

Metal reflector deposition for photodetectors

1. Clean a PET (~50 μm) substrate by acetone, IPA, and DI water, followed by drying with N_2.

2. Spin-coat PR (AZnLOF 2070 (Clariant); 500 rpm/5 s, 4000 rpm/30 s).

3. Soft-bake PR at 100°C for 7 min.

4. Expose PR with i-line (365 nm, 360 mJ/cm^2) mask aligner (Karl Suss MJB3).

5. PEB PR at 110°C for 45 s.

6. Develop PR in aqueous base developer (AZ300 MIF, Clariant) for 1 min.

7. Deposit Cr (30 nm)/Au (70 nm) using an electron beam evaporation system (Temescal).

8. Remove PR using acetone, IPA, and DI water.

Metal heat sink deposition for micro-VCSELs

9. Clean the processed substrate in step 8 using acetone, IPA, and DI water.

10. Pattern PR (AZnLOF 2070) and deposit Cr (15 nm)/Ag (3000 nm)/Au (50 nm) (step 2 - 8).

Printing onto a PET substrate

11. Clean the processed substrate in step 10 using acetone, IPA, and DI water.

12. Spin-coat a UV curable adhesive (2000 rpm/30 s) and bake at 110˚C for 90 s.

13. Pick-up completed, print-ready silicon photodetector arrays using a flat PDMS stamp.

14. Print retrieved silicon photodetector arrays onto the PET substrate in step 2.

15. Pick-up and print an individual micro-VCSEL from the source wafer using a PDMS stamp with a relief feature (300 x 300 μm^2) using a mask aligner (Karl Suss MJB3).

16. Expose the backside of the sample with i-line (100 mJ/cm^2).

17. Bake at 110^oC for 30 min.

18. Remove PR with acetone, IPA, and DI water.

19. Remove the exposed adhesive using oxygen reactive-ion etching (O_2-RIE, Plasmalab) (100 W, 100 mTorr, 3 min).

Dielectric layer deposition for anti-reflection

20. Clean the processed substrate in step 19 using acetone, IPA, and DI water.

21. Pattern PR (AZnLOF 2070) (step 2 - 8).

22. Deposit TiO_2 (90 nm) using a RF sputtering system (AJA Orion5, Ar: 15.0 sccm, 3 mTorr, 100W).

23. Remove PR with acetone, IPA, and DI water.

Interconnection and encapsulation of flexible fluorescence sensors

24. Clean the processed sample in step 23 using acetone, IPA, and DI water and dehydrate at 110^oC for 5 min.

25. Treat UV ozone (UVO) for 10 min.

26. Spin-coat PR (SU-8 2005 (Microchem Corp.); 600 rpm/5 s, 3000 rpm/30 s).

27. Prebake PR at 95^oC for 3 min.

28. Expose PR with i-line (365 nm, 140 mJ/cm^2) mask aligner (Karl Suss MJB3).

29. PEB PR at 95^oC for 2 min 30 s.

30. Develop PR in SU-8 developer (Microchem Corp.) for 100 s.

31. Hard-bake PR at 110^oC for 1 h.

32. Treat UV ozone (UVO) for 10 min.

33. Spin-coat PR (SU-8 2 (Microchem Corp.); 600 rpm/5 s, 3000 rpm/30 s).

34. Prebake PR at 65^oC for 1 min and then 95^oC for 1 min.

35. Expose PR with i-line (365 nm, 80 mJ/cm^2) mask aligner (Karl Suss MJB3).
36. PEB PR at 65^{o}C for 1 min and then 95^{o}C for 1 min.
37. Develop PR in SU-8 developer (Microchem Corp.) for 30 s.
38. Hard-bake PR at 110^{o}C for 1 h.
39. Expose PR with a UV lamp (B-100SP, UVP) for 10 min.
40. Hard-bake PR at 110^{o}C for 1 h.
41. Clean the sample using acetone, IPA, and DI water and dehydrate at 110^{o}C for 10 min.
42. Treat HMDS for 10 min.
43. Pattern PR (AZnLOF 2070) and deposit Cr (15 nm)/Ag (1500 nm)/Au (30 nm) for interconnection (step 2 - 8).
44. Pattern PR (SU-8 2005 and 2) for encapsulation (step 24 - 40).

Dielectric layer depositions for optical filter

45. Clean the processed sample in step 23 using acetone, IPA, and DI water and dehydrate at 110^{o}C for 5 min.
46. Deposit TiO_2 (46 nm)/[SiO_2 (150 nm)/TiO_2 (92 nm)]^3/SiO_2 (150 nm)/TiO_2 (46 nm) using a RF sputtering system (AJA Orion5, Ar: 15.0 sccm, 3 mTorr, 100W for TiO_2 and 200W for SiO_2).
47. Treat HMDS for 10 min.
48. Spin-coat PR (AZ4620 (Clariant); 500 rpm/5 s, 3000 rpm/60 s).
49. Soft-bake at room temperature for 30 min and then at 110^{o}C for 5 min.
50. Expose PR with i-line (365 nm, 600 mJ/cm^2) mask aligner (Karl Suss MJB3).
51. Develop PR in aqueous base developer (AZ400K (Clariant):DI water = 1:4, by volume) for 4 min.
52. Etch the exposed optical filter with diluted HF solution (HF:DI = 1:10, by volume) for 90 s.
53. Remove PR with acetone, IPA, and DI water.

Metal deposition for optical isolation

54. Clean the processed substrate in step 53 using acetone, IPA, and DI water.
55. Pattern PR (AZnLOF 2070) and deposit Cr (150 nm) for optical isolation (step 2 - 8).

1.4. Processing scheme for PDMS fluidic channel

1. Clean a 3D-printed plastic mold (Proto labs) with acetone, IPA, and DI water, followed by drying with N_2.
2. Treat under the atmosphere of tridecafluoroctyltrichlorosilane (United Chemical Technology) for 30 min.
3. Cast PDMS pre-polymer (Sylgard 184, Dow Corning; pre-polymer:curing agent = 10:1, by weight).
4. Cure PDMS pre-polymer at room temperature for 1 day and at 65^{o}C for 1 hr.
5. Slowly peel cured PDMS off from the mold.

2. Supplementary Figures and Legends

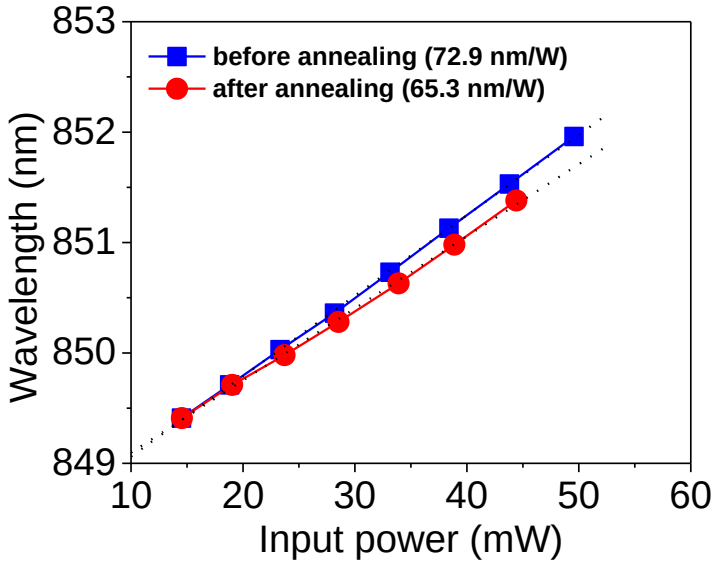

Figure S1. The spectral shift of lasing modes in the 850 nm micro-VCSEL with an aperture area of 22 x 22 μm^2 as a function of input power before (blue diamond) and after (red circle) the thermal annealing (150^{o}C, 1.5 h), where micro-VCSELs were printed on silicon using a photo-curable adhesive (thickness: ~1 μm). The lower slope of the spectral shift after the thermal annealing implies thermal resistance (K/W) of printed micro-VCSEL was reduced due to the evaporation of residual solvent in the adhesive layer and resultant increase of thermal conductivity.

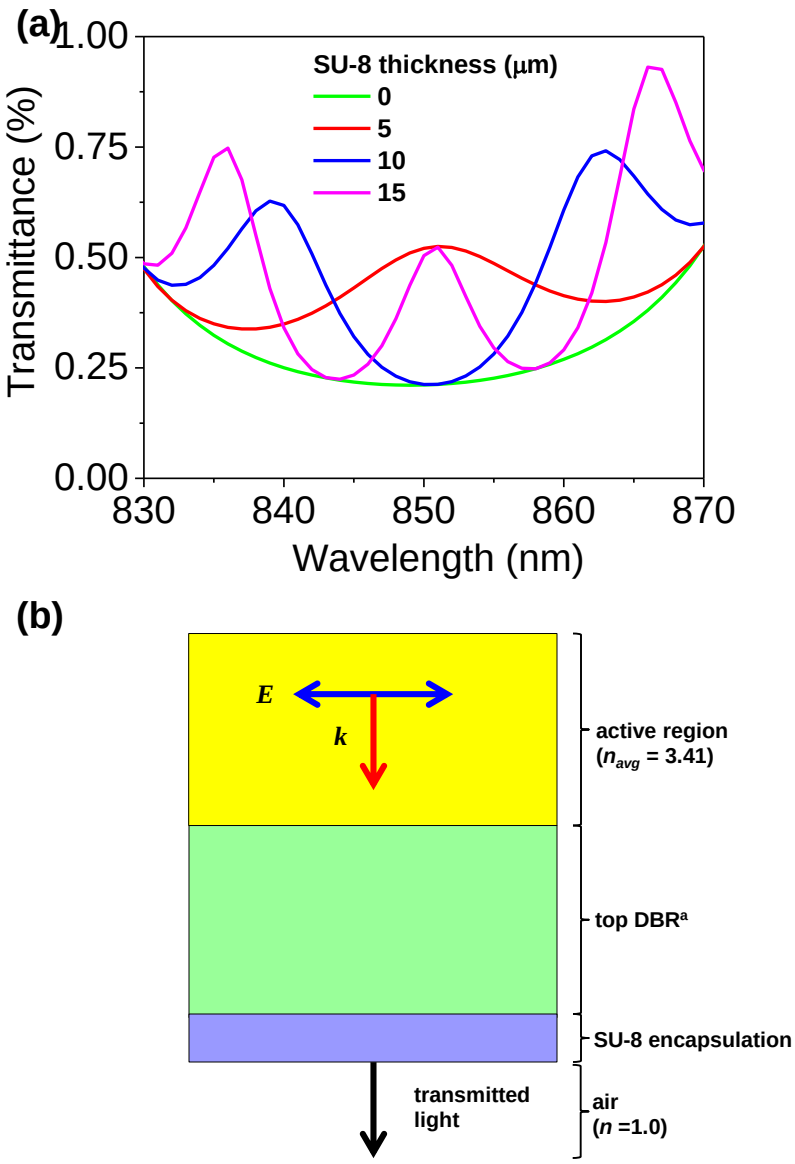

Figure S2. (a) Calculated normal-incidence transmittance spectra of the top distributed Braggs reflector (DBR) of micro-VCSELs at various thicknesses of SU-8 encapsulation layer that cover the top surface of the laser aperture, where the light (i.e. laser output) is assumed to be incident from the active region (n = 3.41) to the top DBR of the micro-VCSEL. **(b)** Schematic illustration of simulated system. [a]Detailed epitaxial design of the top DBR is available in our previous publication (*Advanced Optical Materials*, **2**, 373, (2014)).

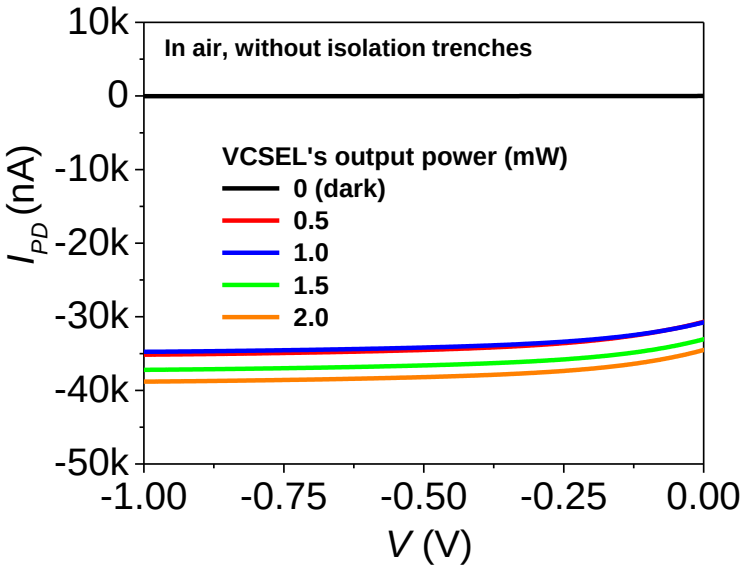

Figure S3. Current (*I*)-voltage (*V*) curves of a printed Si-PD on silicon at various output power levels of the co-integrated micro-VCSEL, measured in air without the implementation of optical isolation trenches.

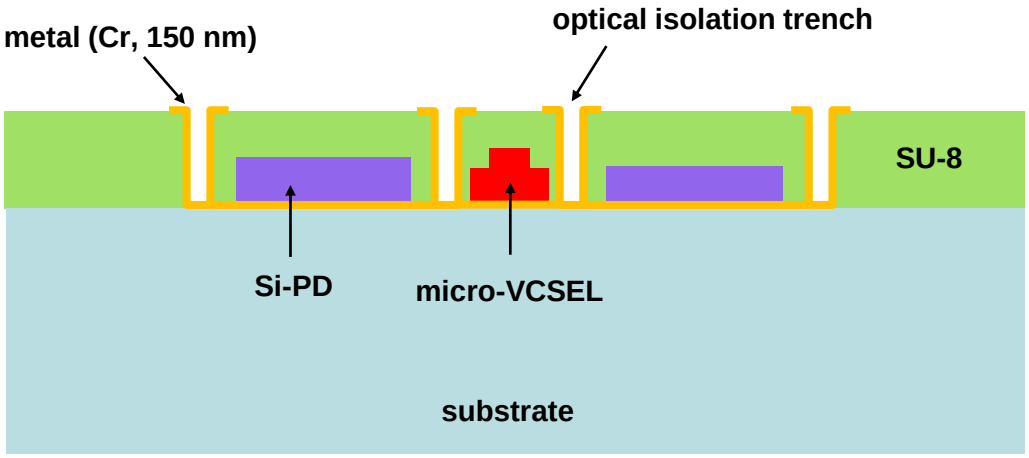

Figure S4. A cross-sectional schematic illustration of an integrated sensor assembly based on printed micro-VCSEL and Si-PD, where metal-deposited optical isolation trenches were implemented to minimize wave-guided spontaneous emission from the VCSEL to the PD and therefore enhance the signal-to-noise ratio.

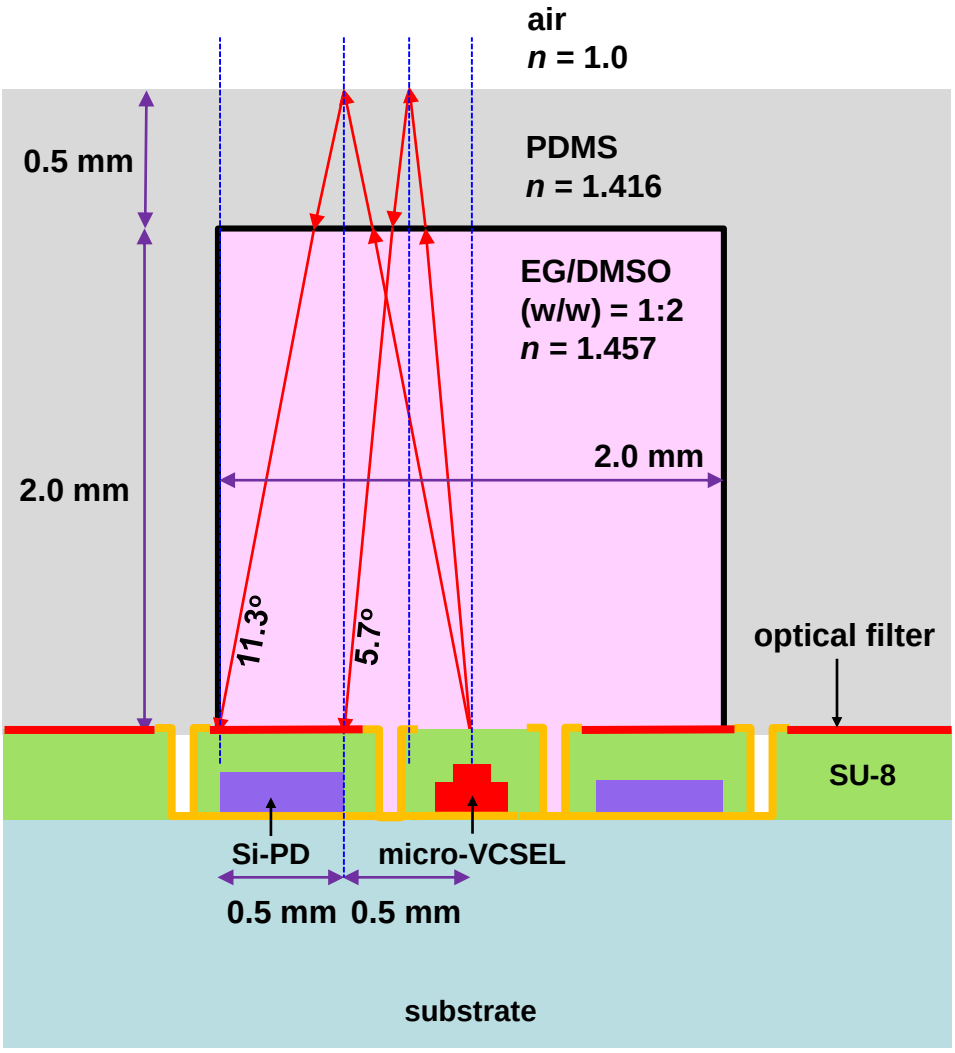

Figure S5. A cross-sectional schematic of opto-fluidic fluorescence sensor monolithically integrated with a PDMS-based fluidic channel. It is shown that some fraction of the stimulated emission from the VCSEL is reflected at the inner and outer wall of PDMS channel and directed back to the adjacent Si-PD at an incidence angle less than ~12º.

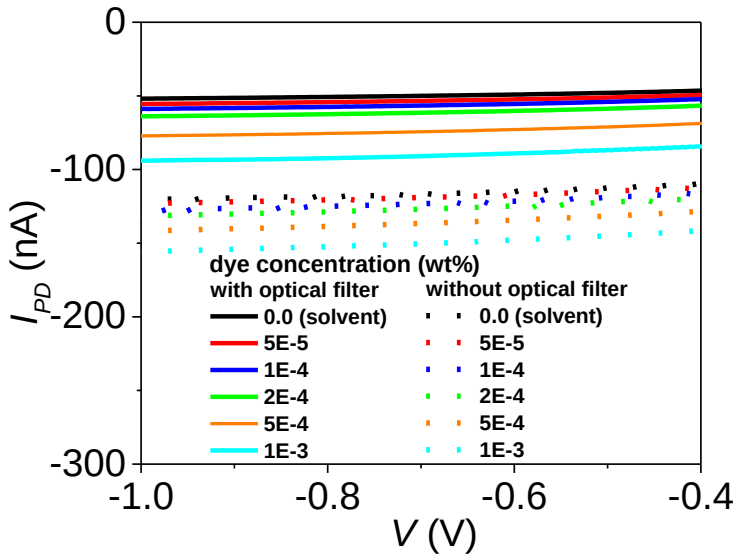

Figure S6. *I-V* curves of Si-PDs in the opto-fluidic fluorescence sensor measured at various dye concentrations under a fixed output power (~2 mW) of the micro- VCSEL with and without optical filter, where dye solutions were flown through the fluidic channel at a flow rate of ~13.3 ml/h.

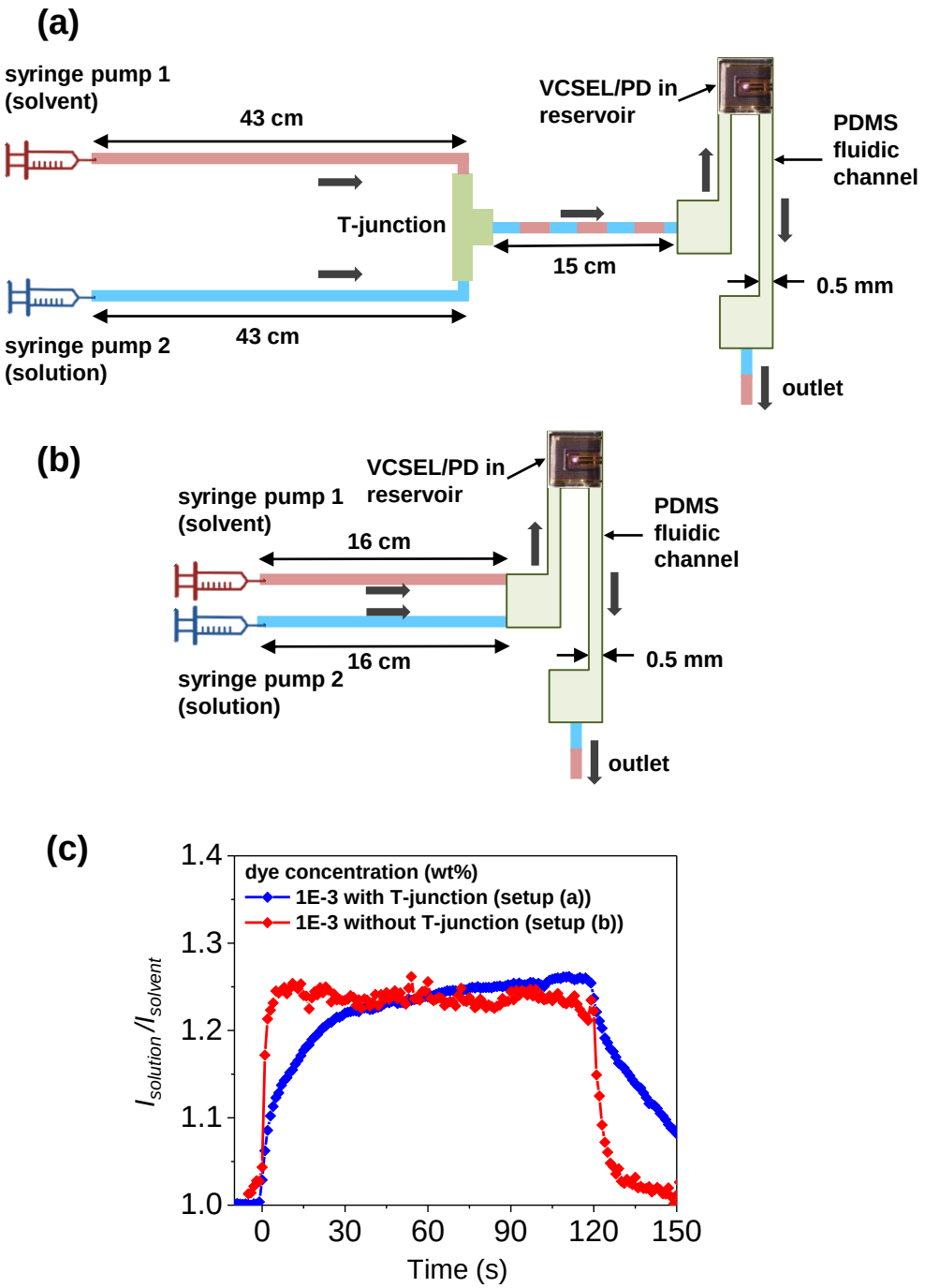

Figure S7. Schematic illustrations of the experimental setups for opto-fluidic measurements (a) with and (b) without a T-junction, where the inner diameter of the tube is 0.89 mm. (c) Continuous, real-time measurement of $I_{solution}/I_{solvent}$ using the above two different experimental setups at the dye concentrations of 1.0 x 10^{-3} wt%, where the solution and solvent were sequentially injected every two minutes with the flow rate of ~13.3 ml/hr. During the measurements, the optical power of micro-VCSEL and the applied voltage of Si-PD were fixed at 2.0 mW and -1.0 V, respectively.

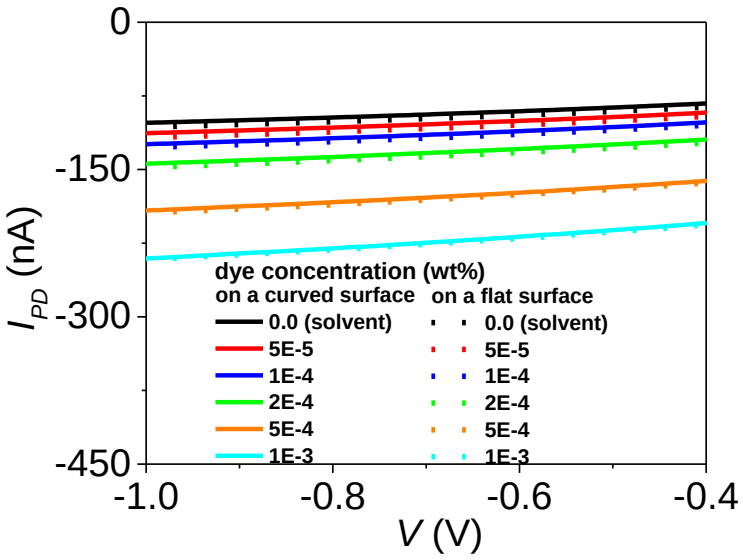

Figure S8. *I-V* curves of a Si-PD in the flexible opto-fluidic fluorescence sensor obtained at various dye concentrations under a fixed output power (~2 mW) of the micro- VCSEL on a curved surface (R = 50 mm) as well as on a flat surface (R = ∞), where the dye solution was injected through the fluidic channel at a flow rate of ~13.3 ml/h.