Supporting Information

An organic/Si nanowire hybrid field configurable transistor

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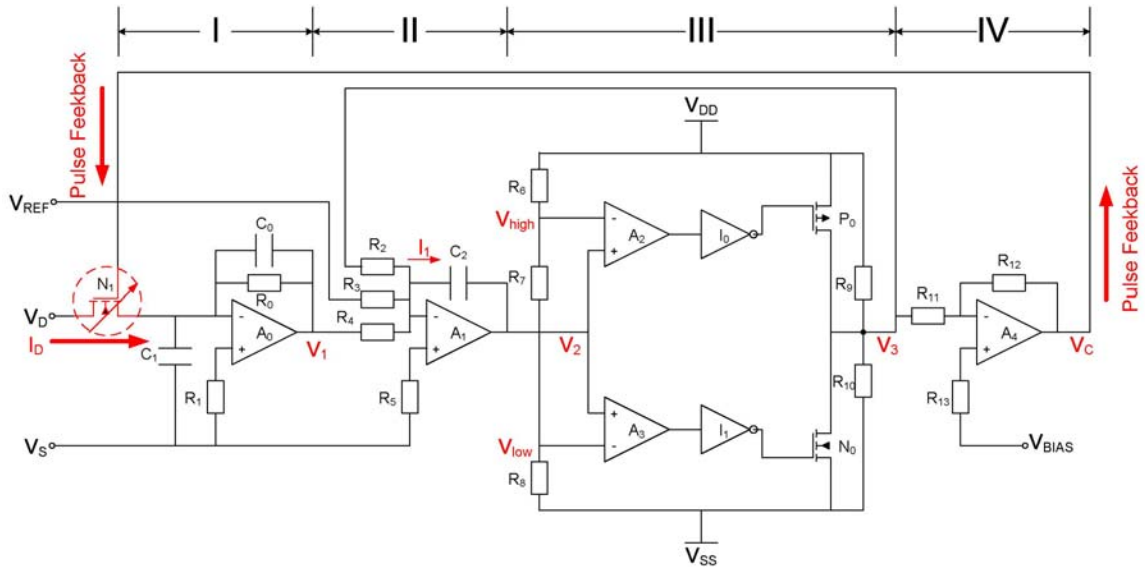
Contents

A. Closed-loop feedback circuit for targeted configuration

In order to precisely program a FCT to an arbitrary targeted value, we designed an analog circuit with a closed-loop feedback mechanism. As shown in Supplementary Figure 1, the circuit consists of four submodules: (I) Current sampling and filtering, (II) Comparison and arbitration, (III) Oscillation and pulse generation, (IV) Amplitude adjustment and feedback. In submodule I, the DC component of the source-drain current I_d of the FCT (marked by the red circle in Supplementary Figure 1) was sampled continuously and converted to a voltage signal V_1 by an integrator composed of an operational amplifier (op-amp), A_0, two resistors, R_0, R_1, and a capacitor, C_0, while the high-frequency noise and transients were filtered by the capacitor C_1. In submodule II, the voltage signal V_1 was compared with a reference voltage, V_{Ref}, which defined the targeted current, I_{Ref}. Because of the "virtual short circuit" effect of the op-amp, A_1, the voltage difference, V_{Ref} - V_1, was converted back to a current $I_1=\left(V_{Ref}-V_1\right)/R$, where $R_3 = R_4 = R$. The op-amp, A_1 and the capacitor C_2 served as an integrator that generated a voltage $V_2(t)=V_2(0)+\left(V_{Ref}-V_1\right)t/C_2R$. Submodule III was basically a sawtooth oscillator. When V_2 was higher (or lower) than the two reference voltages V_{high} and V_{low} provided by the resistors R_6, R_7, and R_8 in series, the transistor P_0 (or N_0) was turned on, and a positive (or negative) pulse V_3 was generated, which recharged capacitor C_2 with the opposite polarity and switched P_0 (or N_0) back to the off state. I_1 was integrated by C_2 again, thus generating the sawtooth waveform V_2 and a positive (or negative) pulse V_3. By adjusting the feedback resistor R_2, the pulse duration was tuned to an optimal value. In submodule IV, the positive (or negative) pulse V_3 generated in submodule III was inverted and amplified to V_C with a rail-to-rail amplitude and applied to the FCT gate to

configure the FCT.

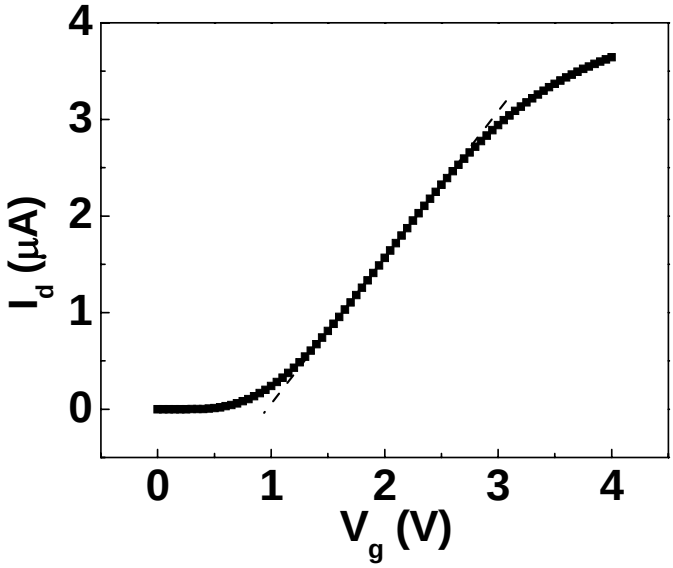
This circuit enabled the reading, comparison, and configuration processes to occur continuously. If I_d was higher (or lower) than I_{Ref}, negative (or positive) configuration voltage pulses, V_g, were applied to the FCT gate to decrease (or increase) I_d, while filtering out the high-frequency current transients. The frequency of pulses was proportional to $|I_{Ref} - I_d|$, so at the beginning of a configuration cycle, I_d was quickly programmed toward the targeted I_{Ref},; the rate gradually decreased as I_d approached I_{Ref}. When I_d reached I_{Ref}, the configuration pulses were halted.



Supplementary Figure 1. The closed-loop circuit used for the targeted configuration of a field configurable transistor.

B. Characteristics of a Si field effect transistor as control

Conventional Si field effect transistors (FETs) (without the $RbAg_4I_5$/MEH-PPV bilayer in the FCT gate shown in Figure. 1a in the paper) were tested as control devices for comparison with the FCT. These FETs had a simple Al/Ti/ SiO_2/p-Si gate structure and were fabricated by using the same process as described for the FCT in the paper except the steps to integrate the $RbAg_4I_5$/MEH-PPV bilayer were omitted. A typical source-drain current (I_d) of an FET measured at a source-drain voltage V_d = 1 V is shown in Supplementary Figure 2 as a function of gate-source voltage (V_g). No hysteresis loop was observed in the I_d–V_g curve. The threshold voltage of the FET is $V_T \approx 1.0$ V.



Supplementary Figure 2. The source-drain current I_d as a function of the gate-source voltage V_g measured in a Si field effect transistor as a control device. The intercept of the dashed straight line tangent to the I_d–V_g curve with the V_g axis determined the transistor threshold voltage to be $V_T \approx 1.0$ V.