Supporting Information for "Minimum Voltage for Threshold Switching in Nanoscale Phase-Change Memory"

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DEVICE FABRICATION

The GeTe (Sb_2Te_3) NWs were suspended in isopropanol (methanol) by sonication, and this solution was deposited on a Si/SiO_2 substrate with a pre-patterned grid. Electron beam lithography was used to define electrical leads to the individual NWs. To make ohmic contacts to the NWs, the chip was cleaned in an Ar plasma, and Cr (50 nm) and Au (150 nm) layers were deposited by sputtering, followed by liftoff. The devices were imaged using SEM at 2-5 kV and then were coated with a protective layer of silicon dioxide or nitride using electron beam evaporation (some devices were left uncovered to test the stability and strain effects). For the GeTe (Sb_2Te_3) NWs, the distance between the electrodes along the NWs ranged from 100 (175) nm to 10 (2) μm, and the diameters of the NWs in measured devices ranged from 30 (45) to 120 (226) nm.

ELECTRICAL CHARACTERIZATION

The temporal response of GeTe and Sb_2Te_3 NW devices to voltage pulses was measured in a probe station equipped with RF probes (Desert Cryogenics TTP4 with ZN50R probes). The voltage pulses were provided by a pulse generator (Stanford Research System Model DG535), and voltage and current time traces were recorded by a digital oscilloscope (Tektronix TDS2022). Figure 1c shows a diagram of the measurement circuit. Both channels of the digital oscilloscope (labeled by Ch1 & Ch2) had a 1 MΩ input impedance. The voltage applied to the devices was measured by Ch1, and the current was obtained by dividing the voltage of Ch2 by the 50 Ω resistance. The pulse generator (labeled by PG) was set at high output impedance for best performance.

KPM MEASUREMENTS

Kelvin probe microscopy enables the determination of local surface potential in NW devices. A commercial AFM (MultiMode, Nanoscope IV, Veeco Instruments) was used for non-contact KPM measurements. A conducting silicon tip ($\rho \sim 0.02$ Ω·cm) was scanned 50 nm above the oxide surface (90 nm above the NW), following the contour of the sample, while the bias across a single GeTe-NW device was held at 1 V. The lateral distance measured by KPM appears much larger than the actual value, since the resolution of the technique is limited by the finite scanning probe size and the height of the probe above the sample.

SIMULATION FOR LOAD RESISTANCE SCALING

Both analytical calculations and numerical simulations were performed for a cylindrical phase-change memory cell with length L and radius r with metal electrodes at both ends (Fig. 5a inset). The load resistance, R_L, was calculated analytically by solving a simplified one-dimensional thermal transport equation $-\kappa \frac{d^2T}{dx^2} = Q$, where Q is current-induced heat load ($Q = I^2\rho/(\pi r^2)^2$), and κ and ρ represent the thermal conductivity and the electrical resistivity of the phase-change material. During the SET process, ρ should be the resistivity of the crystalline phase because of the immediate threshold switching, while κ should be closer to the thermal conductivity of the amorphous phase since the thermal transport properties are most likely determined by the material structure, which changes much more slowly. Assuming the metal contact is at room temperature, a steady state solution to this equation is given by $I = 2\pi\sqrt{\frac{2\kappa\Delta T}{\rho}}\frac{r^2}{L} \equiv A\frac{r^2}{L}$, where ΔT is the difference between room temperature and the temperature at the center of the PCM device. ΔT must be between T_g and the melting point (T_m) of the phase-change materials. When the phase-change switching is controlled by a voltage pulse, I is given by $V / (R_L + R_D)$ where $R_D = \rho L/\pi r^2$ is the device resistance. The magnitude of R_L for the case of constant V_{th} (E_{th}) scaling is given by $R_L = \frac{V_{th}L}{Ar^2} - R_D$ ($\frac{E_{th}L^2}{Ar^2} - R_D$).

This simple analytical prediction was further confirmed with a finite-element numerical simulation using COMSOL. In the numerical simulation shown in Fig. 5, a GeTe cylinder with radius r and length L surrounded by SiO_2 and contacted by two gold electrodes was considered. Values of ρ, κ, and the specific heat (C_V) used in this simulation are: $\rho = 10^{-3}$ Ω cm, $\kappa = 2$ W / m K, $C_V = 1.5$ J / K cm^3 for GeTe, $\rho = 0$, $\kappa = 317$ W / m K, $C_V = 2.5$ J / K cm^3 for Au, $\rho = \infty$, $\kappa = 1.4$ W / m K, $C_V = 1.6$ J / K cm^3 for SiO_2. The lengths of gold and SiO_2 layer were 10 times that of the GeTe cylinder, and the boundary temperature was set to 300 K. R_L was determined for the condition where the final temperature was ~ 500 K for GeTe. As shown in Fig. 5b, the simulation results agree well with the analytical prediction.