

Supporting Information

Programmable Resistance Switching in Nanoscale Two-Terminal Devices

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Fabrication of a-Si pillar switches. The B-doped p-Si bottom electrode layer was deposited by LPCVD (low pressure chemical vapour deposition) on a prime grade silicon substrate with a 200 nm thermal silicon dioxide. The amorphous silicon layer was deposited on top of the B-doped p-Si, followed by two RIE (reactive ion etching) steps to define the a-Si pillar and the p-Si bottom electrode structures. Spin-on-glass (SOG) was then spin coated on the sample at speed of 3000 RPM and cured at 320 °C for 1 hour. The SOG layer was partially etched away to create a flat surface and expose the surface of the a-Si pillars. Ag electrodes to the a-Si pillars were patterned by e-beam lithography and lift-off. Ohmic contacts to the bottom p-Si layer were achieved by Pt electrodes. Special care was given in the pattern design so that the overlap between the top and bottom electrodes is minimized to keep the direct leakage current through the SOG is low.

Measurement. A semiconductor parameter analyzer with a low noise pre-amplifier (Keithley 4200) was used for the DC I - V measurements to allow high resolution signal detection. For the pulse measurements a setup consisting of the switching device and a series resistor (e.g. 10 k Ω) was used. Write/read/erase/read pulse sequences were applied to the setup and I_{on} and I_{off} was monitored in situ by measuring the voltage drop across the series resistor. The programming pulse signals were generated by an arbitrary function generator (Tektronix AFG 3101) controlled via a Labview program.

Bias-Dependent Filament Formation

It is interesting to note the physical origin of V_0 in Equation (3) discussed in the main text. From Figure 2d and to first order, $E_a' = E_a - eEd$, where E_a is the activation energy at zero bias, e is the electron charge assuming the Ag particles are singly charged^{1,2}, E is the electric field and d is the distance between the Ag particle and the peak of the barrier. If we assume that most of the voltage is dropped across the Ag chain and the Ag particles are evenly distributed within the chain then to first order (Fig. 2d) $E_a'(V) = E_a - eV/2n$, where n is the number of the Ag sites. Equation (3) can then be directly derived from Equation (1), with $\tau_0 = 1/\nu e^{E_a/k_B T}$ and $V_0 = 2nk_B T / e$. Interestingly, the V_0 value of 0.155V inferred from the fitting in Figure 2e is very close to that predicated by this simple model, $V_0 = 2nk_B T / e \approx 0.156\text{V}$, assuming there are 3 Ag trapping sites along the chain that forms the filament ($n = 3$), as suggested by the number of major current steps in the semi-log I-V plot in Figure 1c.

The characteristics dwell time vs. bias for 60 nm thick a-Si pillar switches was also measured and plotted in Figure S1 for a typical device. From the exponential fit, V_0 was extracted to be $\sim 0.22\text{ V}$ and consistent with the observed $n = 4$ major steps in the I - V plot in log-scale which leads to $V_0 = 2nk_B T / e \approx 0.21\text{V}$. We note the number of steps in the Ag particle chain is not proportional to the a-Si layer thickness (e.g., $n = 3$ for 30 nm thick devices and $n = 4$ for 60 nm thick devices). These observations can be qualitatively explained by Figure S2 which shows that the portion close to the top Ag electrode is composed of a large volume of Ag particles^{1,2} and effectively acts as a conductor. The device characteristics are mainly dominated by the regions adjacent to the bottom electrode. As a result, there is no direct relationship between the filament length and the a-Si layer thickness. These results are also consistent with earlier studies which show that qualitatively similar results can be observed

for devices with a-Si layer thickness ranging from a few nanometers³ to tens of nanometers⁴. On the other hand, a thinner a-Si layer will potentially lead to a larger slope in the wait time vs. bias function (e.g. Figures 2e and S1e) thus eventually a faster programming speed.

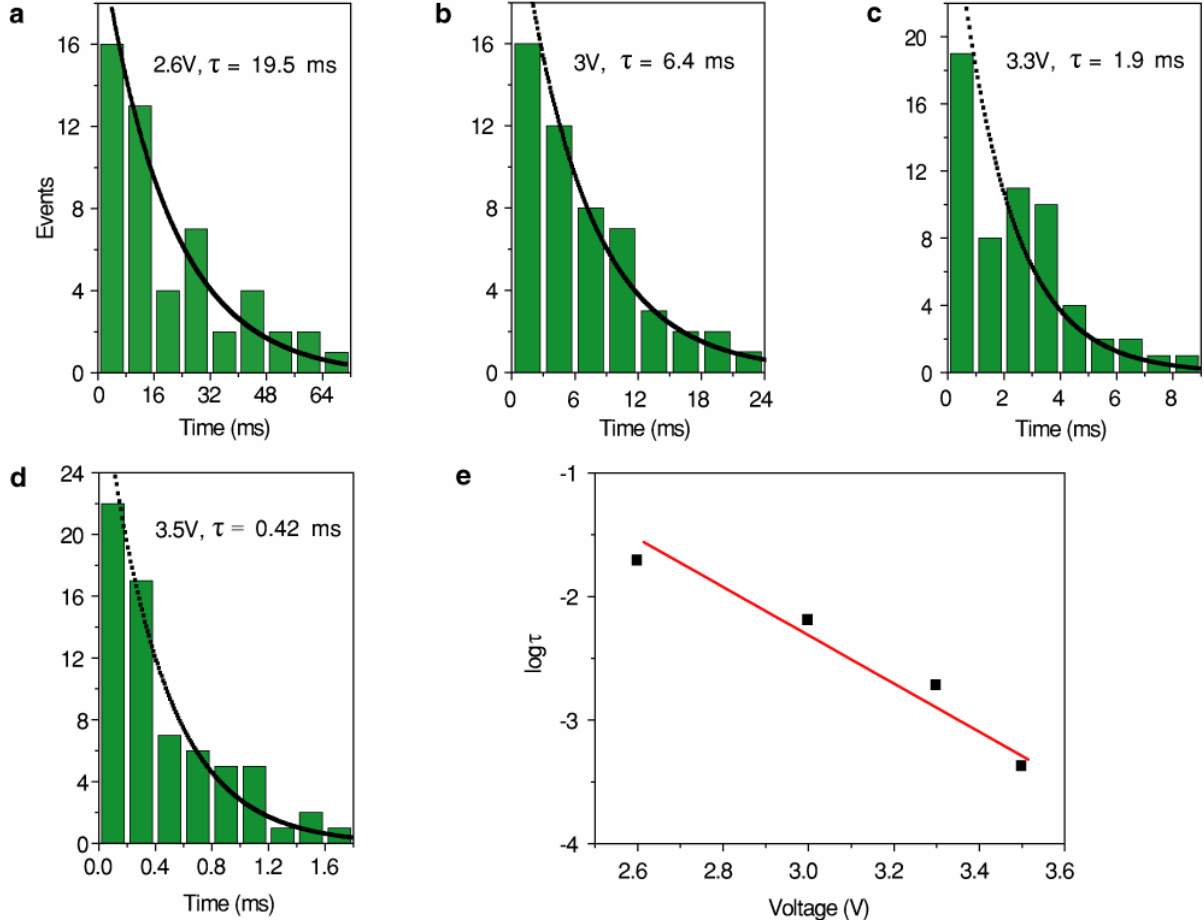


Figure S1. Bias-dependent switching characteristics of a device with a-Si layer thickness of 60 nm. a-d, Histograms of the wait time for the first switching event at bias voltages of 2.6 V, 3.0 V, 3.3 V and 3.5 V, respectively. The solid lines are fits according to Equation (2) using τ as the only fitting parameter. The device diameter was 60 nm. e, Characteristic wait time τ vs. bias along with an exponential fit according to Equation (3).

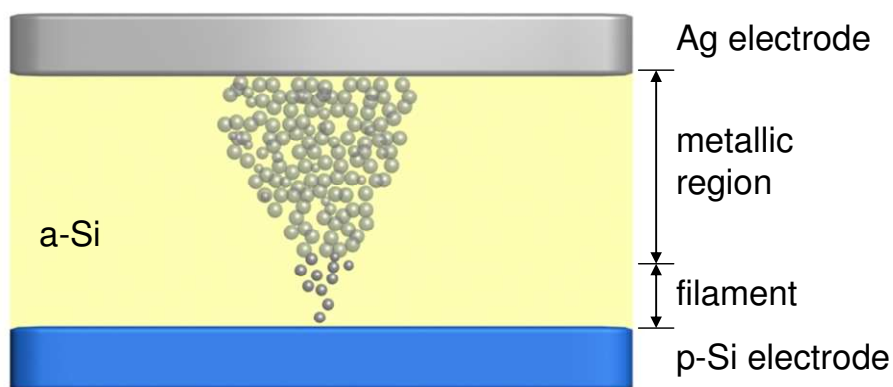


Figure S2. Schematic of the conduction path in the a-Si devices. The portion close to the top Ag electrode is composed of a large volume of Ag particles and the device characteristics are dominated by a single filament close to the bottom electrode.

References

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