Supporting Information

Probing the Surface Glass Transition Temperature of Polymer Films via Organic Semiconductor Growth Mode, Microstructure, and Thin-Film Transistor Response.

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Experimental Section

Reagents and Materials. Pentacene (**P5**, Aldrich) was used after purification by multiple gradient vacuum sublimation, while α-sexithiophene (**α-6T**, Aldrich) was used as received. The semiconductors α,ω-diperfluorohexylcarbonylquarterthiophene (**DFHCO-4T**),[1] α,ω-diperfluorohexylquarterthiophene (**DFH-4T**),[2] 5,5'-bis(4-n-perfluorooctylphynyl)-2,2'-bithiophene (**DFO-PTTP**),[3] and N,N'-bis(n-octyl)-1,7- and N,N'-bis(n-octyl)-1,6-dicyanoperylene-3,4:9,10-bis-(dicarboximide) (**PDI-8CN$_2$**)[4] were available in our laboratory. Polystyrene (PS1, M_n = 280 kg/mol; PS2, M_n = 13 kg/mol; PS3, M_n = 4 kg/mol), poly(4-methylstyrene) (PMS, M_n = 72 kg/mol), poly(methyl methacrylate) (PMMA1, M_n = 15 kg/mol; PMMA2, M_n = 45 kg/mol), poly(t-butylstyrene) (PTBS, M_n = 32 kg/mol), and poly(4-vinylphenol) (PVP, M_n = 20 kg/mol) were purchased from Aldrich and used without further purification. Poly(2-vinylpyridine) (P2VP, M_v = 200 kg/mol) was purchased from Scientific Polymer Products and was used after drying the as-received material in a vacuum oven at ~110 ^{o}C to remove residual monomer. Dioctylphthalate (DOP) (99%, Aldrich) was used as received. Heavily doped p-type Si wafers with a 300 nm thick thermally grown SiO_2 layer (p^+-Si/SiO_2) or n-type Si wafers with native oxide (n^+-Si) (Montco Silicon Tech) were used as device substrates. The calorimetric bulk T_g values for the present dielectric polymers were determined by differential scanning calorimetry (DSC; Mettler Toledo DSC822e, second heat, onset method, 10 K min^{-1}).

Polymer Film Fabrication and Characterization. Pentacene-based TFTs were fabricated on heavily doped p-type Si wafers with a 300 nm thick thermally grown SiO_2 layer (PS1, 70 mg/mL, was also fabricated on heavily doped n-type Si wafers with a native oxide layer). All substrates were cleaned by sonication in ethanol (200 proof) for 3 min, followed by oxygen plasma treatment for 5 min (20W, 0.5 Torr). PS1 (5, 20, 30, 50, 70 mg/mL in anhydrous toluene), PS2 (10, 30 mg/mL in anhydrous toluene), PS3 (5, 20 mg/mL in anhydrous toluene), PMS (5 mg/mL in anhydrous toluene), PVA (30 mg/mL in millipore water), P2VP (3, 5, 20 mg/mL in 1,1,2-trichloroethane), PMMA1 (5, 10, 40 mg/mL in anhydrous toluene), PMMA2 (20 mg/mL in anhydrous toluene), PTBS (10 mg/mL in anhydrous toluene), PVP (20 mg/mL in anhydrous THF), and DOP-doped (4 wt%) PS1 (6, 25 mg/mL in anhydrous toluene) were all spin-coated onto the substrates at 2000−5000 rpm in air, and the resulting films dried in a vacuum oven at 80 – 90 °C overnight.[5] Bilayer polymer films (PS1/P2VP) on 300 nm SiO_2 substrates with top layers of PS1 (5 mg/mL in anhydrous toluene) were spin-coated directly onto the P2VP (5, 20, 40 mg/mL in 1,1,2-trichloroethane) films, since toluene is a nonsolvent for P2VP.[39] Oxygen plasma-treated polymer films (PS1/2- and PVP-OXY) were prepared by exposure to an O_2-plasma for 10 s. The present polymer films afford very smooth morphologies with root-mean-square (RMS) roughnesses of ~ 0.3 nm except in the case of bilayer polymer films where the RMS roughness is ~ 0.5 nm, as characterized by tapping-mode AFM using a Si cantilever. All film thicknesses were measured by profilometer (Tencor, P10).

Device Fabrication and Characterization. The organic semiconductors were vacuum-deposited at ~ 5×10^{-6} Torr (500 Å, ~ 0.5 Å/s for pentacene, ~ 0.3 Å/s for the other semiconductors) at preset deposition temperatures (T_D) of 25 − 90 °C. For post-annealing experiments, pentacene films were deposited on the various polymer gate dielectrics at 25 °C and were annealed on a hot plate under nitrogen at various annealing temperatures (T_A). Thin films of pentacene were analyzed by X-ray diffraction (θ/2θ and ω scan) in a slit-configuration using Ni-filtered Cu Kα radiation (Rigaku ATXG) and by AFM (JEOL-5200 Scanning Probe Microscope) in the tapping mode. For OTFT/MIS (metal-insulator-semiconductor) device fabrication, top-contact electrodes (~ 50 nm) were deposited by evaporating gold (< 1×10^{-6}

Torr) through a shadow mask with channel length (L) and width (W) defined as 100 μm and 5000 μm, respectively.

Electrical Measurements. The capacitances of the present dielectric films were measured on MIS structures using a Signaton probe station equipped with a digital capacitance meter (Model 3000, GLK Instruments) and an HP4192A impedance analyzer (Figure S12). All OTFT measurements were carried out under vacuum (1×10^{-5} Torr) using a Keithly 6430 subfemtoammeter and a Keithly 2400 source meter, operated by a local Labview program with GPIB communication. Mobilities (μ) were calculated in the saturation regime using the standard relationship: $\mu_{sat} = (2I_{DS}L)/[WC_i(V_G\text{-}V_T)^2]$, where I_{DS} is the source-drain saturation current, C_i is the gate dielectric capacitance (per area), V_G is the gate voltage, and V_T is the threshold voltage. The latter can be estimated as the x intercept of the linear section of the plot of V_G vs. $(I_{DS})^{1/2}$.[6]

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(2) Facchetti, A.; Mushrush, M.; Yoon, M.-H.; Hutchison, G. R.; Ratner, M. A.; Marks, T. J. *J. Am. Chem. Soc.* **2004**, *126*, 13859-13874.

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(4) Jones, B. A.; Ahrens, M. J.; Yoon, M.-H.; Facchetti, A.; Marks, T. J.; Wasielewski, M. R. *Angew. Chem. Int. Ed.* **2004**, *43*, 6363-6366.

(5) Kim, C.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2007**, *19*, 2561-2566.

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Table S1. Field-Effect Mobility (μ_{sat}, $cm^2/V{\cdot}s$)[a], Current On/Off Ratio (I_{on}:I_{off}), Threshold Voltage (V_T, V) data for Pentacene TFTs fabricated on the Indicated Bilayer Gate Dielectrics and on c-SiO_2 as a Function of Pentacene Film Deposition Temperature (T_D).

Gate Diel.	T_g[b] (°C)	d (nm)		T_D (°C)												
				25	35	40	45	50	55	60	65	70	75	80	85	90
			μ	0.23				0.20		0.18		0.20		0.18		0.24
c-SiO_2	1175		(I_{on}:I_{off})	(10^8)				(10^8)		(10^8)		(10^7)		(10^8)		(10^6)
			V_T	-22				-22		-24		-23		-25		-14
			μ	0.65				0.68	0.66	0.42	0.05	0.05	0.02	0.01		
		20	(I_{on}:I_{off})	(10^6)				(10^5)	(10^6)	(10^6)	(10^5)	(10^6)	(10^7)	(10^6)		
			V_T	-17				-22	-14	-23	-30	-21	-27	-24		
			μ					0.65	0.59	0.40	0.10	0.05				
		150	(I_{on}:I_{off})					(10^6)	(10^6)	(10^5)	(10^6)	(10^6)				
			V_T					-38	-42	-40	-43	-42				
PS1	103		μ					0.67	0.59	0.44	0.10	0.06				
		400	(I_{on}:I_{off})					(10^6)	(10^6)	(10^6)	(10^7)	(10^5)				
			V_T					-66	-66	-61	-78	-80				
			μ					0.68	0.57	0.38	0.10	0.08				
		800[c]	(I_{on}:I_{off})					(10^6)	(10^7)	(10^6)	(10^6)	(10^6)				
			V_T					-81	-77	-86	-89	-81				
			μ									0.17				
PS1-OXY	103	150	(I_{on}:I_{off})									(10^4)				
			V_T									-23				
			μ	0.54		0.47	0.45	0.34	0.04	0.05	0.007	0.004				
PS2	94	24	(I_{on}:I_{off})	(10^4)		(10^5)	(10^5)	(10^4)	(10^7)	(10^5)	(10^6)	(10^7)				
			V_T	-18		-22	-24	-16	-17	-22	-22	-36				
			μ									0.16				
PS2-OXY	94	80	(I_{on}:I_{off})									(10^4)				
			V_T									-21				
			μ	0.32	0.18	0.08	0.006	0.004	0.006	5x10^{-7}						
		10	(I_{on}:I_{off})	(10^6)	(10^5)	(10^5)	(10^7)	(10^6)	(10^7)	(10^3)						
PS3	83		V_T	-28	-16	-18	-32	-33	-32	-44						
			μ	0.34	0.17	0.20	0.02	0.04	0.005	0.003						
		50	(I_{on}:I_{off})	(10^6)	(10^5)	(10^5)	(10^4)	(10^7)	(10^5)	(10^6)						
			V_T	-25	-28	-29	-28	-27	-36	-37						

[a] Carrier mobilities calculated in saturation within the charge carrier concentration range of 3 – 4 × 10^{12} cm^{-2}. Standard deviations are typically < 10%; otherwise a mobility range is given. [b] From DSC data. [c] These films fabricated directly on Si substrates without a thermal oxide coating.

Table S1. Field-Effect Mobility (μ_{sat}, cm^2/V·s)^a, Current On/Off Ratio (I_{on}:I_{off}), Threshold Voltage (V_T, V)data for Pentacene TFTs fabricated on the Indicated Bilayer Gate Dielectrics and on c-SiO_2 as a Function of Pentacene Film Deposition Temperature (T_D).

Gate Diel.	T_g^{b} (°C)	d (nm)		T_D (°C) 25	45	50	55	60	65	70	75	80	85	90
PVP	171	100	μ							0.34				
			(I_{on}:I_{off})							(10^7)				
			V_T							-20				
PVP-OXY	171	100	μ							0.15				
			(I_{on}:I_{off})							(10^4)				
			V_T							-14				
PMMA	86	10	μ	0.15		0.14	0.14	0.16	0.16	0.15	0.12	0.008	0.001	
			(I_{on}:I_{off})	(10^3)		(10^5)	(10^4)	(10^4)	(10^4)	(10^4)	(10^4)	(10^6)	(10^6)	
			V_T	-9		-19	-21	-19	-16	-15	-13	-19	-25	
		20	μ	0.18		0.14	0.14	0.14	0.17	0.16	0.16	0.06	0.005	2x10^{-6}
			(I_{on}:I_{off})	(10^4)		(10^5)	(10^4)	(10^4)	(10^4)	(10^4)	(10^4)	(10^4)	(10^7)	(10^4)
			V_T	-11		-22	-21	-24	-19	-16	-14	-18	-26	-34
		100	μ	0.17		0.15	0.15	0.15	0.16	0.17	0.10	0.008	0.004	2x10^{-7}
			(I_{on}:I_{off})	(10^4)		(10^5)	(10^4)	(10^4)	(10^4)	(10^4)	(10^4)	(10^5)	(10^6)	(10^2)
			V_T	-25		-25	-24	-29	-24	-31	-24	-28	-23	-14
PMS	107	20	μ	0.73		0.63	0.65	0.58	0.56	0.25	0.15	3x10^{-5}		
			(I_{on}:I_{off})	(10^5)		(10^6)	(10^5)	(10^5)	(10^5)	(10^5)	(10^5)	(10^4)		
			V_T	-18		-20	-30	-31	-30	-24	-26	-23		
PTBS	137	30	μ	0.59					0.63	0.49	0.07 -0.17	0.001 -0.27	0.04 -0.22	0.04
			(I_{on}:I_{off})	(10^4)					(10^6)	(10^5)	(10^8 -10^6)	(10^7 -10^6)	(10^8 -10^6)	(10^8)
			V_T	-7					-24	-9	-27 / -19	-34 / -24	-22 / -15	-30
P2VP	103	8	μ	0.08		0.09	0.08	0.08	0.02	0.02	5x10^{-4}	4x10^{-6}		
			(I_{on}:I_{off})	(10^5)		(10^5)	(10^5)	(10^5)	(10^5)	(10^5)	(10^3)	(10^1)		
			V_T	-21		-26	-27	-26	-25	-21	-28	-25		
		12	μ	0.07		0.07	0.08	0.06	0.01	0.01	5x10^{-4}	2x10^{-6}		
			(I_{on}:I_{off})	(10^5)		(10^5)	(10^5)	(10^5)	(10^5)	(10^5)	(10^3)	(10^1)		
			V_T	-21		-25	-25	-23	-21	-20	-25	-15		
		70	μ	0.08		0.07	0.09	0.08	0.02	0.02	1x10^{-3}	1x10^{-7}		
			(I_{on}:I_{off})	(10^5)		(10^5)	(10^5)	(10^5)	(10^4)	(10^4)	(10^6)	(10^1)		
			V_T	-30		-31	-29	-29	-25	-22	-21	-51		

^{a} Carrier mobilities calculated in saturation within the charge carrier concentration range of 3 – 4 × 10^{12} cm^{-2}. Standard deviations are typically < 10%; otherwise a mobility range is given. ^{b} From DSC data.

Table S2. Field-Effect Mobility (μ_{sat}, cm^2/V·s)[a], Current On/Off Ratio (I_{on}:I_{off}), Threshold Voltage (V_T, V)data for Pentacene TFTs fabricated on the Indicated Multilayer and DOP-doped Polymer Gate Dielectrics and on c-SiO_2 as a Function of Pentacene Film Deposition Temperature (T_D).

Gate Diel.	T_g[b] (°C)	d (nm)		T_D (°C)							
				25	45	50	55	60	65	70	75
PS1 /P2VP	103	12/12	μ	0.52	0.59	0.47	0.34	0.20	0.04	0.002	0.006
			(I_{on}:I_{off})	(10^6)	(10^6)	(10^5)	(10^5)	(10^5)	(10^6)	(10^6)	(10^6)
			V_T	-26	-27	-26	-26	-27	-31	-34	-44
		12/65	μ	0.56	0.45	0.40	0.39	0.19	0.03	0.004	0.006
			(I_{on}:I_{off})	(10^6)	(10^5)	(10^5)	(10^5)	(10^5)	(10^6)	(10^7)	(10^7)
			V_T	-27	-25	-26	-26	-27	-24	-33	-31
		12/205	μ	0.44	0.39	0.32	0.31	0.18	0.03	0.004	0.0002
			(I_{on}:I_{off})	(10^6)	(10^6)	(10^5)	(10^5)	(10^5)	(10^6)	(10^6)	(10^6)
			V_T	-34	-34	-36	-36	-34	-34	-49	-52
DOP (4 wt%)-doped PS1	103	18	μ	0.41	0.63	0.69	0.50	0.42	0.07	0.03	3x10^{-4}
			(I_{on}:I_{off})	(10^7)	(10^6)	(10^5)	(10^5)	(10^5)	(10^7)	(10^7)	(10^6)
			V_T	-23	-26	-26	-17	-24	-20	-27	-44
		80	μ	0.33	0.47	0.47	0.40	0.35	0.09	0.07	0.004
			(I_{on}:I_{off})	(10^6)	(10^5)	(10^6)	(10^5)	(10^5)	(10^5)	(10^5)	(10^4)
			V_T	-28	-32	-32	-35	-32	-29	-28	-29

[a] Carrier mobilities calculated in saturation within the charge carrier concentration range of 3 – 4 × 10^{12} cm^{-2}. Standard deviations are typically < 10%; otherwise a mobility range is given. [b] From DSC data.

Table S3. Field-Effect Mobility (μ_{sat}, cm^2/V·s)[a], Current On/Off Ratio (I_{on}:I_{off}), Threshold Voltage (V_T, V) data for Post-annealed Pentacene TFTs Fabricated on the Indicated Gate Dielectrics and on c-SiO_2 as a Function of Annealing Temperature (T_A).

Gate Diel.	T_g[b] (°C)	d (nm)		T_A (°C)						
				25	70	90	100	110	130	160
c-SiO_2	1175		μ	0.39	0.41	0.41	0.24	0.23	0.04	0.009
			(I_{on}:I_{off})	(10^6)	(10^5)	(10^5)	(10^4)	(10^4)	(10^5)	(10^5)
			V_T	-25	-20	-21	-17	-19	-23	-23
PS1	103	80	μ	0.63	0.53	0.51	0.13	0.04	0.03	0.007
			(I_{on}:I_{off})	(10^6)	(10^5)	(10^5)	(10^5)	(10^5)	(10^7)	(10^7)
			V_T	-32	-33	-37	-37	-39	-26	-28
PMMA2	108	60	μ	0.27	0.24	0.23	0.11	0.09	0.03	0.004
			(I_{on}:I_{off})	(10^4)	(10^4)	(10^4)	(10^4)	(10^6)	(10^6)	(10^7)
			V_T	-34	-33	-34	-35	-29	-29	-28
P2VP	103	70	μ	0.08	0.08	0.08	0.03	0.02	0.003	0.0001
			(I_{on}:I_{off})	(10^5)	(10^5)	(10^5)	(10^5)	(10^6)	(10^6)	(10^3)
			V_T	-33	-32	-13	-25	-20	-29	-22

[a] Carrier mobilities calculated in saturation within the charge carrier concentration range of 3 – 4 × 10^{12} cm^{-2}. Standard deviations are typically < 10%; otherwise a mobility range is given. [b] From DSC data.

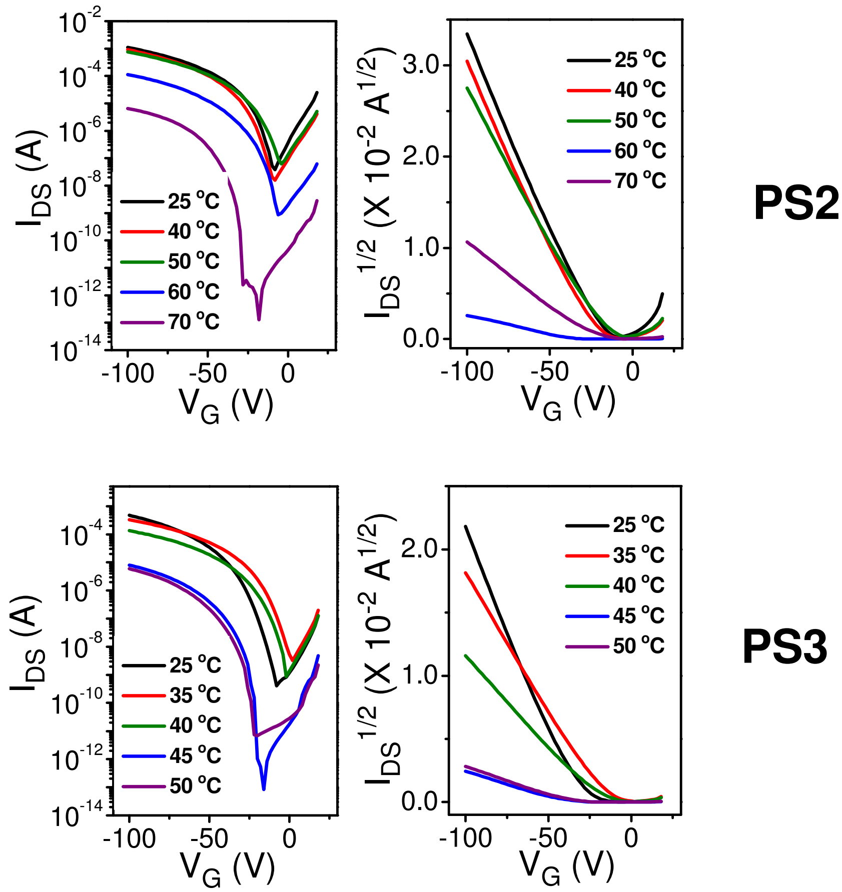

Figure S1. Transfer plots of pentacene TFTs fabricated on PS2 (24 nm) and PS3 (10 nm) gate dielectrics at the indicated T_Ds.

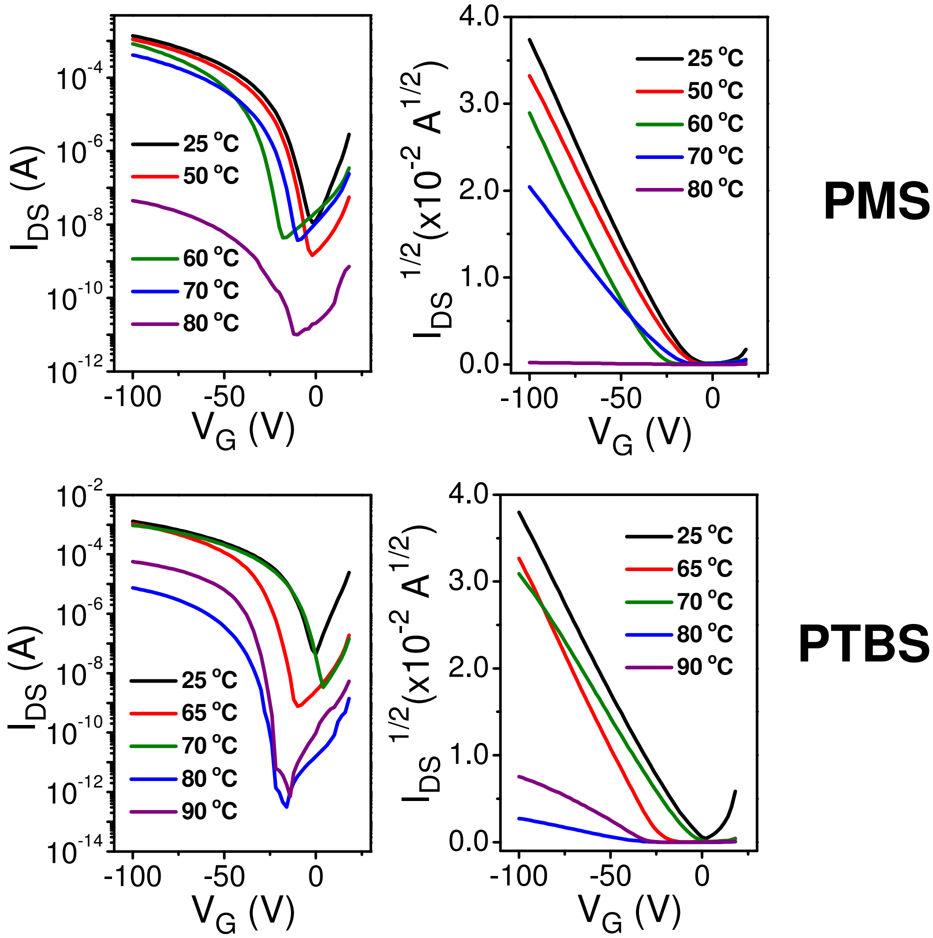

Figure S2. Transfer plots of pentacene TFTs fabricated on PMS (20 nm) and PTBS (30 nm) gate dielectrics at the indicated T_Ds.

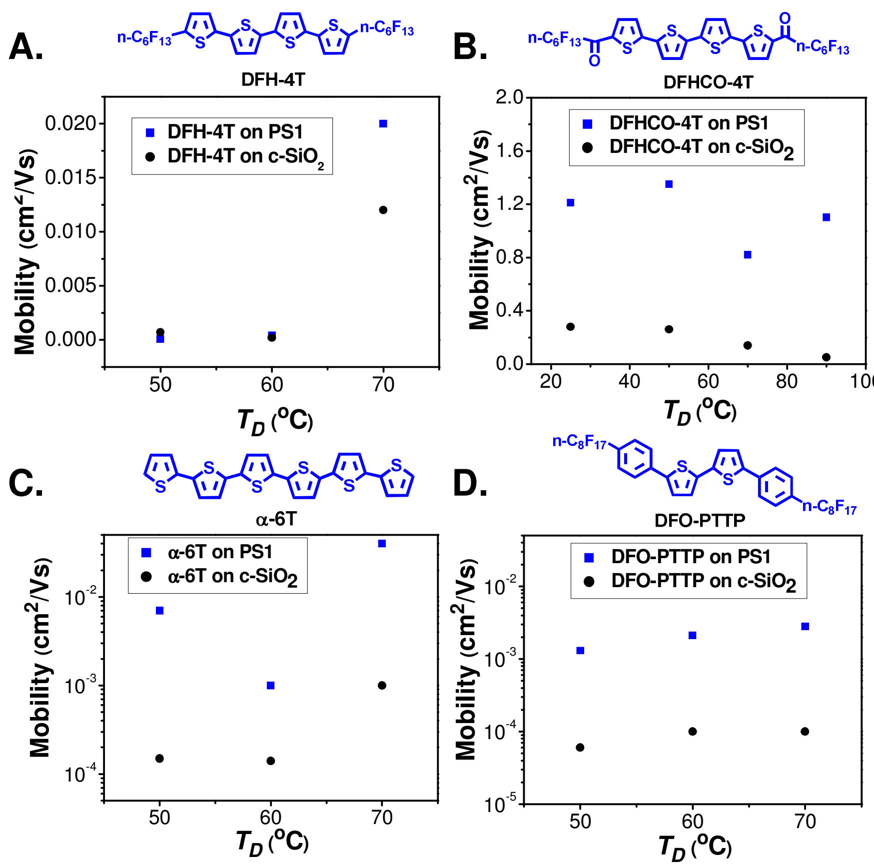

Figure S3. Field-effect mobilities of (A) DFH-4T, (B) DFHCO-4T, (C) α-6T, and (D) DFH-PTTP TFTs fabricated at the indicated T_Ds on PS1 (20 nm) polymer gate dielectrics and on c-SiO_2.

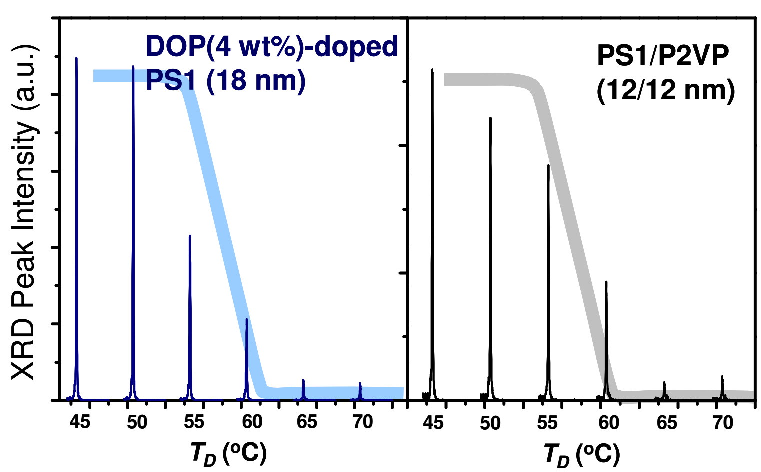

Figure S4. XRD (θ/2θ scan) data for 50 nm thick pentacene films grown on DOP(4 wt%)-doped PS1 (18 nm) and PS1/P2VP (12/12 nm) gate dielectrics at the indicated T_Ds. The solid lines are drawn as guides to the eye.

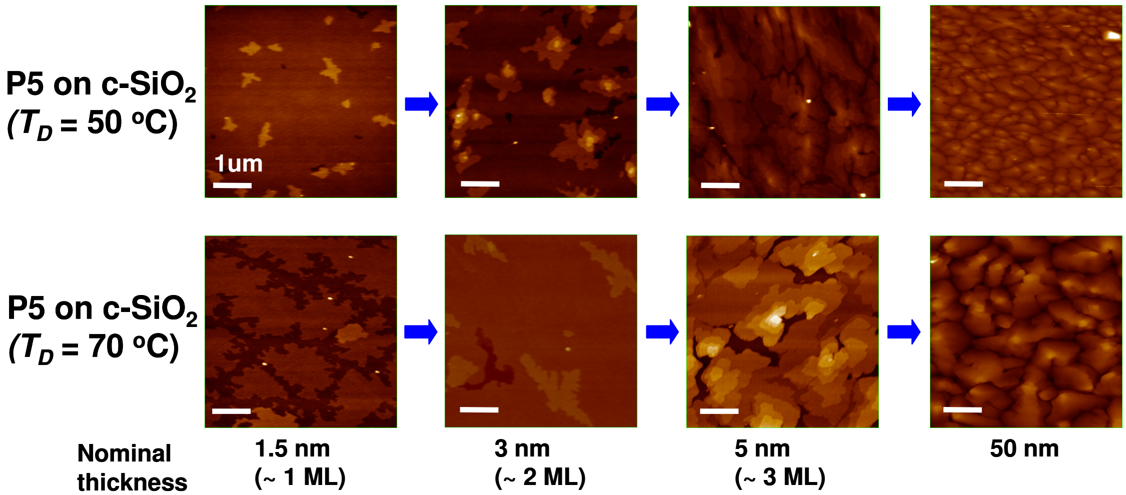

Figure S5. AFM images (5.0 × 5.0 μm^2) of vacuum-deposited pentacene films (1.5 – 50 nm) grown on c-SiO_2 gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

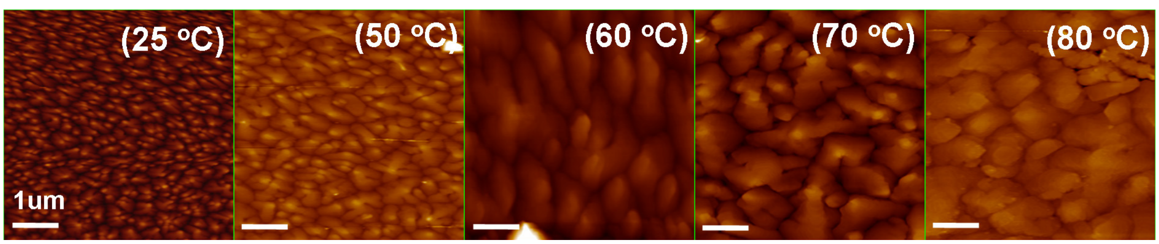

Figure S6 AFM images (5.0 × 5.0 μm^2) of 50 nm thick pentacene films grown on c-SiO_2 gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

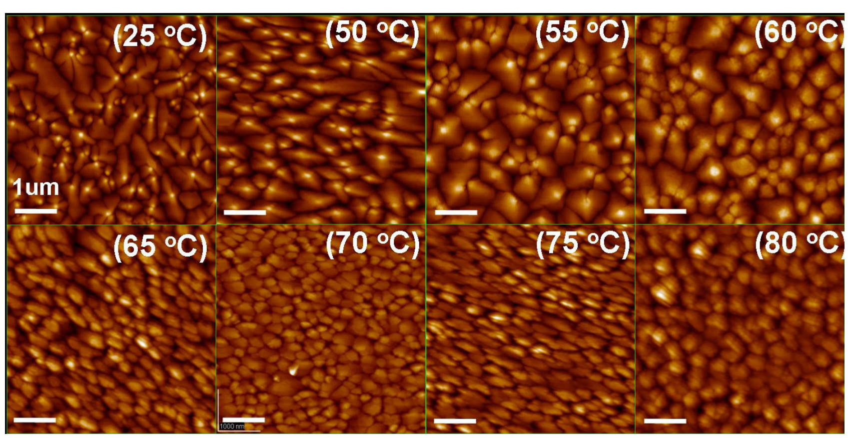

Figure S7. AFM images (5.0 × 5.0 μm^2) of 50 nm thick pentacene films grown on PS1 gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

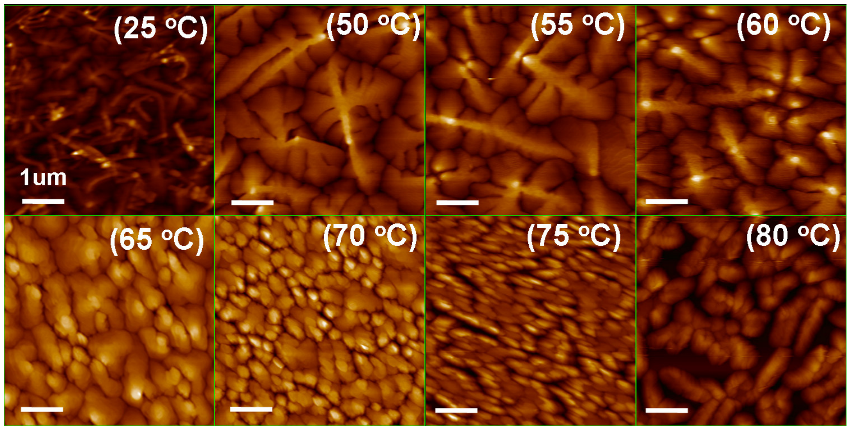

Figure S8. AFM images (5.0 × 5.0 μm^2) of 50 nm thick pentacene films grown on P2VP (12 nm) gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

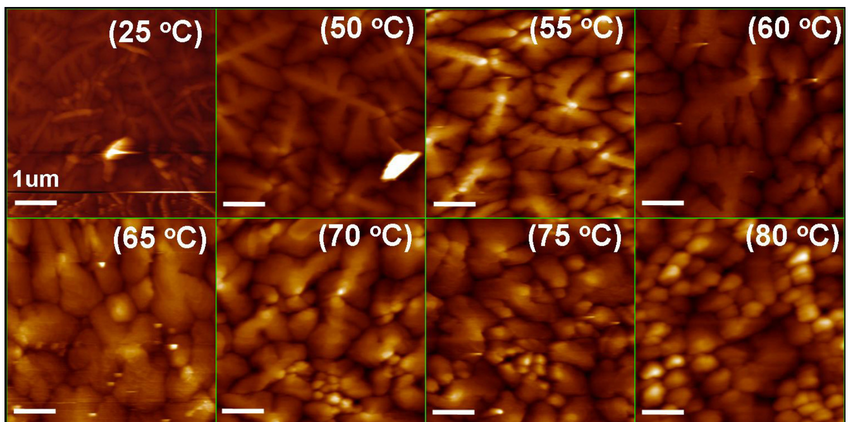

Figure S9. AFM images (5.0 × 5.0 μm^2) of 50 nm thick pentacene films grown on PMMA (10 nm) gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

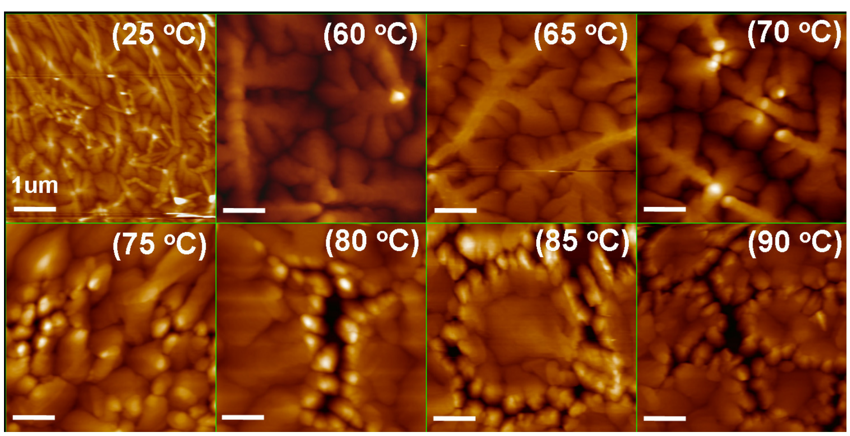

Figure S10. AFM images (5.0 × 5.0 μm^2) of 50 nm thick pentacene films grown on PTBS (30 nm) gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

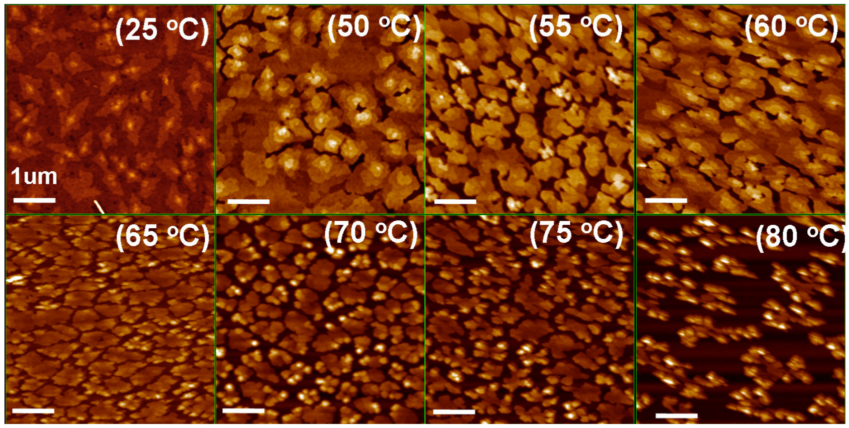

Figure S11. AFM images (5.0 × 5.0 μm^2) of 5 nm thick pentacene films grown on PS1 gate dielectrics at the indicated T_Ds. The scale bars indicate 1 μm.

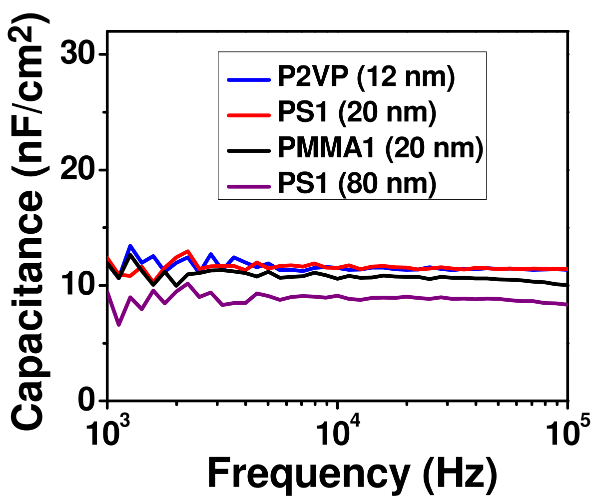

Figure S12. Capacitance-frequency plot for bilayer polymer/SiO_2 dielectrics measured on MIS structure (AC driving voltage = 0.1 V, DC bias offset = -10 V).