Supporting Information for "Direct Heteroepitaxy of Vertical InAs Nanowire Array on Si (111) Substrates for Broadband Photovoltaics and Photodetection"

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Electrical properties of as-grown InAs nanowires.

Back-gated FETs were fabricated to test the single InAs nanowire electrical properties. The InAs nanowires were dispersed in solution and transferred to the SiO_2/Si substrate with the 600 nm SiO_2 and the p^+-Si acting as a dielectric layer and a back-gate, respectively. The InAs nanowires with diameter around 40 nm were chosen and the contacts were patterned by electron-beam lithography. 20 nm thick Ti and 80 nm thick Al layers were deposited sequentially as electrodes immediately after removal of the native oxide by quick etching in HF solution. The I_{ds}-V_{ds} of a typical device with gate modulation is shown in Figure S1 and the inset. Ohmic contacts were formed between the nanowires and the electrodes. An average resistivity of 1.5×10^{-3} Ωcm was calculated from the output characteristics of 7 devices (neglecting the contact resistance), which is very close to the values previously reported for InAs nanowire FETs.[1, 2] An n-type behavior was shown clearly by the gate voltage response. The average electron mobility and concentration were estimated to be around 1,000 cm^2/Vs and 10^{18}-10^{19} cm^{-3}, respectively, using the commonly applied method for nanowire back-gated devices.[2-5] These values are also comparable to those of InAs nanowires grown using the Au catalysts.[2, 3]

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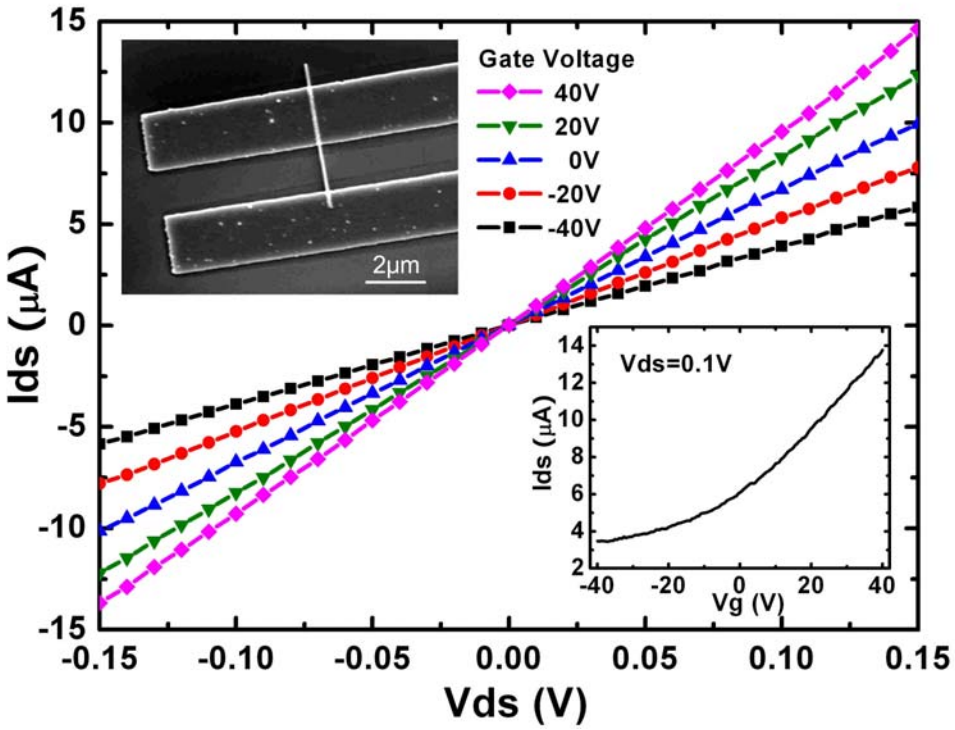

Figure S1. *I-V* characteristics of a single InAs nanowire back-gated field effect transistor (FET) at different gate voltages. Inset is the SEM image of a single InAs nanowire back-gated FET device (left) and the transconductance curve of a typical device at V_{ds} = 0.1 V (right). The channel length is about 1.7 μm and the nanowire diameter is about 40 nm.

Analysis of the temperature dependent energy conversion efficiency and fill factor.

The theoretical upper-limit of the energy conversion efficiency (ECE) and fill factor (FF) of the p-Si/n-InAs heterojunction photodiode tested under AM 1.5 illumination at a fixed power intensity of 2.86mW/cm^3 can be predicted at different temperatures by considering the ideal case when the diode ideality factor to be unity (A=1) and series resistance to be zero (R_s=0).

The output power (P) of the photodiode is given by:

$$P = -IV = I_{ph}V - I_0V\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1)$$

where I is output current, V is the output voltage, I_{ph} is the photo-generated current, I_0 is the reversed saturated current, q is the elementary charge, k is the Boltzmann constant, and T is temperature. The

current density (I_{max}) and voltage (V_{max}) at maximum power points of the I-V curve is given by $\partial P/\partial V=0$ with considering $I_0 = I_{00}\exp[-(E_{g1}-\Delta E_c)/kT]$ and $I_{ph}/I_0 \gg 1$.

$$V_{\max} = \frac{(E_{g1}-\Delta E_c)}{q} + \frac{kT}{q}\ln\left[\frac{I_{ph}}{I_{00}\left(\frac{qV_{\max}}{kT}\right)}\right] \tag{2}$$

$$I_{\max} = I_{00}\exp\left[\frac{(E_{g1}-\Delta E_c)}{kT}\right]\left[\exp\left(\frac{qV_{\max}}{kT}\right)-1\right] - I_{ph} \tag{3}$$

where E_{g1} is the bandgap of Si and ΔE_c is conduction band offset (See Figure 3 in the paper). From the paper, $I_{00} = qA_2N_{v1}[(kT/2\pi m_1^*)^{1/2} + S_{\text{int}}]$, where the N_{v1} is the effective density of states in valence band of p-Si and m_1^* is the effective mass of holes in Si. Recalling the open-circuit voltage (V_{oc}) and short circuit current (I_{sc}) from the paper,

$$V_{oc} = \frac{(E_{g1}-\Delta E_c)}{q} + \frac{kT}{q}\ln\left(\frac{I_{ph}}{I_{00}}\right) \tag{4}$$

$$I_{sc} = I_{ph} \tag{5}$$

the FF and ECE can be calculated by:

$$ECE = \frac{V_{\max}I_{\max}}{P_{in}} = \frac{\left\{\frac{(E_{g1}-\Delta E_c)}{q} + \frac{kT}{q}\ln\left[\frac{I_{ph}}{I_{00}\left(\frac{qV_{\max}}{kT}\right)}\right]\right\}\left\{I_{00}\exp\left[\frac{(E_{g1}-\Delta E_c)}{kT}\right]\left[\exp\left(\frac{qV_{\max}}{kT}\right)-1\right]-I_{ph}\right\}}{P_{in}} \tag{6}$$

$$FF = \frac{V_{\max} I_{\max}}{V_{oc} I_{sc}} = \frac{\left\{ \frac{(E_{g1} - \Delta E_c)}{q} + \frac{kT}{q} \ln\left[\frac{I_{ph}}{I_{00}\left(\frac{qV_{\max}}{kT} \right)} \right] \right\} \left\{ I_{00} \exp\left[\frac{(E_{g1} - \Delta E_c)}{kT} \right] \left[\exp\left(\frac{qV_{\max}}{kT} \right) - 1 \right] - I_{ph} \right\}}{I_{ph} \left[\frac{(E_{g1} - \Delta E_c)}{q} + \frac{kT}{q} \ln\left(\frac{I_{ph}}{I_{00}} \right) \right]} \quad (7)$$

The hole thermionic emission velocity (v_t) in p-Si is mild temperature dependent. Using the average value $v_t = \sqrt{kT / 2\pi m_1^*} \sim 5 \times 10^6$ cm/s, $N_{v1} = 1.8 \times 10^{19}$ /cm^3, $A_2 = A_1 (d/D)^2 = 2.56 \times 10^{-3}$ cm^2 and assuming S_{int} to be very small in our device due to the high quality abrupt nanowire/substrate heterojunctions which are nearly free from interface states, I_{00} can be given by $I_{00} = qA_2 N_{v1} [(kT / 2\pi m_1^*)^{1/2} + S_{\text{int}}] \sim 4 \times 10^4$ A. Considering $E_{g1} - \Delta E_c \sim 1$eV and I_{ph}~2×10^{-5}A and assuming the device is a perfect diode (A=1) and without any series resistance (R_s=0), the temperature dependent ECE and FF can be calculated by Eqs. (6), (7) and plotted as shown in Figure S2, which shows the theoretical upper-limit of ECE and FF of the device under AM 1.5 illumination at P_{in}=2.86 mW/cm^3. As shown in Figure S2, the ECE and FF both increase monotonically with decreasing temperature in and ideal diode case. In reality, however, the series resistance is non-zero and will change with temperature. When temperature goes down, the changing series resistance, combining with the diode ideality factor and all other non-ideal factors, make the ECE and FF of the photodiode change non-monotonically with temperature. The ECE does increase with the decreasing temperature at the beginning. But it reaches the maximum at certain temperature (110K) and then slightly drops down by further lowering the temperature, as in Figure 3b in the paper.

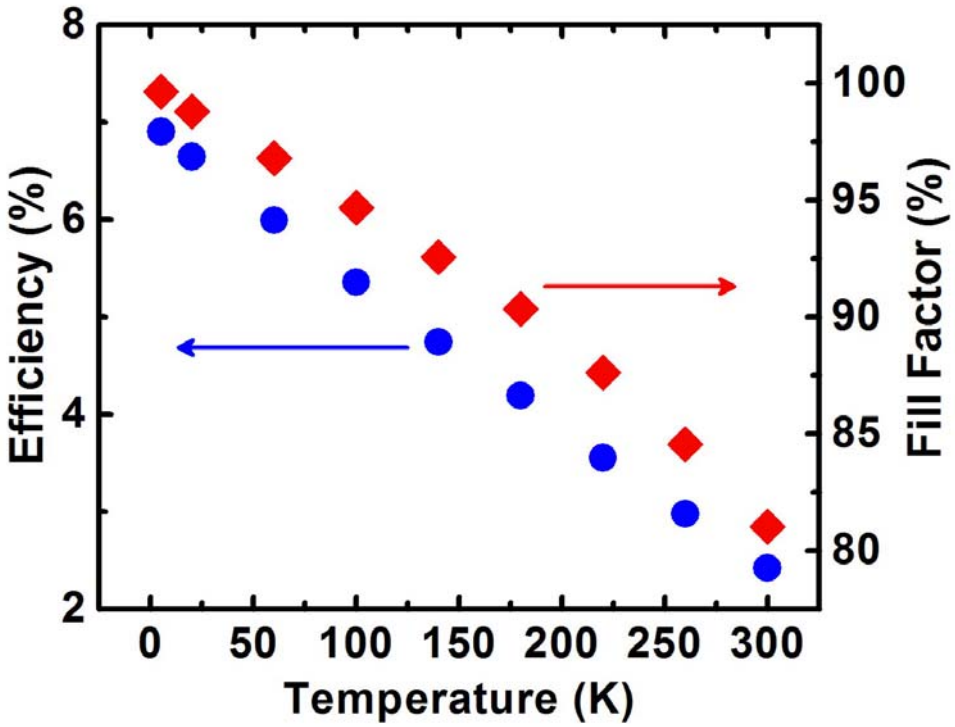

Figure S2. Calculated energy conversion efficiency (blue dots) and fill factor (red diamonds) of the p-Si/n-InAs heterojunction photodiode in ideal case (ideality factor A=1 and series resistance R_s=0) under AM 1.5 illumination at a power intensity of 2.86mW/cm^3.

References:

1.Martensson, T.; Wagner, J. B.; Hilner, E.; Mikkelsen, A.; Thelander, C.; Stangl, J.; Ohlsson, B. J.; Gustafsson, A.; Lundgren, E.; Samuelson, L.; Seifert, W. *Adv. Mater.* **2007,** 19, 1801.

2.Dayeh, S. A.; Aplin, D. P. R.; Zhou, X. T.; Yu, P. K. L.; Yu, E. T.; Wang, D. L. *Small* **2007,** 3, 326-332.

3.Dayeh, S. A., Yu, E. T., Wang D. L. *Adv. Funct. Mater.* **2009,** in press.

4.Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Ph, A. *Appl. Phys. Lett.* **1998,** 73, 2447-2449.

5.Cui, Y.; Duan, X. F.; Hu, J. T.; Lieber, C. M. *J. Phys. Chem. B* **2000,** 104, 5213-5216.