SUPPORTING INFORMATION

Low operating bias and matched input-output characteristics in graphene logic inverters

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1. Formation of top gate stacks by a simple one-step metal deposition

The conventional way to form the top gate stacks with a natural AlOx dielectric layer is as follows. 1) Deposit a very thin (usually in few nanometers) aluminum layer; 2) Break the vacuum and expose devices to air to form the AlOx layer by passivation; 3) Deposit top gate metal. In such a method, the vacuum should be broken during the process. While in our novel way, the gate stacks (containing both electrode and oxide dielectric layers) can be simply fabricated in a ONE-STEP deposition of 30 nm aluminum, without breaking vacuum midway. In the deposition process, no dielectric layer between Al and graphene is intentionally introduced; instead the dielectric layer is formed after air exposure. The fabrication process is shown in Fig. S1.

People often have the intuition that the oxygen cannot diffuse into the Al/graphene interface after the Al deposition. Our method appears contradicted with the intuition, but it indeed works. For the formation of gate oxide below our thick Al layer, we attribute to the weak interaction between aluminum and graphene as revealed by theoretical calculation,[R1] and the oxygen diffusion into the interface as the device is exposed to air. The oxidation process arises from the passivation effect of aluminum and is expected to terminate at some oxide thickness. Thus, the oxide layer is expected to be uniform.

2. Capacitance and leakage of the natural alumina dielectric beneath TG

In graphene, both the top and bottom gates can effectively control the carrier density and contribute to the position of CNP together. From the trace of CNP on the two-dimensional resistance plot (dashed lines in Fig. S2a), a linear relation between the variations of V_{TG} and V_{BG} can be deduced. When V_{BG} is varied from -30 to 30 V, the CNP position changes from 1.10 to -0.95 V on the V_{TG} axis accordingly. This indicates that the bias change of about 2 V on TG is equivalent to that of 60 V on the 90-nm-SiO_2 incorporated silicon BG, or, equivalently, 200 V on the normally used 300-nm-SiO_2 incorporated silicon BG. Compared with the 300-nm-SiO_2 dielectric, the natural alumina dielectric beneath the Al TG shows 100 times enhancement on the coupling capacitance, i.e., $C_{AlO_x} / C_{300\,\text{nm-SiO}_2} = 100$. Taking into account the capacitance of parallel plate capacitors $C = \varepsilon_0 \varepsilon / t$, the thickness of the natural alumina dielectric is $t_{AlO_x} = \frac{1}{100} t_{SiO_2} \varepsilon_{AlO_x} / \varepsilon_{AlO_x}$. The thickness of the natural alumina TG dielectric layer is estimated to be 4–8 nm, given the fact that the typical relative permittivity of natural alumina ranges from 4.5 to 8.9.[R2]

For such a thin dielectric layer, the insulating ability and leakage should be carefully checked. In order to monitor the leakage currents from the TG, a load resistor of 100 kohm was connected in series. By measuring the voltage drops on the load resistor, real-time monitor of the leakage can be obtained. Figure S2b shows the leakage current for the TG stacks. Typically, the leakage is smaller than 0.2 nA, which is greatly smaller than the μA-order channel current, indicating an excellent dielectric property for the natural alumina beneath the TG. In addition, the voltage drop on the load resistors is below 20 μV, which is also negligible as compared with the gate biases.

3. Estimation of carrier mobility of the graphene channel under the natural alumina dielectric

For the TG-controlled graphene FETs, the total resistance between source and drain $R_{total}=R_{channel}+R_{contact}+R_{uncovered}$, where $R_{channel}$, $R_{contact}$ and $R_{uncovered}$ are the resistances from the graphene channel, electrode-graphene contacts and TG-uncovered graphene, respectively. The latter two terms are both extrinsic resistance (R_{ext}) from the two-probe measurement. The $R_{contact}$ is nearly fixed and the $R_{uncovered}$ changes with V_{BG}. Thus, the R_{ext} should be reasonably deducted in order to accurately estimate

the carrier mobilities. Here we employ the way of linear conductance fitting to deduct the R_{ext}.[R3] Figure S3a shows the TG-tuned resistance characteristics under varied V_{BG} from 6 to -6 V at a step of 3 V. Although the CNP shifts linearly with V_{BG}, the low resistance region behaves irregularly, reflecting the contribution of BG-tuned $R_{uncovered}$. Thus, we need to carefully deduct this contribution at different V_{BG}. Figure S3b displays the corresponding conductance behavior obtained from R_{tot} with and without 3-kohm R_{ext} deduction. Although the conductance curve at V_{BG}=-6 V becomes linear after the R_{ext} deduction, other curves are still sublinear. This means higher R_{ext} should be deducted under other V_{BG}. Figure S3c shows the mobility estimation with R_{ext} deduction of 5 kohm at V_{BG}=0 V. According to the linear fittings, the slopes of conductance are -0.25 and 0.44 mS/V for the hole and electron branches, respectively. Considering the channel aspect ratio of 6 and using the relation $\mathrm{d}\sigma / \mathrm{d}Vg = \alpha e \mu$,[R4] with $\alpha \approx 7.2 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ for the natural alumina dielectric, the hole and electron mobilities are estimated to be 1300 and 2300 cm^2/Vs, respectively. This indicates that there is no apparent mobility degradation of graphene below the natural alumina dielectric.

Reference

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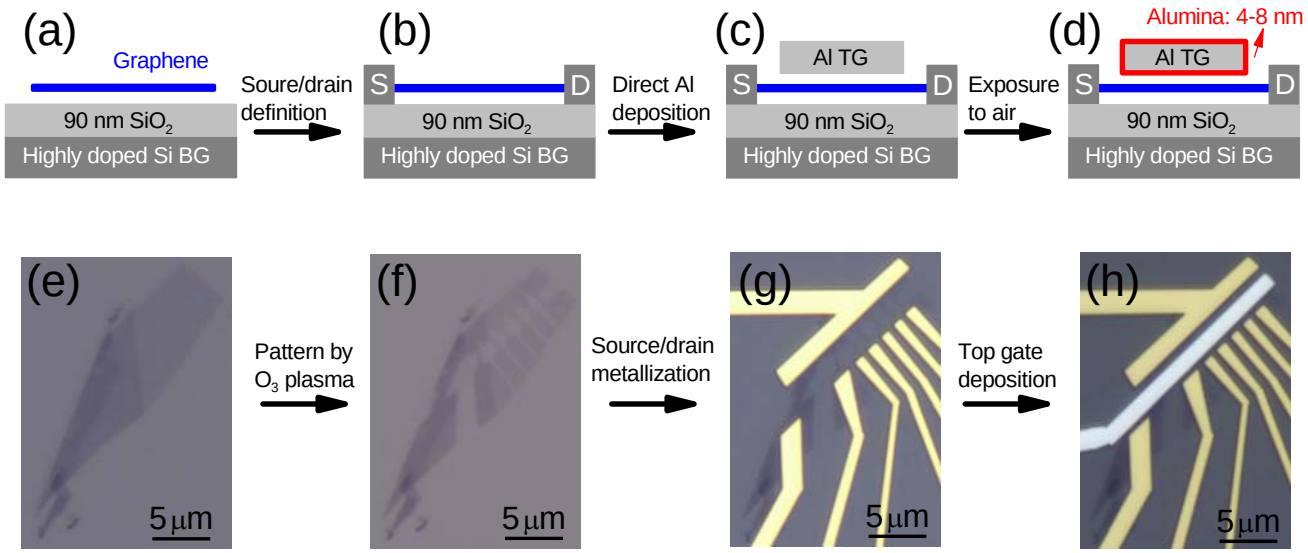

Figure S1. (a)-(d) Schematic flow of device fabrication. In this method the top gate stacks, including both the electrode and oxide dielectric layers, are fabricated by a one-step deposition of aluminum metal. (e)-(h) Typical optical images for a device at different process stages. In this device, seven FETs are defined in total, including five single-layer, one bi-layer, and one tri-layer FETs.

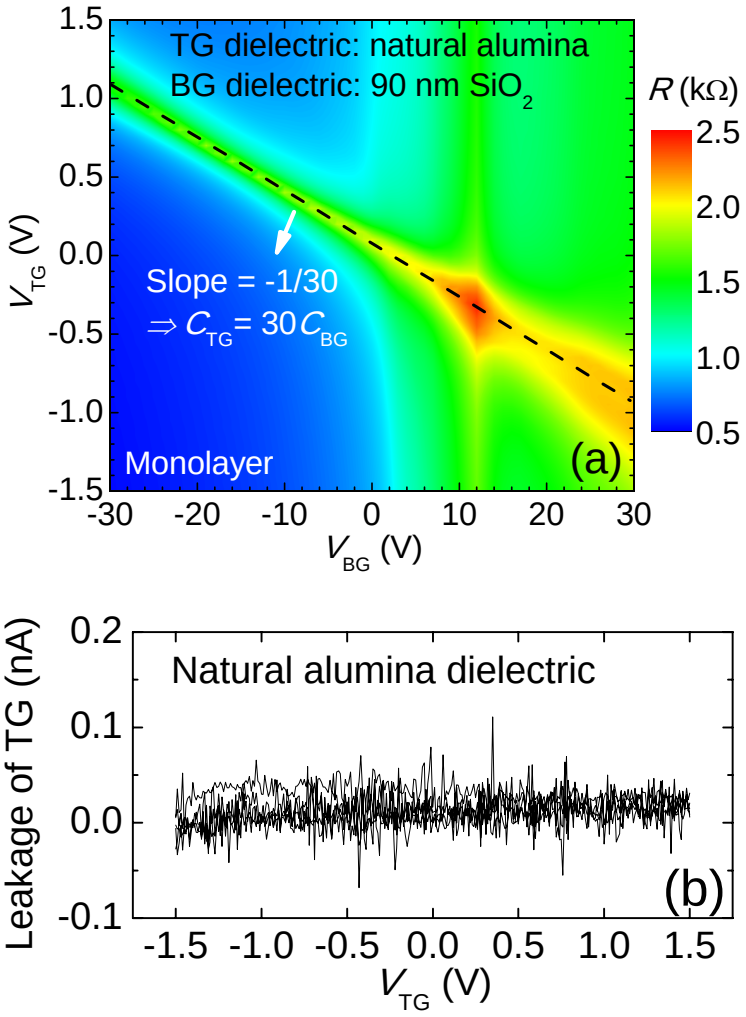

Figure S2. (a) Two-dimensional resistance plot versus V_{TG} and V_{BG} for a SLG FET. From the CNP trace, the capacitive efficiency of the thin natural alumina dielectric below TG can be estimated. (b) Leakage current monitoring of the TG through the alumina layer. The leakage is within 0.2 nA, indicating an excellent insulating property.

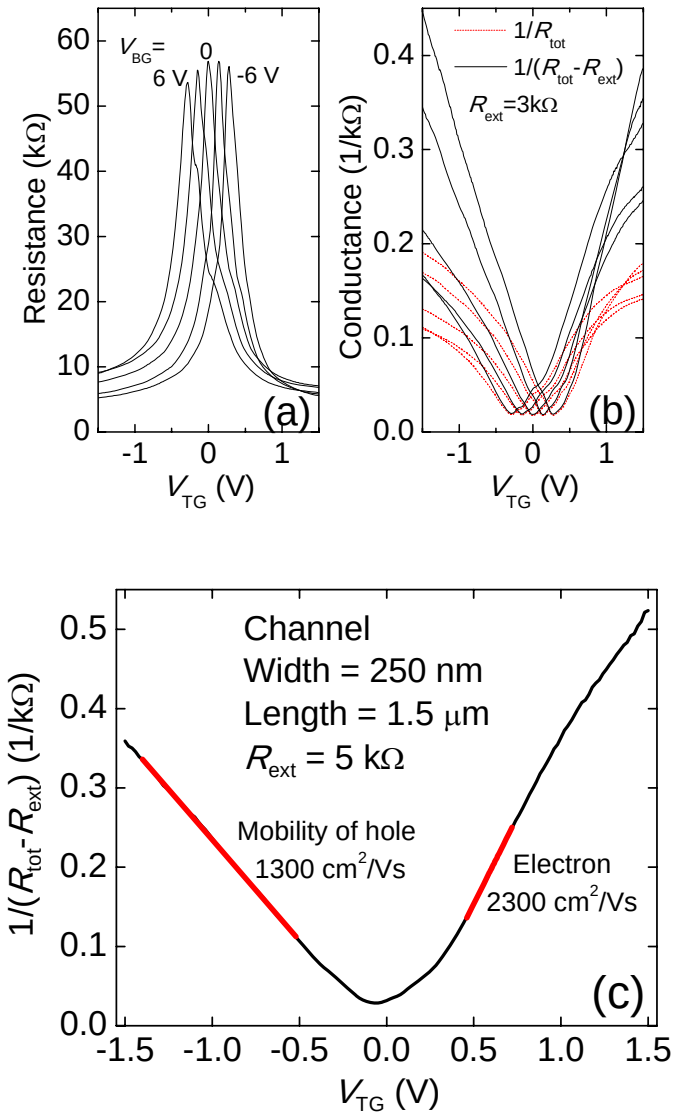

Figure S3. Estimation of carrier mobilities for the graphene channel underneath the natural alumina dielectric. (a) Resistance characteristics under varied V_{BG} from 6 to -6 V at a step of 3 V. (b) Corresponding conductance behavior with and without 3-kohm R_{ext} deduction. (c) Carrier mobility estimation for the channel at V_{BG}=0 V with a 5-kohm R_{ext} deduction. The estimated hole and electron mobilities are 1300 and 2300 cm^2/Vs, respectively.