Surface State Transport and Ambipolar Electric Field Effect in Bi_2Se_3 Nanodevices

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Supporting Information

Two-carrier surface-bulk model

To calculate the Hall voltage in magnetic field B in a general multiple-carrier model, one sums over the contributions of all carriers to the conductivity tensor σ^{tot}:

$$\sigma_{xx}^{tot} = \sum_i \frac{n_i e \mu_i}{\left(1+\mu_i^2 B^2\right)}; \quad \sigma_{xy}^{tot} = \sum_i \frac{n_i e \mu_i^2 B}{\left(1+\mu_i^2 B^2\right)}$$

Where the sum is over the carrier index i, n_i and μ_i stand for density and mobility of carrier i, respectively, and e is the absolute value of the electron charge. ρ_{xy} is the off diagonal element of $(\sigma^{\mathrm{tot}})^{-1}$. For two carriers:

$$\rho_{xy}(B) = -\frac{B}{e}\frac{\left(n_1\mu_1^2 + n_2\mu_2^2\right) + B^2\mu_1^2\mu_2^2\left(n_1+n_2\right)}{\left(n_1\mu_1 + n_2\mu_2\right)^2 + B^2\mu_1^2\mu_2^2\left(n_1+n_2\right)^2}$$

and for small B:

$$\rho_{xy}(B) = -\frac{B}{e}\frac{\left(n_1\mu_1^2 + n_2\mu_2^2\right)}{\left(n_1\mu_1 + n_2\mu_2\right)^2}.$$

It is common to use the Hall coefficient R_{H}:

$$R_H = \frac{\rho_{xy}}{B} = -\frac{1}{e}\frac{\left(n_1\mu_1^2 + n_2\mu_2^2\right)}{\left(n_1\mu_1 + n_2\mu_2\right)^2}.$$

When expressed in 3D units, n being a volume density, we substitute $n_1 = n_{\mathrm{bulk}}$, $\mu_1 = \mu_{\mathrm{bulk}}$, $n_2 = n_{\mathrm{surface}}/d$, $\mu_2 = \mu_{\mathrm{surface}}$:

$$R_H = -\frac{1}{e}\frac{\left(n_{bulk}\mu_{bulk}^2 + n_{surface}\mu_{surface}^2/d\right)}{\left(n_{bulk}\mu_{bulk} + n_{surface}\mu_{surface}/d\right)^2}.$$

Setting $\alpha = \mu_{\mathrm{bulk}} / \mu_{\mathrm{surface}}$ we finally arrive at Eq. 1 of the main text describing the dependence of $R_{\mathrm{H}}^{\mathrm{2D}}$ and $R_{\mathrm{H}}^{\mathrm{3D}}$ on d:

$$R_H^{2D} = -\frac{\left(n_{bulk}\alpha^2 d + n_{surface}\right)}{e\left(n_{bulk}\alpha d + n_{surface}\right)^2}; \quad R_H^{3D} = R_H^{2D} d$$

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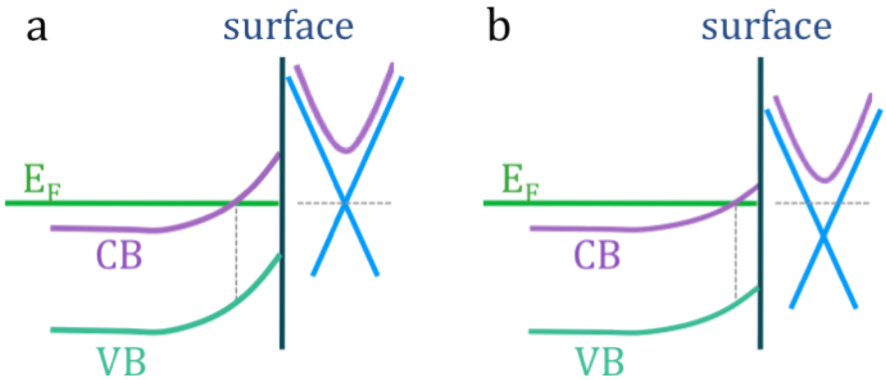

Figure S1: Sinultaneous charging of the bulk and surface states. (a) the dispersion of the bulk conduction band (purple) and surface states (blue), is drawn on the right. The position dependence of the bulk bands is plotted on the left. The surface state is tuned such that the Dirac point is at the Fermi energy. The bottom of the bulk band is at 0.2eV. The bulk bands bend near the surface, forming a depletion layer (vertical dashed line) (b) As a gate voltage is applied and charge is added the dispersions of both bulk and surface states are shifted downward. The change in the bulk dispersion results in a narrower depletion layer.

Simultaneous charging of bulk and surface

We noted in the main text that based on geometry considerations, presented in Figure 2, both bulk and surface channels contribute significantly to the electronic transport. Here we argue that such bulk contribution should be detectable also in gating measurements. We demonstrate that the surface and bulk have to charge together using the energy band diagram in Figure S1. When the surface denstiy is zero the Dirac point is at the Fermi energy (a). Since the bulk conduction band is 0.2eV above the surface Dirac point, it will have to be above the Fermi energy, and hence undergo band-bending from bulk to surface, resulting in a depletion layer. The thickness of the depletion layer could be in the order of 1nm for the bulk densities in our samples. Charging the surface states results in a downward shift of their dispersion with respect to the Fermi energy (b). The bulk dispersion shifts downwards at the surface and within the depletion layer, narrowing of the depletion layer and hence charging the bulk. The charge added by the applied gate voltage is therefore shared between the surface states and the bulk. Note that this is not a consequence of screening, but rather of the coupling of surface and bulk dispersions which reside in the same band-structure. Screening plays an additional role in determining the amount of charge induced at the surface versus the bulk.

Compilation of $\Delta G(V_{TG})$ Results

If the application of gate voltage modifies the charge of the bulk, this should have a signature in the field effect measurements presented in Fig 3. We can notice this effect in Figure S2, where we plot $\Delta G(V_{TG}) = G(V_{TG})\text{-}G(V_{min})$ measured for 7 different devices with HfO_2 dielectric, fabricated on the same sample from Ingot E. This data set included the devices discussed in the main text (Devices 1, 2 and 5 marked on the panels).

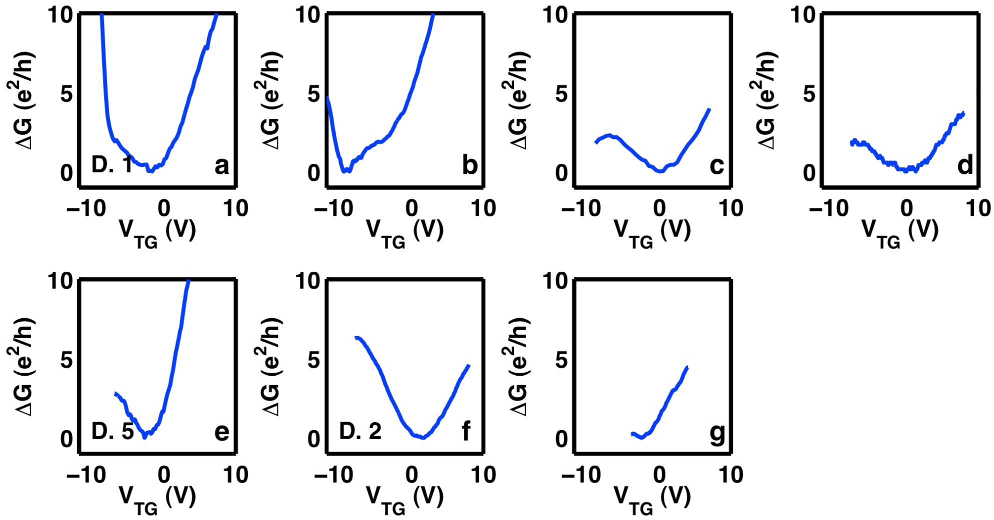

Figure S2: Collection of $\Delta G(V_{TG})$ of 7 devices fabricated from Ingot E. Devices 1, 2 and 5 discussed in the main text are marked.

If we symmetrize the data by subtracting a linear component from each data set (Figure S3) we find all the data sets are similar, with small variability of the minimal conductance feature around $V_{TG} \sim 0$V, and a typical slope $\Delta G/\Delta V_{TG}$. 2 out of the 7 devices exhibit a sharp increase in conductance at $V_{TG} \sim -8$V.

The conductance of each device can therefore be modeled as a sum of three contributions, assiciated with the bulk and both surfaces, where both the bulk and the top surface which on the gate voltage:

$G^{tot} = G^{bot} + G^{bulk}(V_{TG}) + G^{top}(V_{TG})$, where $G^{bulk}(V_{TG})$ is linear and $G^{top}(V_{TG})$ is ambipolar.

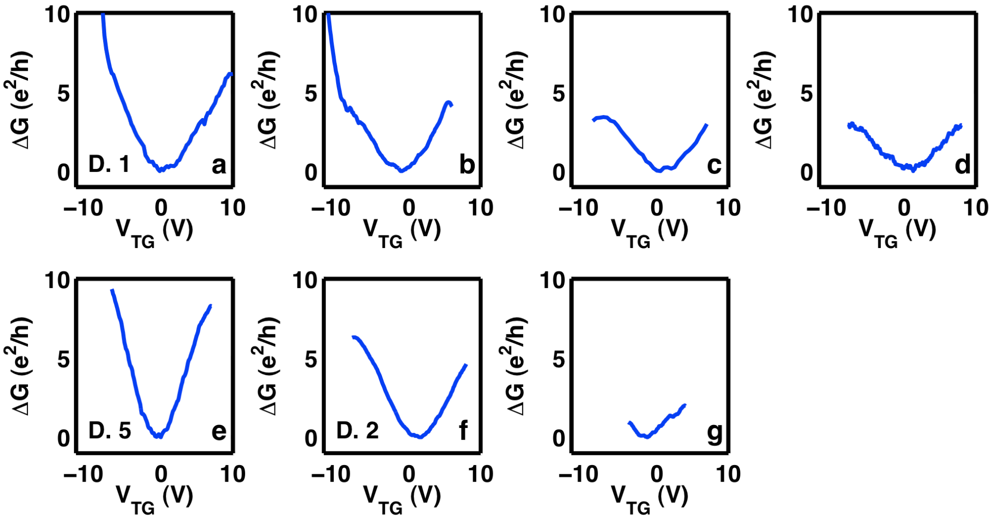

Figure S 3: The same ΔG(V_{TG}) scans presented in Figure S1, with a contant slope Gsl = SL×V_{TG} subtracted from each one.

To gain a quantitative estimate of the surface vs. bulk charging it is required to solve Poisson's equation within the depletion layer, accounting for all charge accumulated on the surface - including the topological states, metal-induced gap states, and all other surface defects. Precise accouting of all those surface effects requires a complex model which extends beyond the scope of this work. The slopes required to symmetrize each of the data sets presented in Figure S3 vary widely, and it is possible that this variability is related to differences in such surface details.

Possible origin of the sharp decrease in resistance at negative gate voltage

In some devices (e.g. D1 in Figure S3) a sharp increase in conductance appears at a negative gate voltage V_{TG} ~ -8 V. This feature is difficult to investigate since it appears near the limit of the voltage accessible by the top gate. One possible origin is that at negative voltage the valence band is pulled above the Fermi energy, forming an inversion layer where electrical transport is carried by holes in the bulk (Figure S4).

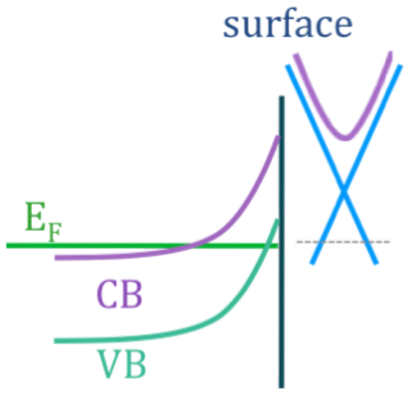

Figure S4: Inversion layer formed at the top surface by the application of negative top-gate voltage.