Supporting Information

Drastic control of texture in a high performance n-type polymeric semiconductor and implications for charge transport

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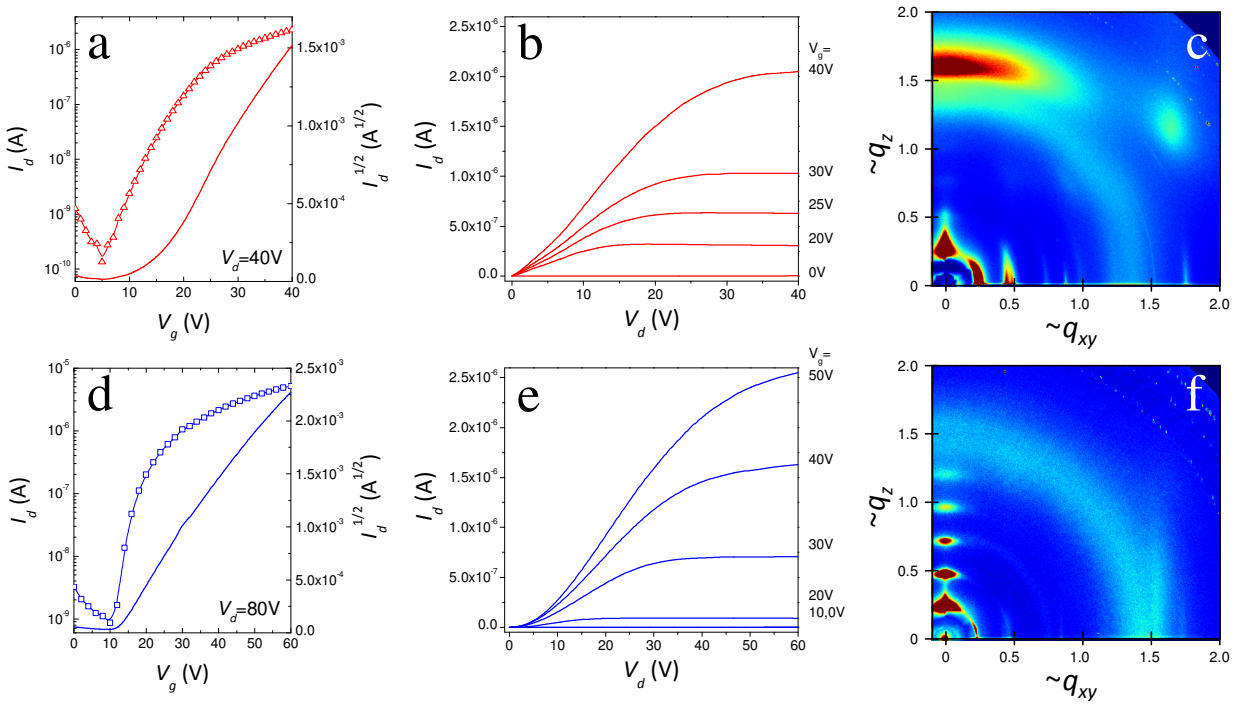
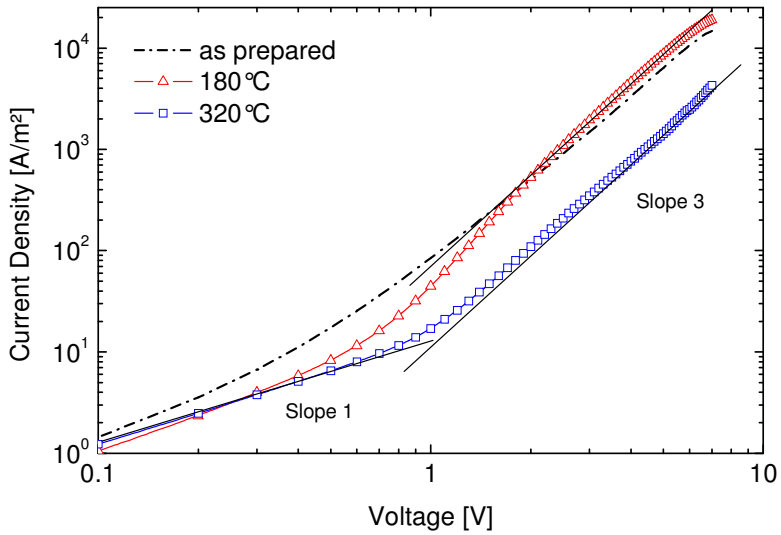
Table S1. Peak positions and widths for high resolution data presented in Figure 2 (top, middle) of P(NDI2OD-T2) films annealed below the glass transition temperature, and above the melting temperature.

Peak	Anneal (150ºC)		Melt anneal, (306ºC)	
	q_{peak}, Å^{-1}	w_{peak}, Å^{-1}	q_{peak}, Å^{-1}	w_{peak}, Å^{-1}
Grazing incidence (in-plane)				
(100)	0.251	0.020	*	*
(200)	0.500	0.038	*	*
(300)	0.745	0.053	-	-
(400)	1.00	0.08	-	-
(500)	-	-	-	-
(010)	-	-	1.58	0.14
(001)	0.455	0.037	0.490	*
(001)'	0.890	0.021	0.887	0.027
(002)'	1.771	0.033	1.766	0.030
Specular (out-of-plane)				
(100)	0.259	0.094	0.258	0.020
(200)	*	*	0.509	0.032
(300)	*	*	0.759	0.046
(400)	-	-	1.017	0.067
(500)	-	-	1.26	0.09
(010)	1.60	0.10	-	-

* peak is too weak or convoluted to determine peak position (or width).
- peak in question is not evident in diffraction pattern.



Supplemental Figure S1. TFT device testing. a-c) P(NDI2OD-T2) annealed to 150ºC; d-f), device melt annealed (310ºC). Transfer characteristics (a,d), output characteristics (b,e) for bottom gate, top contact TFTs. The morphological changes described in the main body of the paper are verified using GIXD (c,f).



Supplemental Figure S2 Current-Voltage Characteristics of P(NDI2OD-T2) electron-only devices (d=300nm).