Supporting Information

Carbon Nanotube Field Effect Transistors With Suspended Graphene Gates

Johannes Svensson, Niklas Lindahl, Hoyeol Yun, Miri Seo, Daniel Midtvedt, Yury Tarakanov, Niclas Lindvall, Oleg Nerushev, Jari Kinaret, SangWook Lee and Eleanor E. B. Campbell

1 Raman spectroscopy

Raman spectroscopy is used to verify that the graphene gates are single layered. A single Lorentzian can be used to fit the G'-band peak which is strong evidence that the graphene is single layered (figure S1)[1].

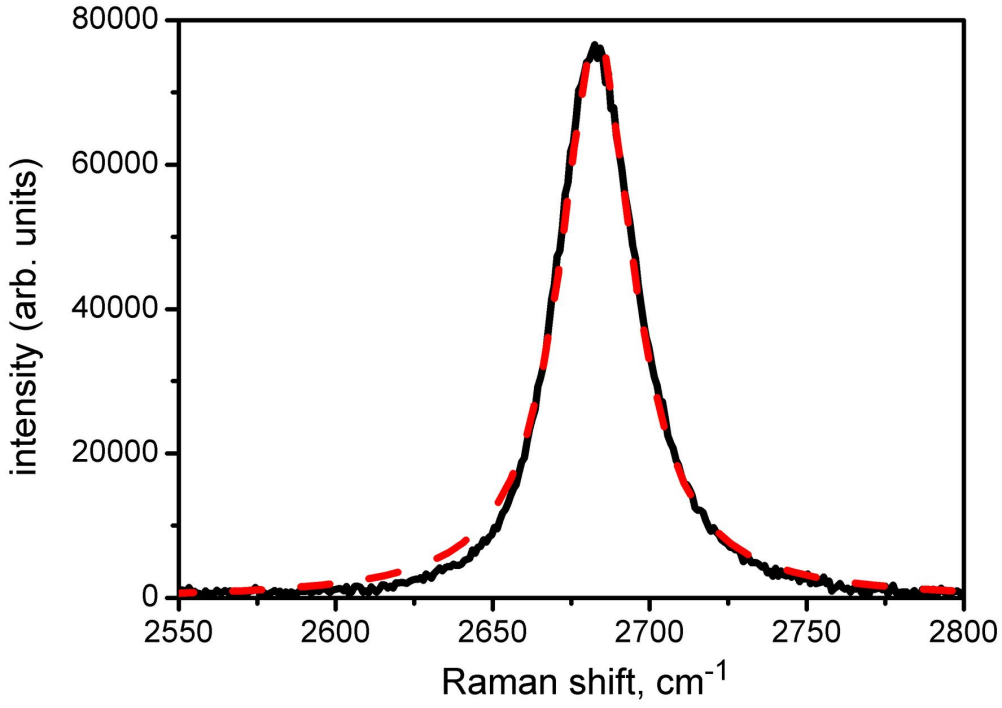

Figure S 1: *Raman spectrum of the graphene gate in the device in figure 3a obtained using a 514 nm wavelength laser. A single Lorentzian is used to fit to the G' peak (dashed red line).*

2 Electrostatic pull-in of graphene gate

If a sufficiently high voltage difference is applied between the graphene and the back gate, the attractive electrostatic force is stronger than the restoring force due to tension in the graphene [2]. For a device with few layered graphene suspended 170 nm over the CNT a gate voltage difference of 21 V results in a shift of the threshold voltage of 6 V and an improvement of the inverse subthreshold slope (figure S2a). AFM imaging of the device after electrical measurements reveal that the graphene has been irreversibly pulled down to the substrate surface (figure S2b).

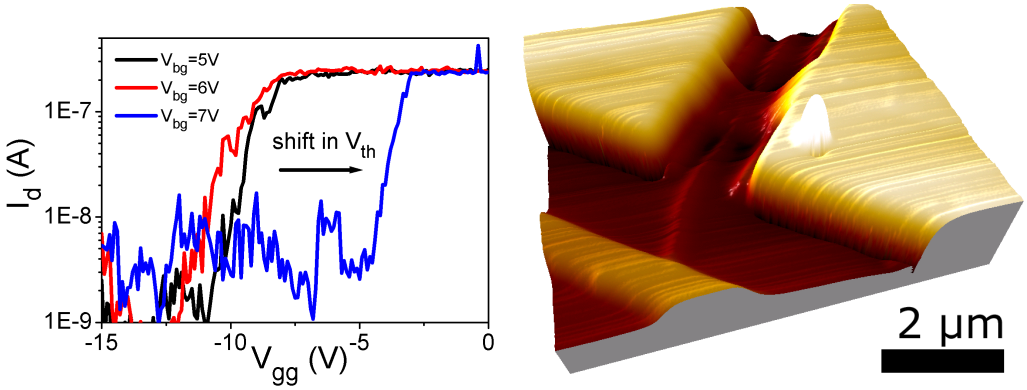

Figure S 2: *a) IV_{gg} characteristics at different V_{bg} obtained at room temperature in air with $V_d = 500$ mV for a CNTFET with a few-layered graphene gate. b) AFM height image of the device after electrical characterisation. The central part of the graphene gate has been pulled down to the substrate surface.*

3 Fabrication of test devices for electrostatic deflection of graphene

Single layered graphene flakes exfoliated from natural graphite and deposited on Si substrates with 295 nm SiO_2 are first located using an optical microscope. The graphene flakes are cut into beams of different length using an oxygen plasma with the beams protected by PMMA patterned by EBL. Top electrodes (3 nm Cr / 150 nm Au) are then patterned using EBL. Finally, 250 nm of the SiO_2 is etched in HF and subsequent critical point drying results in suspended graphene beams. Since HF etches SiO_2 quickly underneath graphene [2], the overlap between the beams and the electrodes are

designed to only be 300 nm to avoid a too large undercut which may cause the electrodes to collapse.

4 Simulations of electrostatic deflection of graphene and CNT transport

We have developed a theoretical model of the electromechanical operation of the CNTFET with a suspended graphene gate. The mechanics of the suspended graphene can be described within the elasticity theory for thin plates [3]. Within the out-of-plain approximation, the static vertical displacement of the graphene flake obeys the equation

$$T_0\nabla^2 u(x,y) + T_1\left(\partial_x\left(\partial_x u|\nabla u|^2\right) + \partial_y\left(\partial_y u|\nabla u|^2\right)\right) = -P_z(x,y), \quad (1)$$

where T_0 is the initial tension of the suspended graphene, $T_1 = 112$ N/m, u is the vertical displacement and $P_z(x,y)$ is the vertical external force per unit area exerted on the graphene.

The graphene gate is mechanically actuated by applying a voltage difference $\Delta V = V_{gg} - V_{bg}$ between the graphene and the back-gate electrode. The vertical component of the electrostatic force P_z per unit area of graphene at position $\mathbf{r}$ is given by

$$P_z(\mathbf{r}) = -\sigma(\mathbf{r})\partial_z\phi(\mathbf{r}), \quad (2)$$

where $\phi(\mathbf{r})$ is the electrostatic potential and $\sigma(\mathbf{r})$ the surface charge distribution [4]. These are connected through the integral Poisson equation

$$\phi(\mathbf{r}) = \frac{1}{4\pi\epsilon_0}\int_S \frac{\sigma(\mathbf{R})ds}{|\mathbf{R}-\mathbf{r}|}, \quad (3)$$

where the integral is taken over the surfaces of all conductors and ds is a small surface area of a conductor located at position $\mathbf{R}$ carrying the charge $\sigma(\mathbf{R})ds$ [4]. The boundary conditions for this equation are the values of ϕ on the surfaces of the conductors (V_{gg} and V_{bg} on the graphene gate and backgate respectively). It is important to note that upon deforming the graphene gate, the changed geometry of the system leads to a change of electrostatic potential and hence electrostatic force. Therefore, the force exerted on the graphene gate is a function of the deflection, $P_z = P_z[u(x,y)]$.

The electron and hole current densities in the semiconducting CNT are given by

$$j_n = \sigma_n\frac{\partial}{\partial x}\left(\frac{\xi}{e} - \phi_{scnt}\right) \quad (4)$$

$$j_p = \sigma_p\frac{\partial}{\partial x}\left(\frac{\xi}{e} - \phi_{scnt}\right), \quad (5)$$

where σ_n and σ_p are the electron and hole conductivities, respectively, ϕ_{scnt} is the electrostatic potential induced on the channel CNT, ξ is the chemical potential which is connected to the concentrations of electrons n and holes p through

$$\begin{aligned} n(\xi) =& \frac{8}{3\pi E_0} \int_{E_0}^{\infty} \frac{EdE}{\sqrt{E^2 - E_g^2}} \frac{1}{1 + e^{\frac{E-\xi}{kT}}} \\ p(\xi) =& n(-\xi) \end{aligned} \tag{6}$$

where the energy and the chemical potential are counted from the middle of the band gap, $E_0 = E_g/2$ where E_g is the bandgap width, and d is the diameter of the CNT.

In the case when no bias is applied along the channel CNT, the absent electric currents in equilibrium are equivalent to the condition

$$\xi - e\phi_{CNT} = C \tag{7}$$

where C is a constant. Since the CNT is connected to grounded leads, we have $C = 0$. The potential ϕ_{CNT} can be found from the Poisson equation (3) where the surface charge density on the CNT is given by $\sigma_{CNT} = \frac{1}{\pi d} e(p - n)$.

The system of equations (1), (3), (6) and (7) is solved numerically in a self-consistent way to obtain the deflection of graphene $u(x, y)$ and the concentration profiles $n(x)$ and $p(x)$ in the CNT. Equation (1) is solved using the finite element method and equation (3) using the boundary element method [5].

The conductance of the channel CNT is calculated from the carrier concentrations in the following way. The resistance ρ per unit length of a semiconducting CNT with the electron concentration n is given by

$$\rho(n) = \frac{1}{G_0 l_0} \frac{1 + \left(\frac{3\pi}{8} nd\right)^2}{\left(\frac{3\pi}{8} nd\right)^2}, \tag{8}$$

where $G_0 = 4e^2/h$ is the conductance quantum and l_0 is the scattering length in the CNT [6]. The total resistance R_{tot} and the conductance G of a CNT with a charge density distribution $n(x)$ can be found by dividing the CNT into small segments of length dx and noticing that these segments are connected in series, which yields

$$R_{tot} = G^{-1} = \left(\int_0^L \rho(n(x)) dx \right). \tag{9}$$

The hole conductance can be calculated from $p(x)$ using equations (8) and (9) with n substituted by p.

4.1 Scaling of inverse subthreshold slope

In order to assess the scaling of the inverse subthreshold slope S with the suspension height h and initial tension T_0 of the graphene gate, we have developed a lumped-parameter electrostatic model for the deflection of the graphene gate and the carrier concentration in the section of the channel CNT beneath it.

The inverse subthreshold slope gives the voltage needed to change the current in the channel by one order of magnitude, and can be calculated as

$$S = \left[\frac{\partial log\left(\frac{I_d}{I_0}\right)}{\partial V_{gg}} \right]^{-1}. \tag{10}$$

Assuming that the section of the channel CNT of length L_g electrostatically controlled by the graphene gate is uniformly charged with electron concentration n, we infer from equation (7) that the CNT is effectively kept at a uniform potential $\phi_{CNT} = \xi(n)/e$. Treating the system of the CNT and gates as a capacitive network, we write down the relation between the potential ϕ_{CNT} and the charge $Q = -enL$ in the CNT,

$$Q = C_{gg}(\phi_{CNT} - V_{gg}) + C_{bg}(\phi_{CNT} - V_{bg}) + \phi_{CNT}C_p, \tag{11}$$

which is easily transformed to

$$\phi_{CNT}(Q) - \frac{Q}{C_\Sigma} = \frac{V_{gg}C_{gg} + V_{bg}C_{bg}}{C_\Sigma}, \tag{12}$$

where C_{gg} (C_{bg}) is the capacitance between the channel CNT and the graphene gate (backgate), V_{gg} (V_{bg}) is the graphene gate voltage (backgate voltage) and $C_\Sigma = C_{gg} + C_{bg} + C_p$ where C_p is the parasitic capacitance of the CNT.

Since the switching of the transistor occurs when the channel CNT is depleted, we analyze the above expression in the limit of very small accumulated charge on the CNT. In this limit, equation (6) is reduced to

$$Q = Q_0 e^{\xi/k_B T}, \tag{13}$$

where $Q_0 = en_iL_g$, $n_i = \frac{8}{3\pi E_0 d}\int_{E_0}^{\infty} \frac{EdE}{\sqrt{E^2 - E_0^2}} \exp\left(-\frac{E}{k_B T}\right)$ is the intrinsic carrier concentration in a semiconducting CNT. This is used to express the potential in the CNT as a function of the charge Q as

$$\phi_{CNT}(Q) = \frac{\xi}{e} = \frac{k_B T}{e} log\left(\frac{Q}{Q_0}\right) \tag{14}$$

Inserting this into equation (12), we find that

$$\frac{k_B T}{e} log\left(\frac{Q}{Q_0}\right) + E_0 - \frac{Q}{C_\Sigma} = \frac{V_{gg}C_{gg} + V_{bg}C_{bg}}{C_\Sigma} \tag{15}$$

In the small charge limit $Q \ll Q_0$, the capacitive contribution to the total potential in the CNT $\frac{Q}{C_\Sigma}$ can be neglected, and the above equation simplified to

$$\frac{k_B T}{e} log\left(\frac{Q}{Q_0}\right) = \frac{V_{gg}C_{gg} + V_{bg}C_{bg}}{C_\Sigma} \tag{16}$$

Assuming that the current in the channel CNT is proportional to the carrier concentration in it, we can express S as a function of capacitances between the CNT and the gates, and voltages on the gates, as

$$S^{-1} = \frac{e}{k_B T \log(10)} \frac{\partial}{\partial V_{gg}} \left[\frac{C_{gg}V_{gg} + C_{bg}V_{bg}}{C_\Sigma}\right] \tag{17}$$

Taking the derivative with respect to V_{gg} in the above equation, and noticing that a change of V_{gg} leads to a displacement of the graphene gate and hence a change of C_{gg}, we come to the following expression for S

$$\frac{k_B T \log(10)}{e} S^{-1} = \frac{C_{gg}}{C_\Sigma}\left(1 + \frac{C'_{gg}C_{bg}}{C_{gg}C_\Sigma}\left(\Delta V + V_{gg}\frac{C_p}{C_{bg}}\right)\right) \tag{18}$$

where $C'_{gg} = \frac{\partial C_{gg}}{\partial V_{gg}}$. The first term in the above expression gives S of the static gate transistor, while the second term, summarizes the effect of the non-static gate. Note that assuming the full depletion of the channel, which is expressed by $C_{gg}V_{gg} + C_{bg}V_{bg} = 0$, the above equation can be reduced to $S = \frac{k_B T \ln(10)}{q} \frac{C_{tot}}{C_g + V_{gg}\partial C_{gg}/\partial V_{gg}}$, which yields equation (4) in the main article.

We note that (i) the first term is bounded by $\frac{C_{gg}}{C_\Sigma} < 1$, which results in a lower limit for S equal to $k_B T \log(10)/e$ known as the thermal limit, and (ii) since the graphene gate capacitance C_{gg} will increase when the graphene sheet is deflected, the second term will always be positive, meaning that the subthreshold slope will always be larger for a non-static gate transistor as compared to a static gate transistor. The developed model is used to determine the parameter ranges where the mechanical motion of the graphene gate reduces S below the thermal limit.

We model the capacitances between the CNT and the gates by analytical expressions for the capacitance between a cylinder and a metallic plate known from elementary electromagnetics,

$$C = \frac{2\pi\epsilon}{log\left(\frac{4H}{d}\right)} \tag{19}$$

where H is the distance between the plate and the cylinder, d is the diameter of the cylinder and ϵ is the dielectric constant of the surrounding medium. For C_{bg}, the distance H is equal to the distance between the CNT and the backgate while for C_{gg}, $H = h - u$, where u is the maximum deflection of the graphene gate. This deflection can be expressed through ΔV by an approximate relation

$$u = u_1 \Delta V^{\alpha} \tag{20}$$

where u_1 depends on the initial tension. For a completely linear graphene sheet, $\alpha = 2$ for deflections that are negligible compared to the distance between the graphene and the backgate. Mechanical nonlinearities cause α to decrease, so for small deflections we can assume $\alpha \lesssim 2$. This expression gives a good fit to both simulated and experimentally measured functions $u(\Delta V)$ and a derivative of the gate capacitance

$$C'_{gg} = \frac{\partial C_{gg}}{\partial u}\frac{\partial u}{\partial V_{gg}} = \frac{\alpha u}{\Delta V}\frac{\partial C_{gg}}{\partial u} \tag{21}$$

From equation (18) we see that S is a function of the gate deflection u, however for a given geometry and back gate bias, the switching of the transistor will occur at a specific gate voltage, and hence at a specific gate deflection. To find this deflection, we note that the switching occurs when the applied voltages deplete the channel CNT. As a result, the following condition holds to a good approximation,

$$V_{gg}C_{gg} + V_{bg}C_{bg} = 0, \tag{22}$$

which can be rewritten as

$$\Delta V = \frac{|V_{bg}|(C_{gg} + C_{bg})}{C_{gg}}. \tag{23}$$

Substituting equations (19), (20) and (22) into (18) we arrive to

$$\frac{k_B T \log(10)}{e} S^{-1} = \frac{C_{gg}}{C_{\Sigma}}\left(1 + \frac{C_{gg}\alpha u}{2\pi\epsilon(h-u)(1 + C_{gg}/C_{bg})}\right), \tag{24}$$

where C_{gg} is a function of the deflection u. This equation gives S as a function of the graphene suspension height h and the parameter u_1 which is a function of the initial tension of graphene T_0.

The scaling of S with the suspension height h and the initial tension T_0 calculated using the above equation is presented in Figure S3. The solid lines give S as a function of h with fixed initial tension values T_0 for each line, while the dotted lines give the same dependence with fixed ratios of

the maximum deflection u to the suspension height h. The ratio u/h which exceeds ~ 0.7 leads to irreversible pull-in and adhesion of graphene to the substrate [7], which is why combinations of S and h that lie below the line that corresponds to $u/h = 0.7$ are unattainable. The maximum suspension height at which an S below the thermal limit can be obtained without pull-in is therefore given by the intersection of the $u/h = 0.7$ line with the horizontal line that corresponds to $S/S_0 = 1$. This point is marked by arrows in the figures. The optimal value of initial tension T_0 is obviously such such that the curve $S(h)$ with $T = T_0$ goes through this point. Generally, lower T_0 allows for easier deflection of the graphene, resulting in a lower V_{gg} and hence higher S at the pull-in threshold.

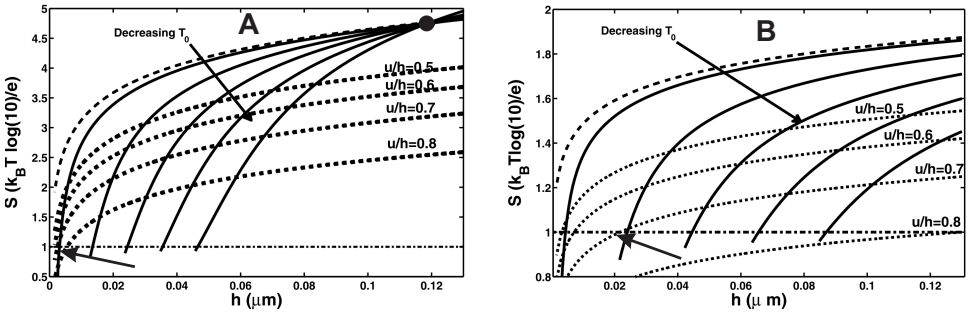

Figure S 3: *The inverse subthreshold slope S as a function of the graphene gate suspension height h. Solid lines correspond to different values of initial tension T_0 of the graphene sheet. Dashed lines show the scaling of S for the CNTFET with a fixed graphene gate. Dotted lines show the $S(h)$ dependence for fixed displacement to suspension height ratios, u/h. On both figures, thick arrows indicate maximum suspension heights where S below the thermal limit can be obtained without pull-in. In (A), the parasitic capacitance of the channel CNT was extracted by fitting S at $h = 120$ nm to the experimentally obtained value 286 mV/dec (indicated by a circle) for each initial tension. In (B), the parasitic capacitance is assumed to be zero.*

The results shown in Figure S3A are fitted to the experimental $S = 286$ mV/dec at $h = 120$ nm by choosing the parasitic capacitance level. These results reveal that due to considerable parasitic capacitance contributions, the suspension height would have to be reduced to 3 nm with an initial tension $T_0/T_1 \approx 0.45\%$ in order to obtain S below the thermal limit without pull-in.

On the other hand, reducing the effect of parasitic capacitances improves the scaling of S considerably. In Figure S3B, the scaling of S in the absence of parasitic capacitance of the channel is presented. As seen from the figure,

in order to obtain S lower than the thermal limit in this case, an initial CNT-graphene distance of 20 nm is sufficient. The corresponding initial tension in the case is $T_0/T_1 \approx 0.08\%$.

We note that there is a trade-off between a desired sharp response of the graphene sheet to the applied voltage and pull-in at large deflections. This balance is reflected in the existence of an optimal value of the parameter T_0. If the initial tension is higher than this value, the suspension height required to reach the thermal limit has to be reduced, and if it is lower, the graphene will always snap-in to the substrate before reaching the thermal limit.

References

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