Stretchable Graphene Transistors with Printed Dielectrics and Gate Electrodes

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Growth and transfer of graphene film layer by layers

Mono-layer graphene film was primarily grown on Cu foil (*t* ~25 μm, Alfa Aesar) by chemical vapor deposition in a 4inch quartz tube through typical growth process: i) load inner tubes in which copper foils insulted, into a 4inch outer tube to minimize temperature gradient;(pumping) ii) after remove the gas in the chamber by pump, heat the furnace up to 1000℃ with flow of 10 sccm H_2(89 mTorr). when the temperature reached to 1000℃, the Cu foil was annealed for 30 min to clean the surface of the foil by reduction of copper(II) oxide and grow the grain size; iii) The mixture of CH_4(15 sccm) and H_2(10 sccm) was injected to the tube for 30 min(310 mTorr); iv) except for flow of H_2, all the power and gas were turned off to cool the furnace under 100℃.

After synthesis of graphene, we stacked the graphene sheet layer by layer for a stretchable graphene device. Different from conventional methods, we transferred graphene directly on graphene grown Cu foil as shown below. Finally, we could fabricate three layers of graphene sheet without organic impurity among graphene layers.

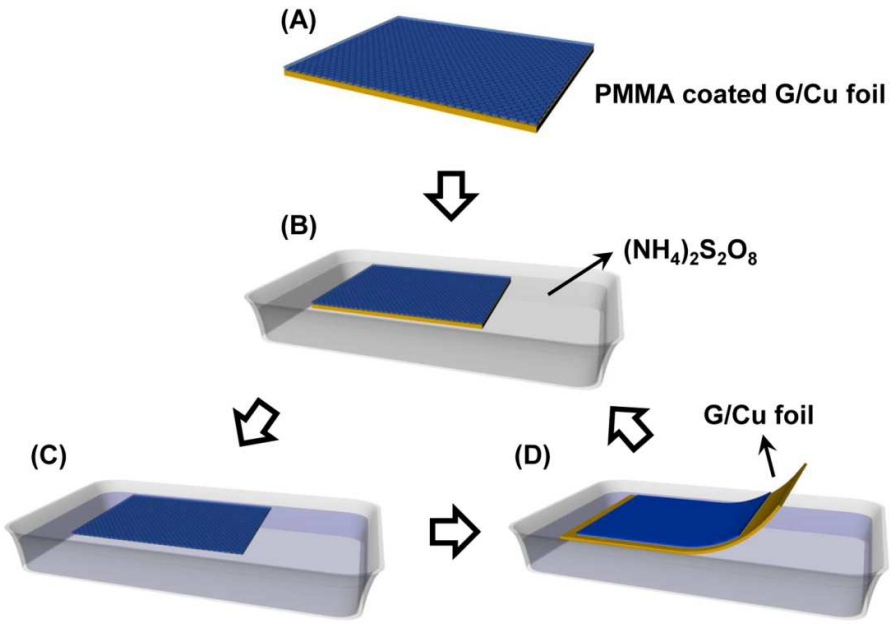

Figure S1. Schematic of direct transfer method. (A) Spin coating of PMMA as supporting layer after synthesis of graphene on Cu film. (B) Floating of the film on 0.1M $(NH_4)_2S_2O_8$ solution to dissolve the copper catalyst. (C-D) After removing the copper, lift up the PMMA/G film using another graphene grown Cu foil. Multiple stacked graphene sheet was fabricated by repeating from b) to d) process.

Device fabrication

A. Preparation of the patterned graphene on Cu foil

i) Transfer 3 layers graphene on Cu foil using direct transfer method.

ii) Remove the PMMA supporter by dipping the PMMA/3 layers-G(3L-G)/Cu foil in acetone at 80℃ to remove the PMMA residue.

iii) Attach the 3L-G/Cu foil on glass for easy handling.

iv) Pattern the source, drain and channel region using AZ1512.

v) Erase the exposed graphene by O_2 plasma for ~7 sec.

vi) Erase PR by dipping the sample in acetone.

B. Transfer of graphene on rubber substrate

i) Spin coat AZ 1512 on the patterned graphene/Cu foil as supporting layer instead of PMMA (500 rpm/5 sec, 3000 rpm/30 sec and curing in oven at 100℃ for 1min 30sec).

ii) Float the PR/patterned 3L-G/Cu foil on 0.1M $(NH_4)_2S_2O_8$ solution to dissolve the copper.

iii) Rinse (DI-water, ~10 min) the PR/patterned 3L-G film after removing copper and lift it up using PDMS substrate (t~1.5 mm).

iv) Dip the sample in acetone for 10 min to remove PR supporting layer.

C. Printing of ion gel and gate electrode using aerosol jet printer

i) Prepare ion gel ink by mixing poly(styrene-methyl methacrylate-styrene) (PS-PMMA-PS),1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) and ethyl acetate. The weight ratio is 0.1:0.9:9, respectively.

ii) Print the ion gel gate dielectric layer on channel region. As ion gel ink changed to mist state by ultra-sonication, it could be printed on target by control of atomizer and sheath gas for high resolution.

iii) PEDOT:PSS gate electrode was printed over the channel region.

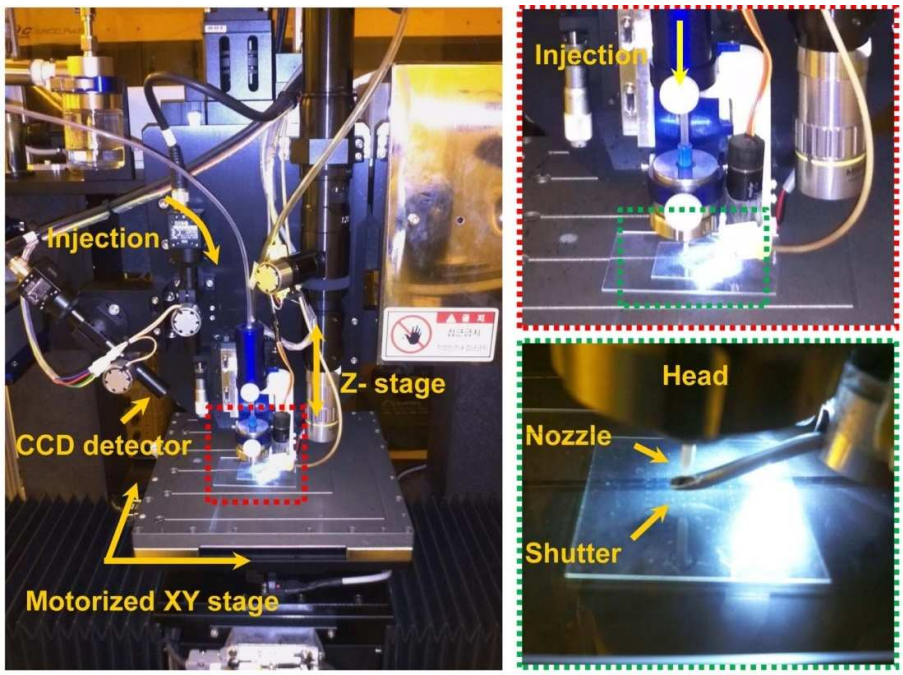

Figure S2. Aerosol jet printer for printing ion gel gate dielectric and PEDOT:PSS gate electrode.

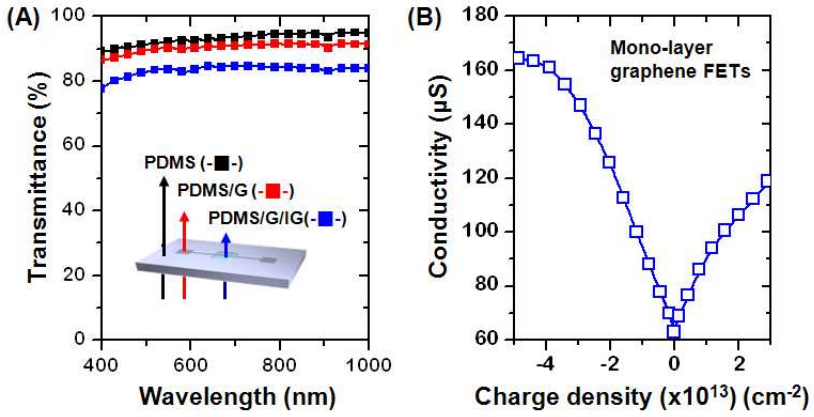

Figure S3. (A) UV-vis spectra of a poly(dimethylsiloxane) (PDMS) rubber substrates (black) with graphene source/drain electrodes (red) and an ion gel gate dielectric (blue). (B) Conductivity *vs.* charge density plots of the mono-layer graphene FETs fabricated on PDMS rubber substrate.

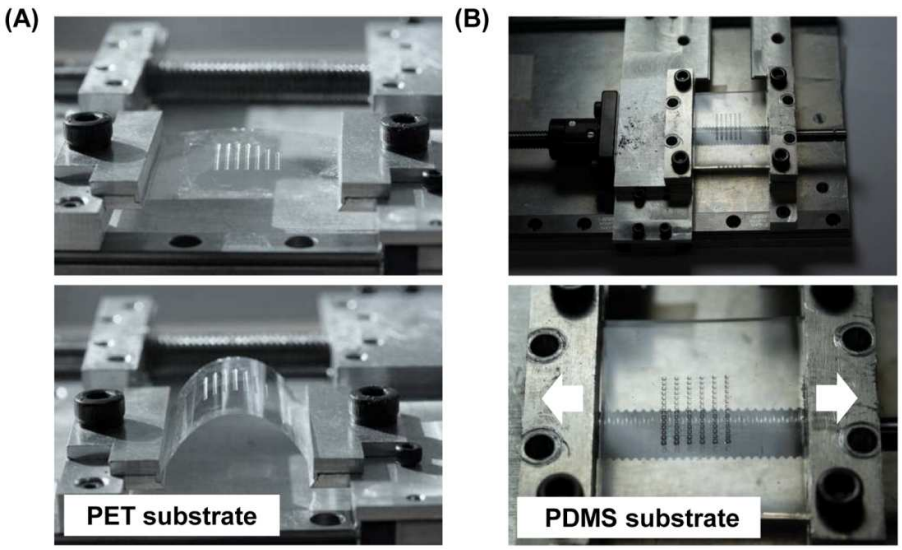

Figure S4. Home-built bending (A) and stretching (B) machine to measure the changes in the electrical performance of the ion gel-gated graphene FETs fabricated on polyethylene terephthalate (PET, t ~188 μm) and polydimethylsiloxane (PDMS, t ~1.5 mm) substrates.

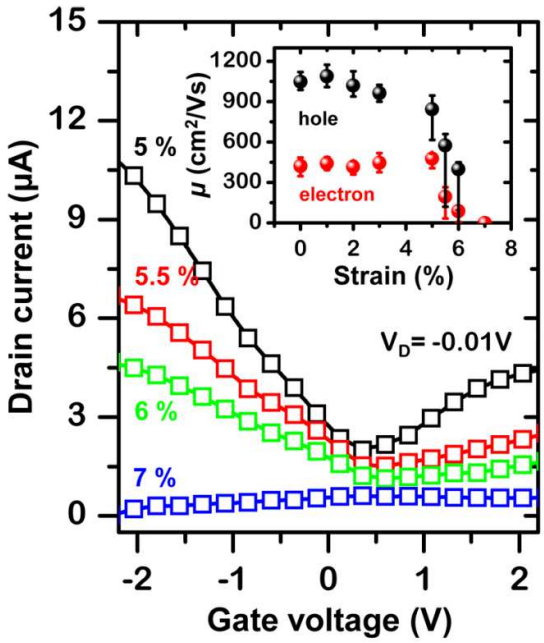

Figure S5. Transfer characteristics of tri-layer graphene FETs on PDMS substrates at strains in excess of 5% applied along the longitudinal direction of the channel. The inset shows the hole and electron mobilities of tri-layer graphene FETs as a function of the strain.

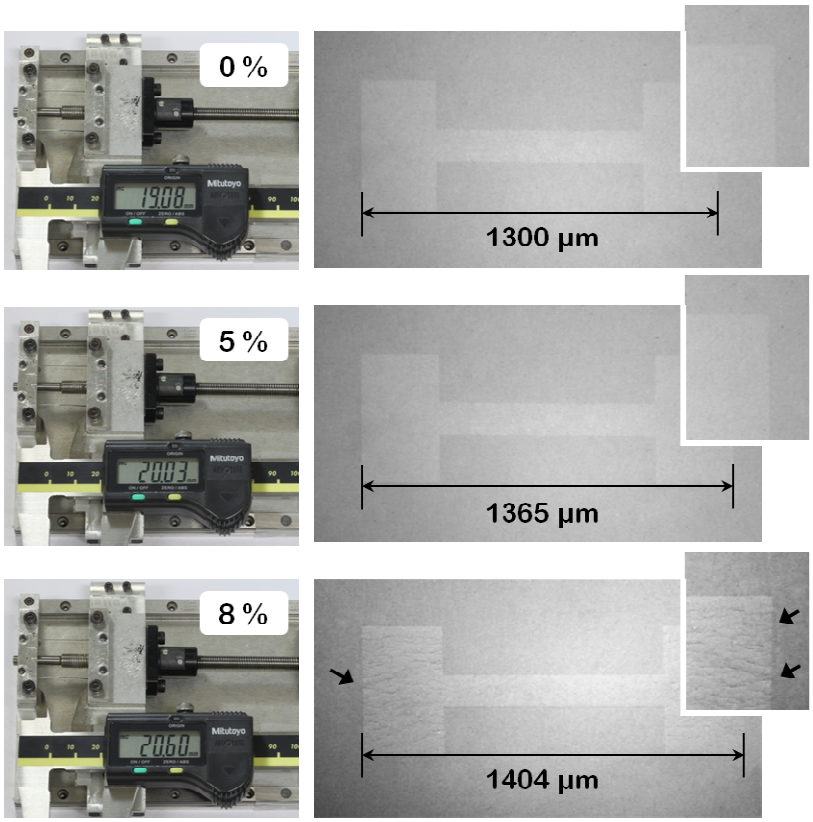

Figure S6. Optical microscope image of a graphene test structure under different uniaxial applied strains (0%, 5%, 8%). Under 5%, there is no significant non-uniform deformation at the channel or electrode regions. Strains of 8% lead to micro-cracking.