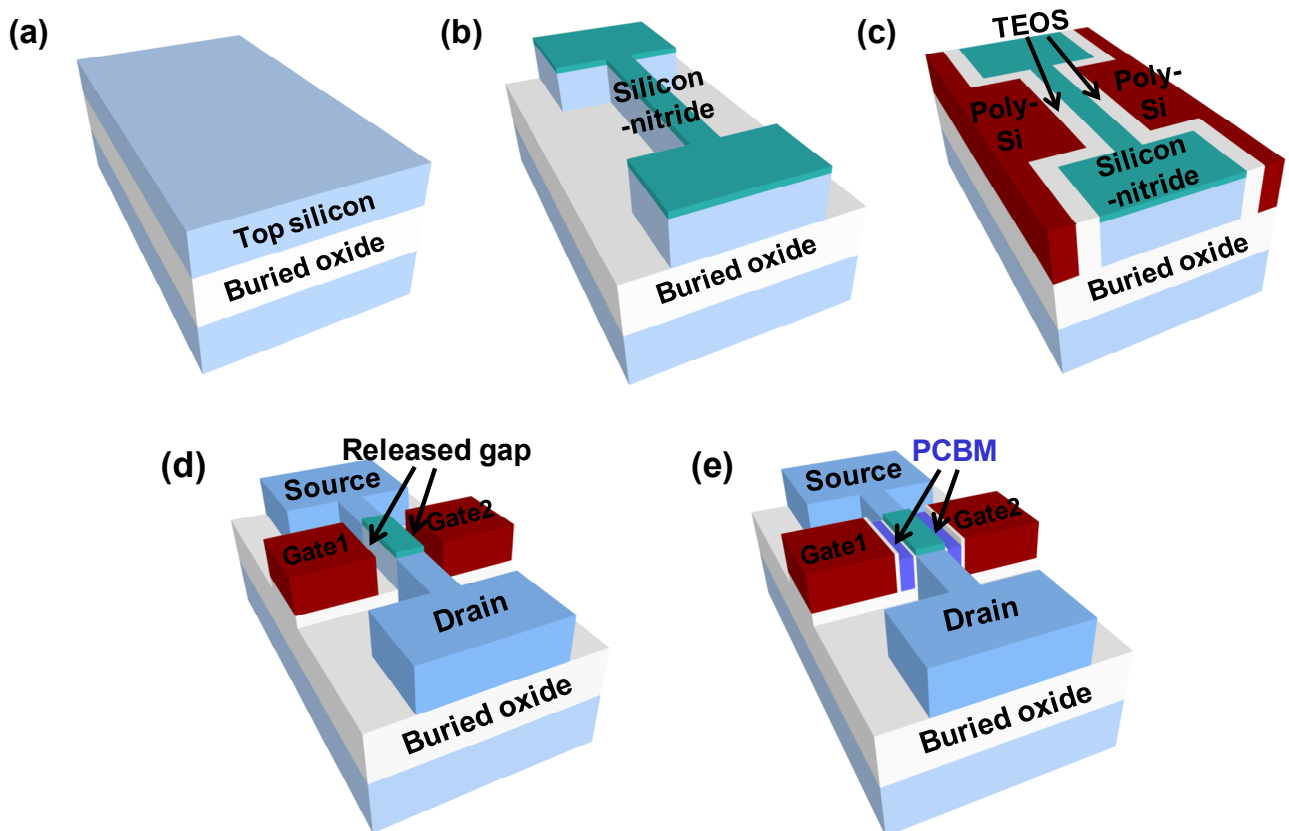# Supporting Information for "Photoactive Memory by a Si-Nanowire Field-Effect-Transistor"

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1. Process flow of the photoactive Si-NW device

Figure S1. The fabrication process flow of the photoactive Si-NW FET. (a) Starting SOI wafer (b) Deposition of silicon nitride as a hard mask and NW formation (c) Deposition of TEOS and poly-silicon, chemical-mechanical polishing (d) Gate patterning, source/drain implantation and nanogap creation by wet-etchant (e) Re-oxidation (white and thin layer) and PCBM dipping

2. Effect of white-light alone
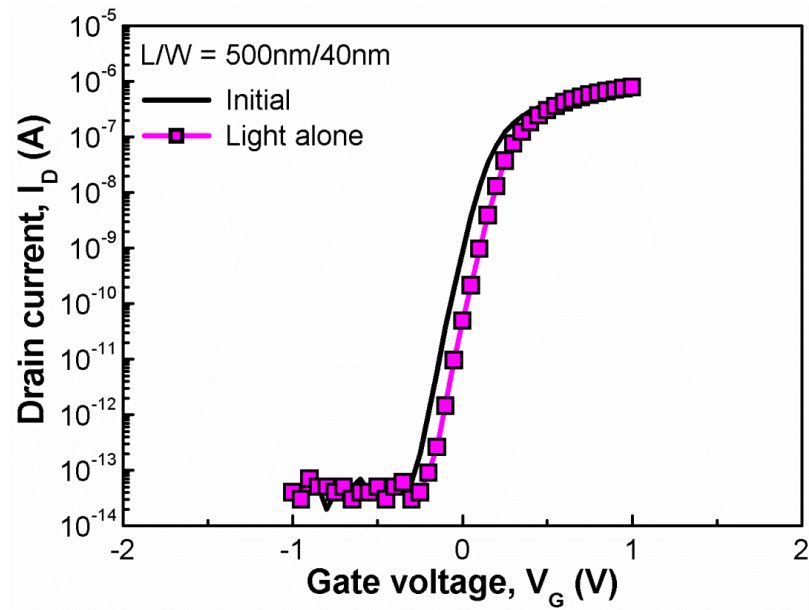
Figure S2. Comparison of I_D-V_G characteristic in a photoactive Si-NW FET before and after applying white light alone.

3. Device scalability according to the gate mode

(a)

(b)
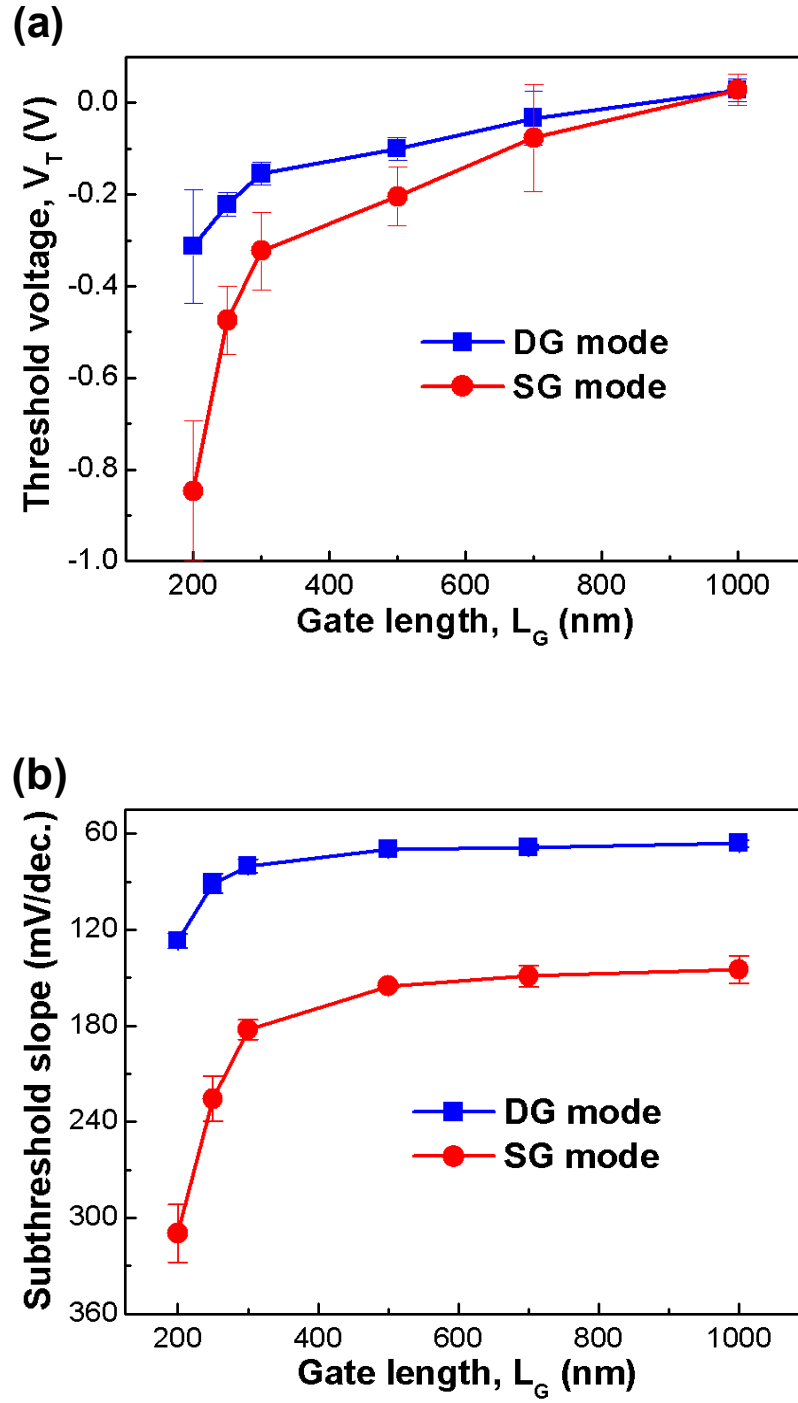
Figure S3. (a) V_T change and (b) subthreshold slope to investigate the immunity against short-channel-effect according to the gate length for SG and DG modes

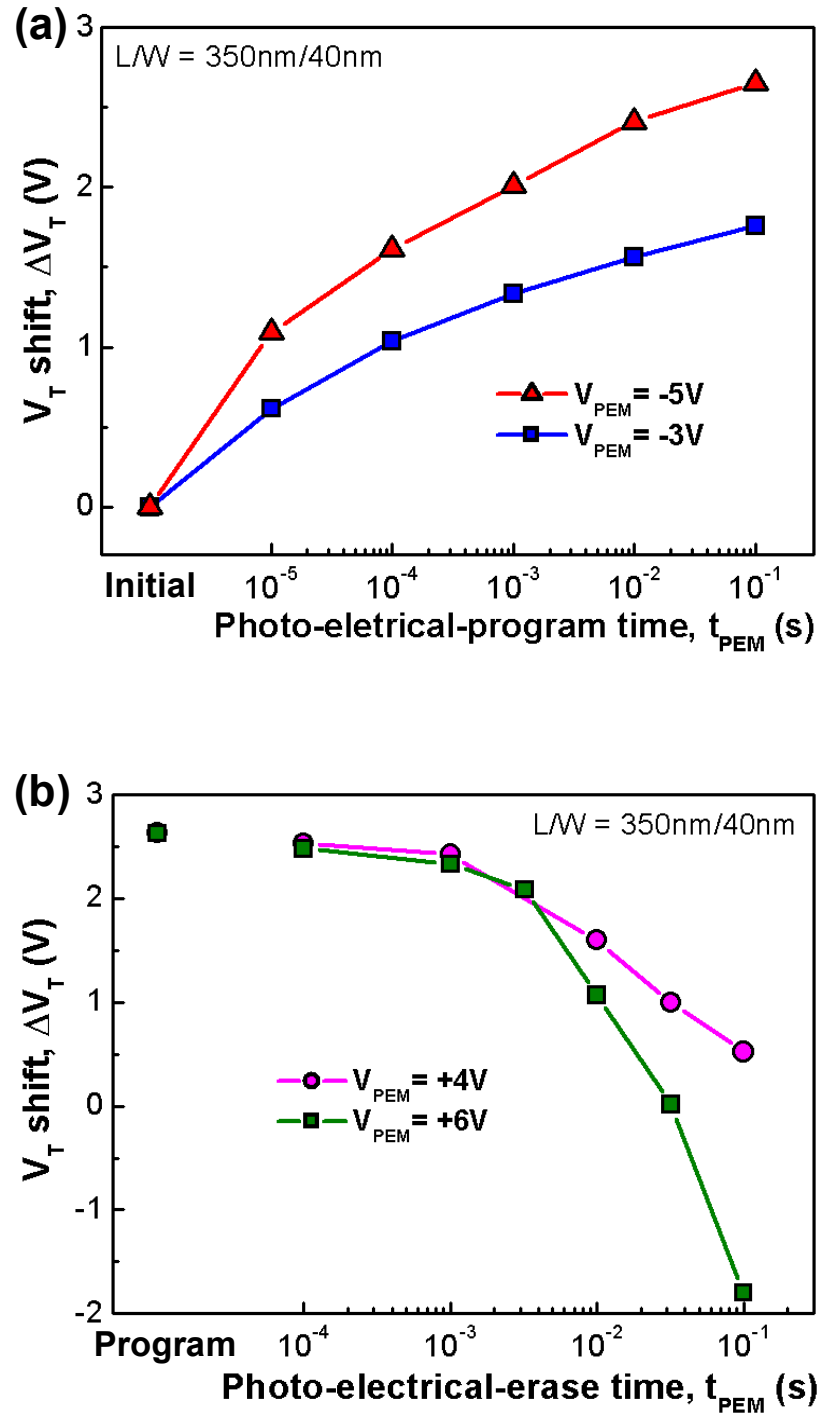## 4. The program and erase characteristics in Si-NW photoactive memory

Figure S4. (a) Program and (b) erase speed characteristics
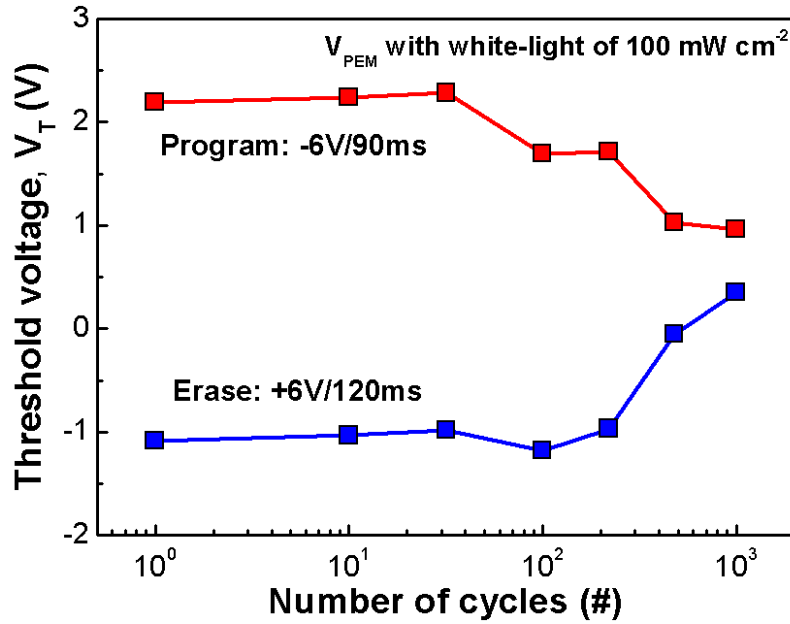
5. Repeatability characteristics

Figure S5. Repeatability characteristics after program/erase cycles

6. Simulation proof of independently-controlled double-gate structure

Figure S6 explains the mechanism of the independently-controlled gate. Using a commercially available numerical simulation,[1] the charges are artificially distributed and the resultant V_T is extracted. If the charges are located close to the drive gate, as shown in Figure S6a, they only contribute to the V_T shift, proportional to the increased charge amount, similar to a typical Flash memory (Figure S6c). It should be noted that the V_T shift is not influenced by Gate 2 bias, because all the charges are located at the side of the drive gate. If the charges are located close to the opposite gate (*i.e.*, the supporting gate) (Figure S6b), however, the V_T does not follow this kind of linear behavior. First, as shown in Figure S6c, the V_T increases faster than the case of charges close to the drive gate, and is then gradually saturated. This V_T trend is the same as the V_T change, which is read with the SG mode before photo-electrical-

program, according to the Gate 2 bias shown in Figure S6d. In other words, charges close to the supporting gate play a role as a negatively-biased gate, *i.e.,* negative optical gating.[2] Through the DG photo-electrical-program, charges are generated at both sides of PCBM simultaneously, and these charges result in a synergetic V_T shift, which is the combined effect of charges at each side, with the aid of the independent gate structure.
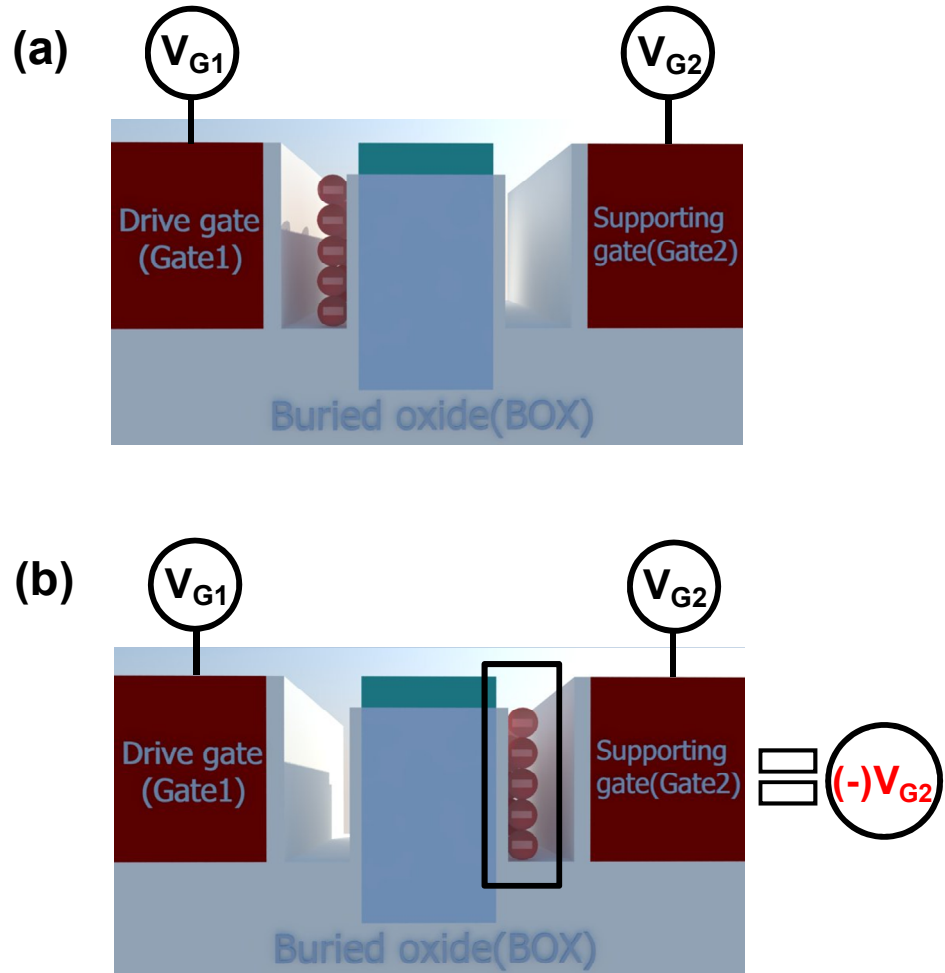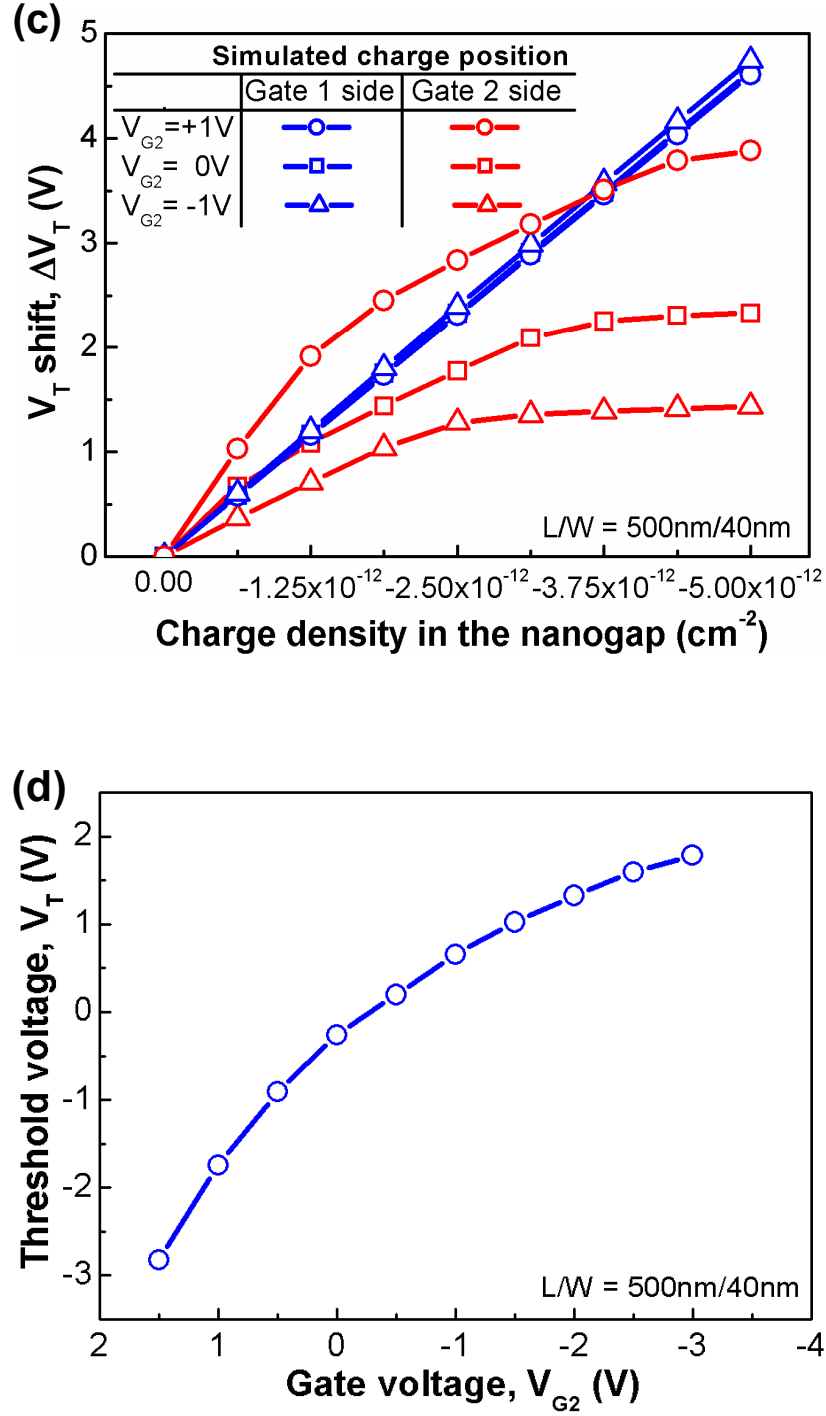
Figure S6. Schematic of the charges located close to the (a) drive gate and (b) supportive gate. The charges in the case of (b) play the part of a negatively biased supportive gate. (c) V_T read margin according to the charge amount to verify the role of each gate according to the position of charges implemented with numerical simulations. (d) V_T change according to Gate 2 voltage in the photoactive Si-NW FET read with the SG mode before the photo-electrical-program.

REFERENCES

(1)   ATLAS User's Manual. *SILVACO Inc.*, CA, **2008**.

(2)   Borghetti, J.; Derycke, V.; Lenfant, S.; Chenevier, P.; Filoramo, A.; Goffman, M.; Vuillaume, D.; Bourgoin, J. P. Optoelectronic Switch and Memory Devices Based on Polymer-Functionalized Carbon Nanotube Transistors. *Adv. Mater.* **2006**, *18*, 2535-2540.