

Supporting Information

Ambipolar MoS₂ Thin Flake Transistors

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This supporting information contains:

- 1. Flake thickness identification**
- 2. Surface morphology**
- 3. Transfer characteristics of thin flakes**
- 4. Equivalent circuit of EDLT device**
- 5. Hall effect measurement**

Figure S1 to S5

1. Flake thickness identification

MoS₂ thin-flake electric double layer transistors (EDLTs) were fabricated on transparent sapphire substrates. Using sapphire to replace traditional SiO₂/Si substrates allowed us to make a quick estimation of the thickness and better identification of the uniformity of the flakes after mechanical exfoliation, based on the observation of light transmittance (shown below). Apart from the flake thickness, uniform surface is also quite important in EDLTs since transistor channel is formed at the surface of the flakes.

To establish the relationship between the transmittance and thickness of the flake, we first measured the thickness by an atomic force microscope (AFM) and compared with optical microscope (OM) images taken under transmission mode, for many exfoliated MoS₂ thin flakes. Figure S1 (a) shows OM images and thickness profiles along red solid lines measured with AFM. Next, we analyzed OM images, extracted the transmittance, the ratio $I_{\text{flk}}/I_{\text{sub}}$ of light intensity transmitted through the flakes and the substrate, for red, green, and blue channels. The value $I_{\text{flk}}/I_{\text{sub}}$ is plotted as a function of thickness (Figure S1 (b)).

This color code served as a guidance to identify sample thickness and suitable flakes for device fabrication. As shown in Figure S1 (b), the change of thickness can be easily identified when the flake is less than 30 nm in thickness, where the transmittance changes significantly with the change of thickness. In the reflection mode, on the other hand, it is more difficult to identify the

non-uniform profile in flakes thicker than 10nm. As shown in Figure S1 (c), the color contrast under transmittance mode is much larger than that under reflection mode.

2. Surface morphology

Figure S2 shows AFM images and surface morphology of bulk (a and b) and thin flake (c and d) samples after the fabrication process. In the AFM image of the thin-flake sample, there are several red colored areas as marked by black lines (Figure S2 (c)). These features are ascribed to e-beam resists after the micro-fabrication process. However, the highest conductivity (at $V_G = 3V$) is almost independent of sample thickness (Figure S2 (e)), indicating that the conduction channel is formed only near the top surface, and that those residues do not seriously affect the transport properties.

3. Transfer Characteristics of thin flakes

We measured several devices with different flake thicknesses as shown in Figure S3. The ambipolar characteristics were observed for all thin flake samples up to a thickness of 25 nm. While the “ON” state conductivity is almost unchanged for the electron accumulation, the “OFF” state conductivity decreases dramatically with decreasing of flake thickness. This tendency can be explained by the decreasing of the transport contribution from the inside beneath the channel surface as discussed in section 4 of this Supporting Information.

4. Equivalent circuit of the devices

As shown in Figure 2, transport properties of bulk and thin-flake EDLTs are significantly different. In the transfer curve (I_{DS} vs V_G), we observed on/off ratios of 4 and 7 for bulk and thin flake samples, respectively, whereas, in the gate voltage dependence of conductivity (σ_{2D}), the on/off ratio of the thin flake sample is much larger than that of the bulk sample. To understand these differences, it is quite useful to consider an equivalent circuit shown in Figure S4. This equivalent circuit is composed of contact resistances (R_C), in series with two parallel resistances; namely R_S and R_B . R_S and R_B represent the contribution from channel surface (1~2 atomic layer thick) due to the field accumulation of carriers, and inside resistance of the sample beneath the channel, respectively. R_B is assumed to be independent of gate bias (V_G).

First of all, the sheet conductivity, contributed by R_S and R_B in parallel, is not affected by the R_C since we performed a 4-probe measurement. In the “OFF” state, the main contribution comes from inside resistance because the contribution of charge accumulation at channel is negligible and current flows through the whole sample. We can calculate the sheet resistivity $\rho_{2D, \text{off}}$ from the gate voltage dependence of sheet conductivity σ_{2D} (Figure 2 (b)). We obtained $\rho_{2D, \text{off}} = 568 \text{ k}\Omega$ for thin flake device and $\rho'_{2D, \text{off}} = 1.49 \text{ k}\Omega$ for bulk device, The large difference of “OFF” state sheet resistivity is attributed to the thickness of the sample. If we assume similar 3-dimensional conductivities for both thin flake and bulk samples, then the thickness of bulk sample will be ~400 times larger than that of

thin flake sample, reaching the order of ~ 10 micrometer. This agrees fairly well with the real thickness of our bulk device.

For the bulk sample, the fact that $\rho'_{2D,off} = 1.49 \text{ k}\Omega$ is comparable to $\rho_{2D,on} = 0.64 \text{ k}\Omega$ indicating that contribution of $\rho'_{2D,inside}$ must be taken into account even at “ON” state. Therefore on/off ratio of bulk sample is mainly limited by the small “OFF” state resistance. In thin flake devices, on the other hand, $\rho_{2D,off} = 568 \text{ k}\Omega$ is much larger than $\rho_{2D,on} = 2.35 \text{ k}\Omega$, indicating the inside contribution in the “ON” state is negligible. Since the inside contribution to the transport cannot be ignored in the bulk sample even at “ON” state, it is more appropriate to consider relative increases of conductivities rather than on/off ratios themselves when we compare bulk and thin flake devices. The relative increases of conductivities can be mainly ascribed to the change of transport of the channel surface. From Figure 2 (b) we get $\Delta\sigma_{2D} = 0.4 \text{ mS}$ and $\Delta\sigma'_{2D} = 0.7 \text{ mS}$ for thin flake and bulk sample, respectively. These two values are in the same order and in good agreement with the previous analysis.

From the transfer curve (Figure 2(a)), we can calculate the contact resistance R_C by knowing the R_S and R_B . For bulk sample R_C is $15 \text{ k}\Omega$ (“ON” state) and $67 \text{ k}\Omega$ (“OFF” state), while for thin flake sample R_C is $26 \text{ k}\Omega$ (“ON” state) and $57 \text{ k}\Omega$ (“OFF” state). The R_C of “ON” state is more than one order of magnitude larger than R_S of both bulk and thin flake samples. Hence, I_{DS} (and on/off ratio of I_{DS}) is limited by contact resistance for both samples,.

5. Hall effect measurement

We performed Hall effect measurement under magnetic field B up to 9 Tesla to confirm carrier polarity and sheet carrier density n_{2D} . In Figure S5 anti-symmetrized Hall resistance R_{xy} is plotted as a function of external magnetic field B . Dashed lines in the figure are linear fitting of the plot. The $(dR_{xy} / dB)^{-1}$ clearly changes its sign as a function of gate voltage V_G , indicating that carriers under positive and negative V_G have different polarity, hence we confirm both electron and hole operation were realized by switching V_G .

Captions

Figure S1 (a) Optical micrographs of mechanically exfoliated MoS₂ thin flakes and AFM identification of their thickness profile. (b) Transmittance $I_{\text{flk}}/I_{\text{sub}}$ for red, blue, and green channels as a function of thickness of the flake. Broken lines are guides for eyes. (c) Comparison of optical micrograph taken under reflection (left panel) and transmission (right panel) modes. Surface profile can be identified more clearly under transmission mode.

Figure S2 (a) AFM image of a bulk sample surface. (b) Surface morphology along the red line in panel (a). (c) AFM image of a thin flake sample after a complete micro-fabrication process. Possible area with residues of e-beam resists are circled by black lines. (d) surface morphology along the red line in (c). (e) Sheet conductivity at gate bias 3V vs. flake thickness for several samples.

Figure S3 Transfer characteristics of thin flakes with various thicknesses determined by AFM. Ambipolar operation of the devices was observed in all thin flake samples.

Figure S4 Equivalent circuit of EDLT devices. The circuit used to bias thin flake transistors is composed of two parallel resistances R_S and R_B , in series with contact resistance (R_C). Due to the existence of transport through the inside of the sample, R_B of bulk sample is comparable to R_S of

channel surface so that on/off ratio in sheet conductivity is much smaller than that of thin flake sample. For both bulk and thin flake samples, maximum I_{DS} is mainly limited by R_C .

Figure S5 Hall effect measurement of carrier accumulation on a thin flake MoS₂ EDLT. Hall resistance R_{xy} is anti-symmetrized and plotted against magnetic field B . Change of sign of linear fittings (dashed lines) indicates the change of carrier polarity with gate voltage. In both electron and hole accumulation, the maximum carrier density ($|V_G| = 3$ V) is in the order of $\sim 10^{14}$ cm⁻², which is more than one or two order of magnitude larger than the capability of traditional FETs.

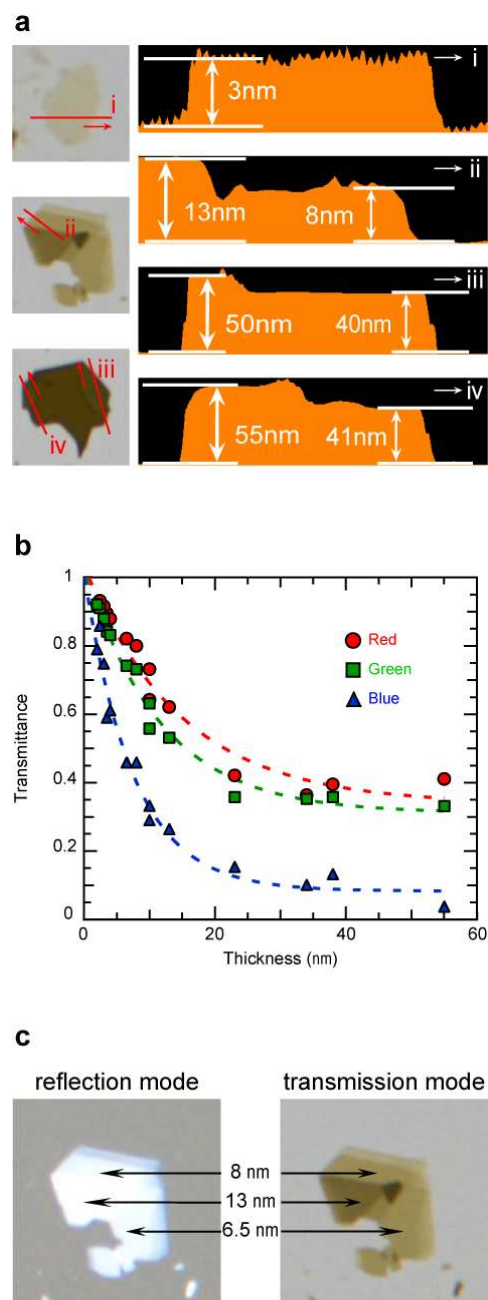


Figure S1

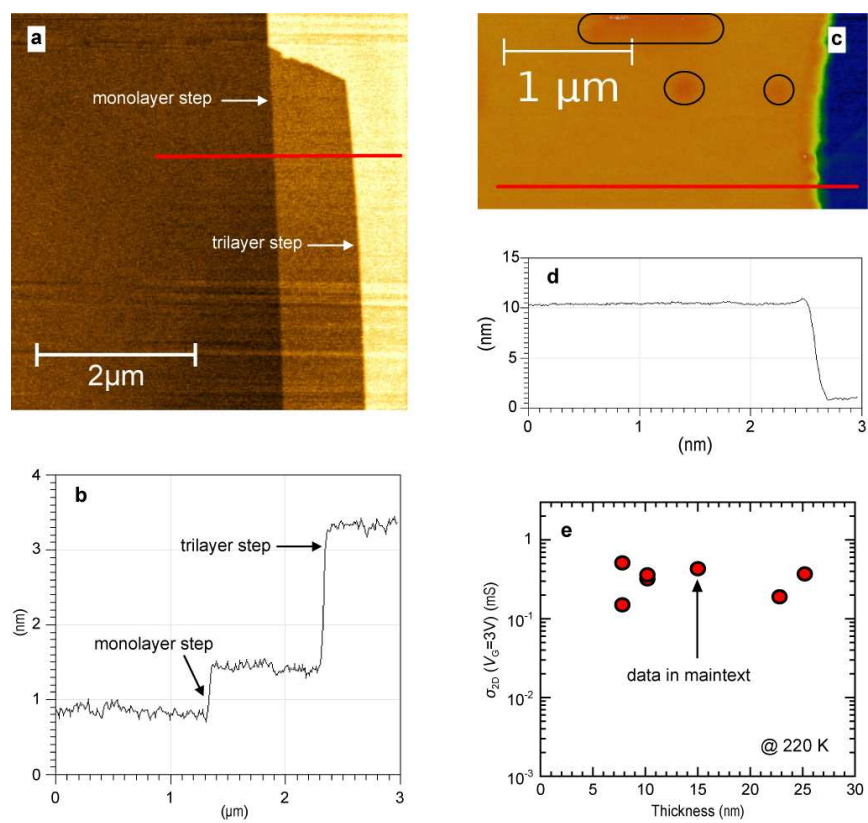


Figure S2

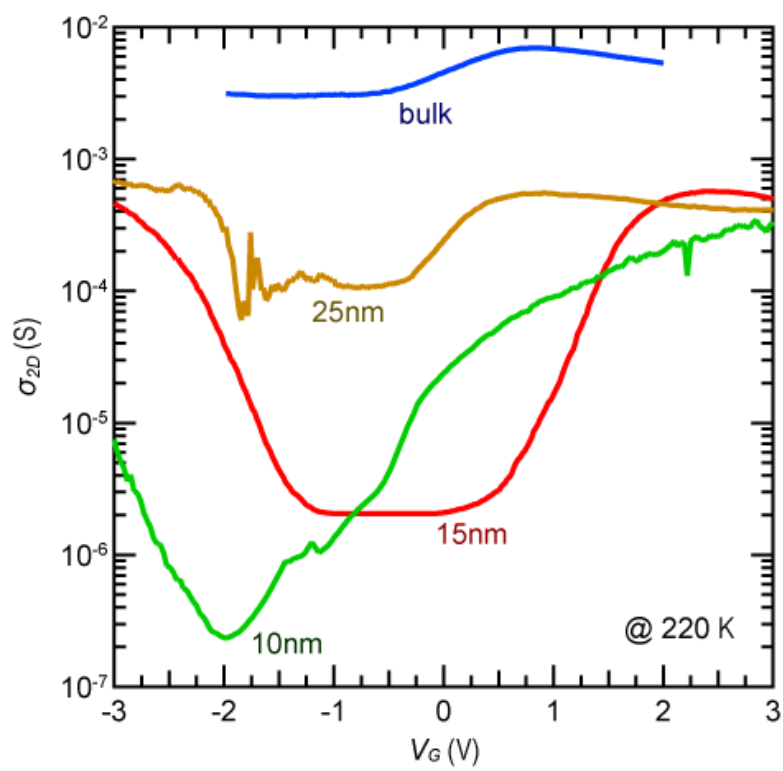


Figure S3

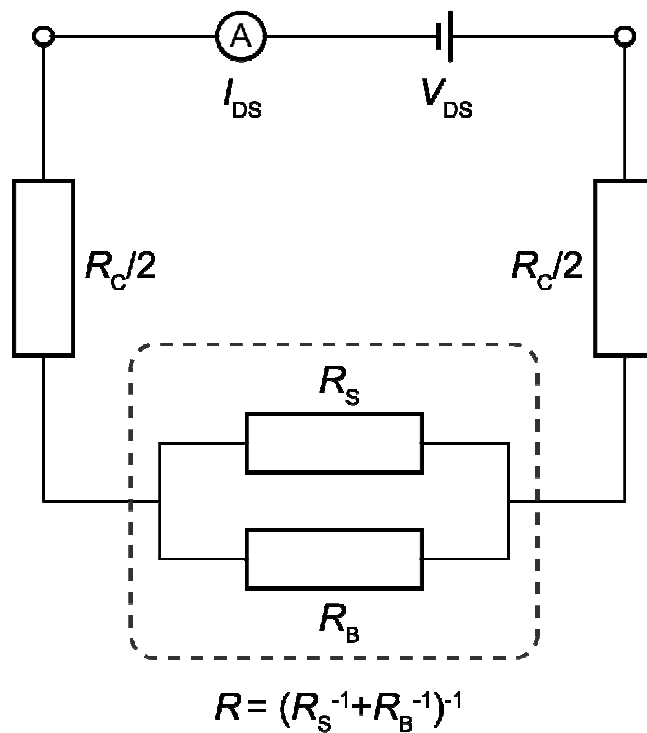


Figure S4

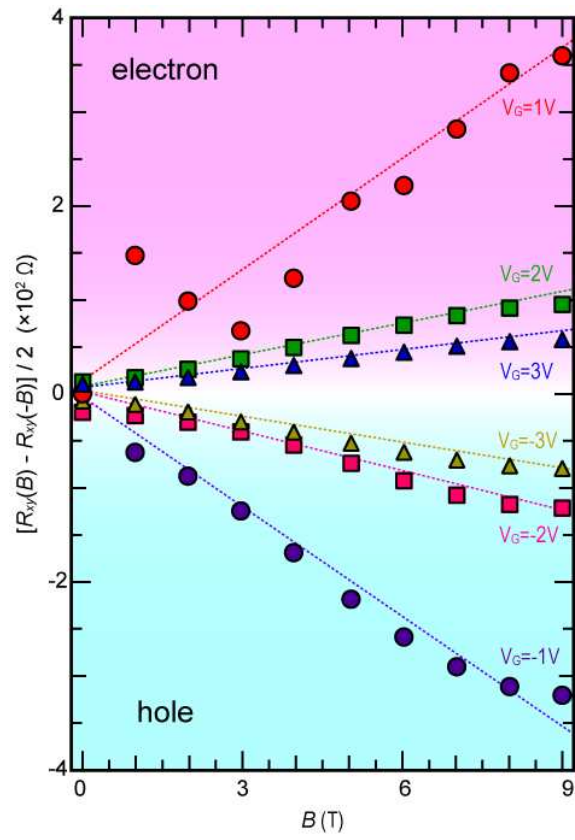


Figure S5