Supplementary Information:

Figure S1 indicates the specific capacity of the MoO_{3-x} NWs in the lower potential range for 20 cycles. Figure S2 shows the reactor setup used for the silicon coating on the MoO_{3-x} nanowires. Figure S3 corresponds to the SEM image of pure MoO_{3-x} NW arrays and silicon coated MoO_{3-x} nanowire array with the diameter scales.

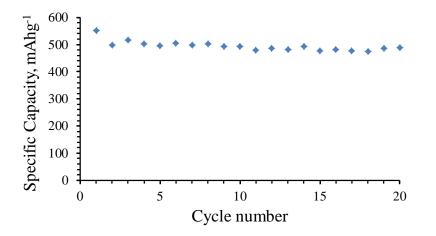


Figure S1: Capacity retention below 0.7 V for pure $MoO_{3-x}NW$ arrays .

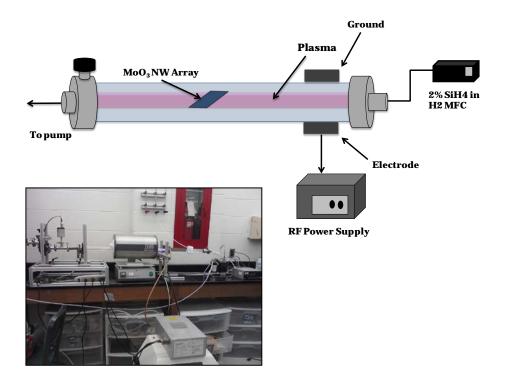


Figure S2: Schematic and picture of the reactor setup used for silicon coating.

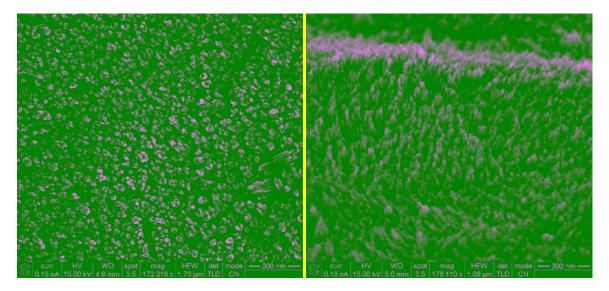


Figure S3: SEM images of silicon coated MoO_{3-x} NW arrays.