Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate

*Alexander Badmaev, Yuchi Che, Zhen Li, Chuan Wang and Chongwu Zhou**

Department of Electrical Engineering, University of Southern California, Los Angeles California 90089, USA.

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*To whom correspondence should be addressed. E-mail chongwuz@usc.edu

Supplementary Information

Experimental Methods.

Graphene synthesis and transfer Monolayer graphene films were synthesized on copper foils (Alfa Aesar, 99.8% purity) through a low pressure chemical vapor deposition (CVD) method. Copper foils were loaded in the quartz tube furnace. The chamber then was pumped and pressure maintained at 500 mTorr. The temperature was raised to 1000 ºC while flowing 30 sccm of hyrdrogen. Then, graphene growth was obtained by flowing 30 sccm hydrogen and 7 sccm methane at 1000 ºC for 30 min, while keeping 500 mTorr pressure in the chamber. The chamber was then cooled to room temperature while keeping the same gas flow. In order to transfer graphene to Si/SiO_2 substrates, we first covered graphene on the copper foils with PMMA.

Copper foil was then etched away in a ferric chloride solution, leaving floating PMMA film with attached graphene. PMMA/graphene film was thoroughly rinsed in DI water and placed on top of the target substrate. The substrate was dried out of water and PMMA was removed in acetone and dichloroethane solvents, leaving graphene on the target substrate.

T-shaped gate fabrication After graphene transfer, we defined metal pads (1nm Ti/60 nm Pd) in coplanar waveguide geometry for microwave probing. Then, we fabricated T-shaped Al gates using bilayer e-beam resist. Bottom layer, PMMA 950k A2, was spin-coated at 5,000 RPM and baked on a hotplate at 180 ºC for 10 min. Top layer, P(MMA-MAA) E6, was spin-coated at 1,500 RPM and baked at 150 ºC for 10 min. Bilayer e-beam resist was exposed with electron beam of around 400 $\mu C/cm^2$ dose at the center of T-gate and around 150 $\mu C/cm^2$ dose outside the center. The bilayer e-beam resist was then developed in MIBK:IPA 1:3 solution for 1 min. 140 nm Al film was deposited and lift off in acetone leaving T-shaped Al gate. Al gate was then oxidized in air at 140 ºC for 1 hour. Deposition of 12 nm Pd film over the active area with T-shaped gate created separated source and drain electrodes and completed the transistor fabrication.

De-embedding procedure Figure S3 shows schematic images of open and short structures used for the de-embedding procedure. The de-embedding procedure subtracts the effect of the pads, and provides microwave response from the device in the active areas, which includes ~1 μm source/drain electrodes, graphene channel and top gate electrode and connection. We call the de-embedded results as 'device' performance, since it is the performance of an integrated transistor in a circuit, where it does not require probing pads.

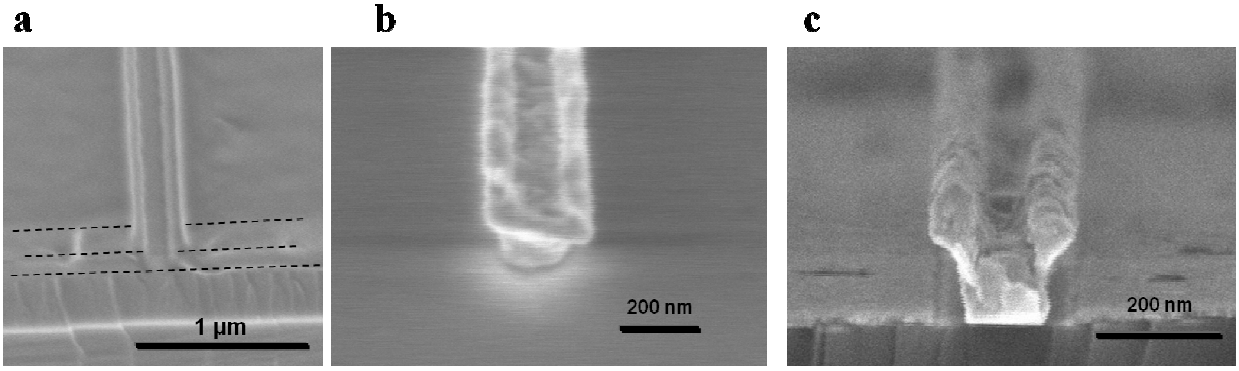

Figure S1. Fabrication of T-gate transistors. (a) SEM image of the bilayer e-beam resist after the gate e-beam writing and development (45 degree viewing angle). (b) SEM image of an Al T-shaped gate after lift-off (45 degree viewing angle). (c) Cross section SEM image of a a complete self-aligned graphene transistor.

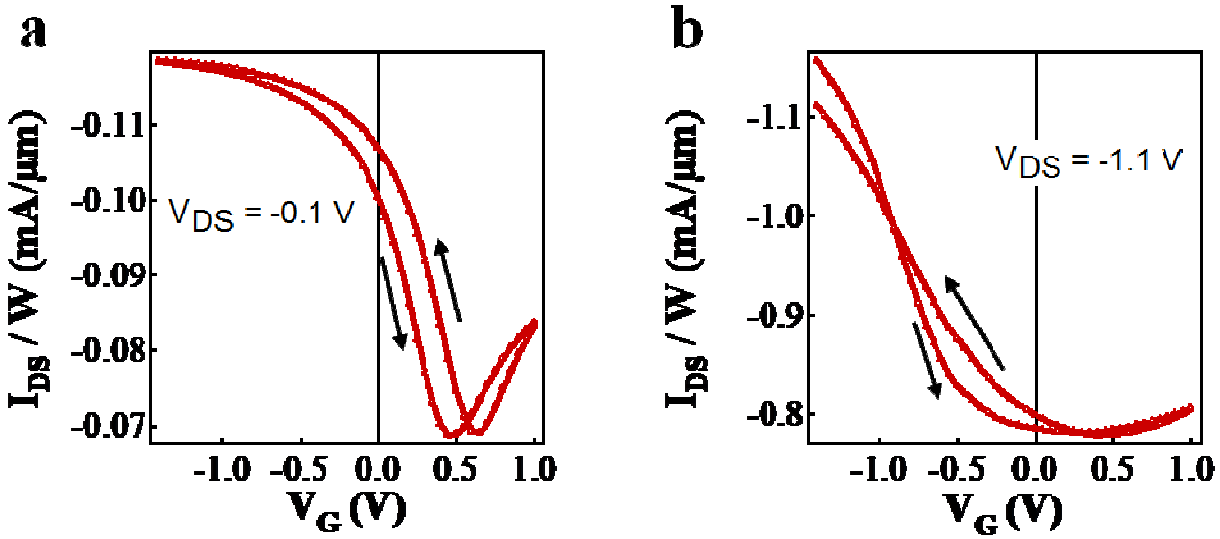

Figure S2. Hysteresis in graphene transistors. Transfer curves for a graphene transistor at source-drain bias V_{DS} = -0.1 V (a) and V_{DS} = -1.1 V (b). Arrows show the direction of measurement sweep. Back gate (substrate) voltage is equal to 0 V.

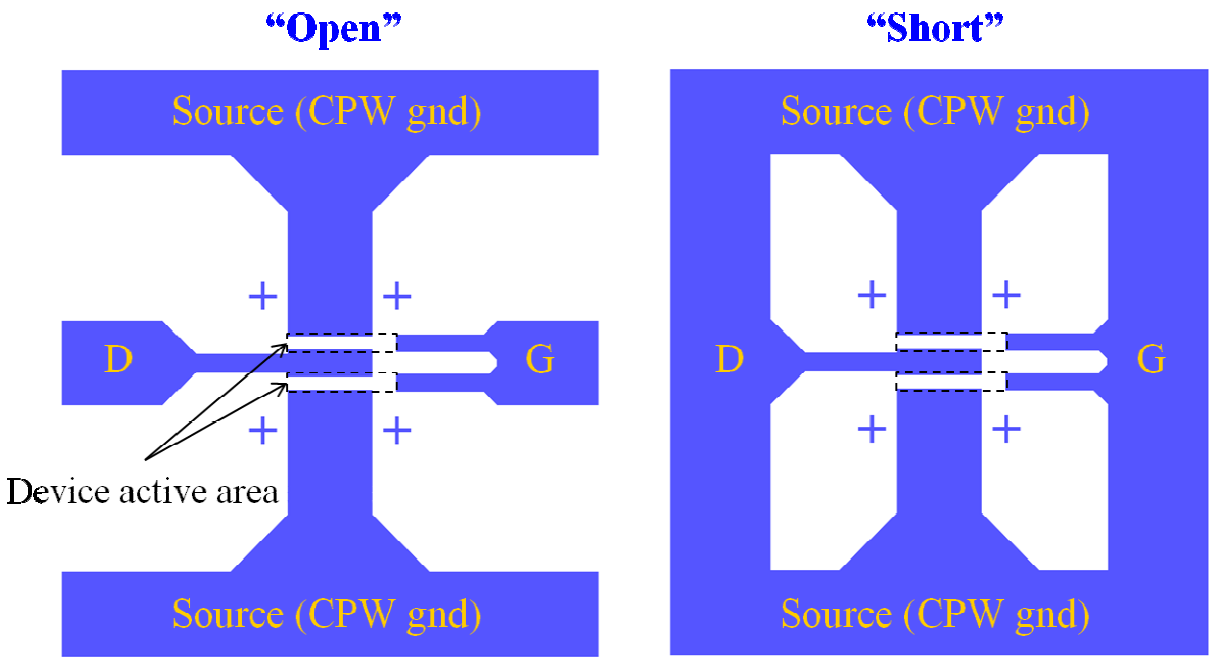

Figure S3. Schematic images of open and short structures used for the de-embedding procedure. The de-embedding procedure subtracts the effect of the pads, and provides microwave response from the device in the active areas, which includes ~1 μm source/drain electrodes, graphene channel and top gate electrode and connection.

Graphene transistors on quartz Another way, to obtain intrinsic device performance is use of an insulating substrate. In this case, the parasitic pad capacitance becomes negligible. Using the same self-aligned T-gate fabrication procedures, we also fabricated graphene transistors on quartz substrates. Figure S4 shows extrinsic (as measured) microwave current and power gain of a graphene transistor on quartz substrate. Here, we obtain the extrinsic cut-off frequency of 20 GHz, similarly to the de-embedded 'device' performance of the T-gate graphene transistors.

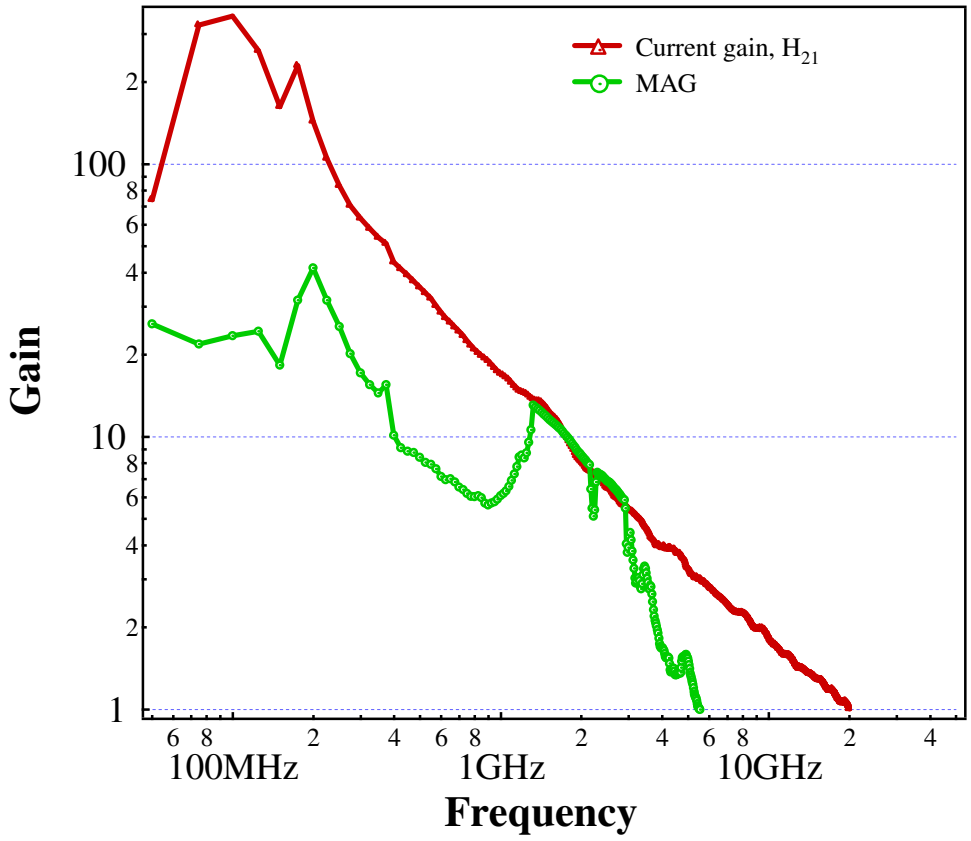

Figure S4. Extrinsic current gain (H_{21}) (red line) and maximum available gain (MAG) (green line) of a graphene transistor fabricated on quartz substrate.