Supporting Information for

High Mobility Flexible GrapheneField-Effect Transistors with Self-Healing Gate Dielectrics

Chun-Chieh Lu,[1] Yung-Chang Lin,[1] Chao-HuiYeh,[1] Ju-Chun Huang,[2] Po-Wen Chiu[1]*

[1]Department of Electrical Engineering, National TsingHua University, Hsinchu 30013, Taiwan

[2]Center for Nanotechnology, Materials Science and Microsystems, National TsingHua University, Hsinchu 30013, Taiwan

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*E-mail: pwchiu@ee.nthu.edu.tw

1. Optical photographs, Raman spectrum, and light transmittance of CVD graphene

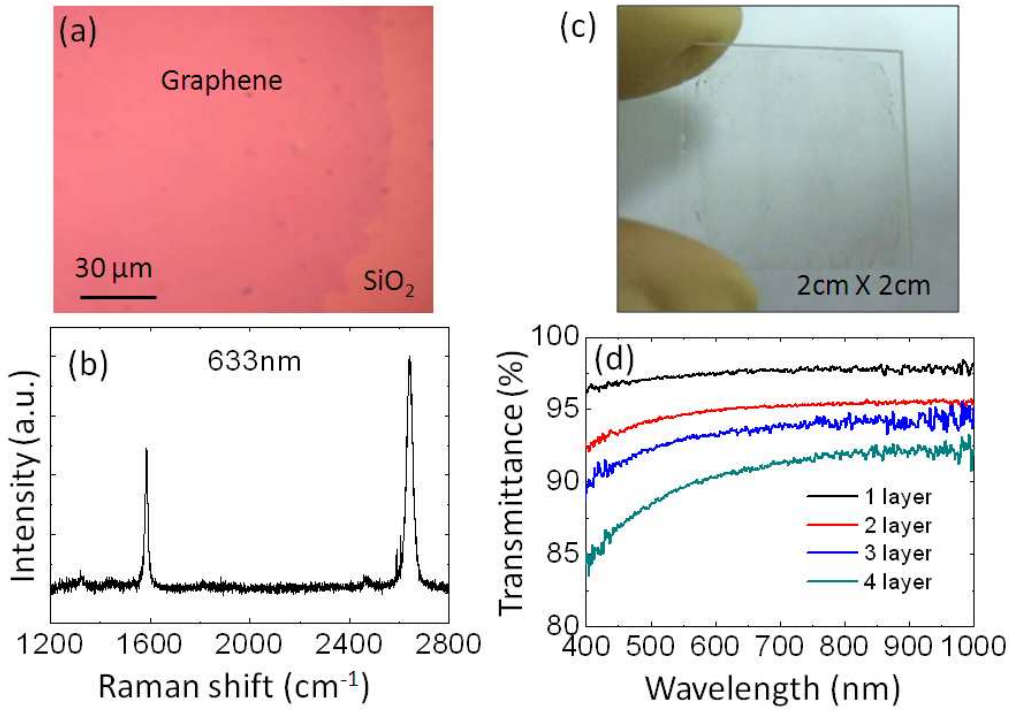

Figure S1 (a) Large-area clean CVD graphene transferred to Si substrate with 300 nm oxide layer on top. No macroscopic metal and polymer residues are seen on graphene surface. **(b)** Raman spectrum of the transferred graphene on SiO_2. The 2D peak can be described by a symmetric single Lorentzian with the full width of half maximum of 30 cm^{-1}.The 2D over G intensity ratio is >1.5. The spectrum is featureless near the D mode (1350 cm^{-1}), indicating that the transferred graphene film contains very low defects. **(c)** Optical photograph of a 2×2 cm^2 CVD graphene transferred to glass substrate. **(d)** Light transmittance of graphene films with 1 to 4 layers. The light transmittance of a single-layer graphene is ~97% at 550 nm, close to the theoretical attenuation value of 2.3%.

2. TEM characterization of CVD Graphene

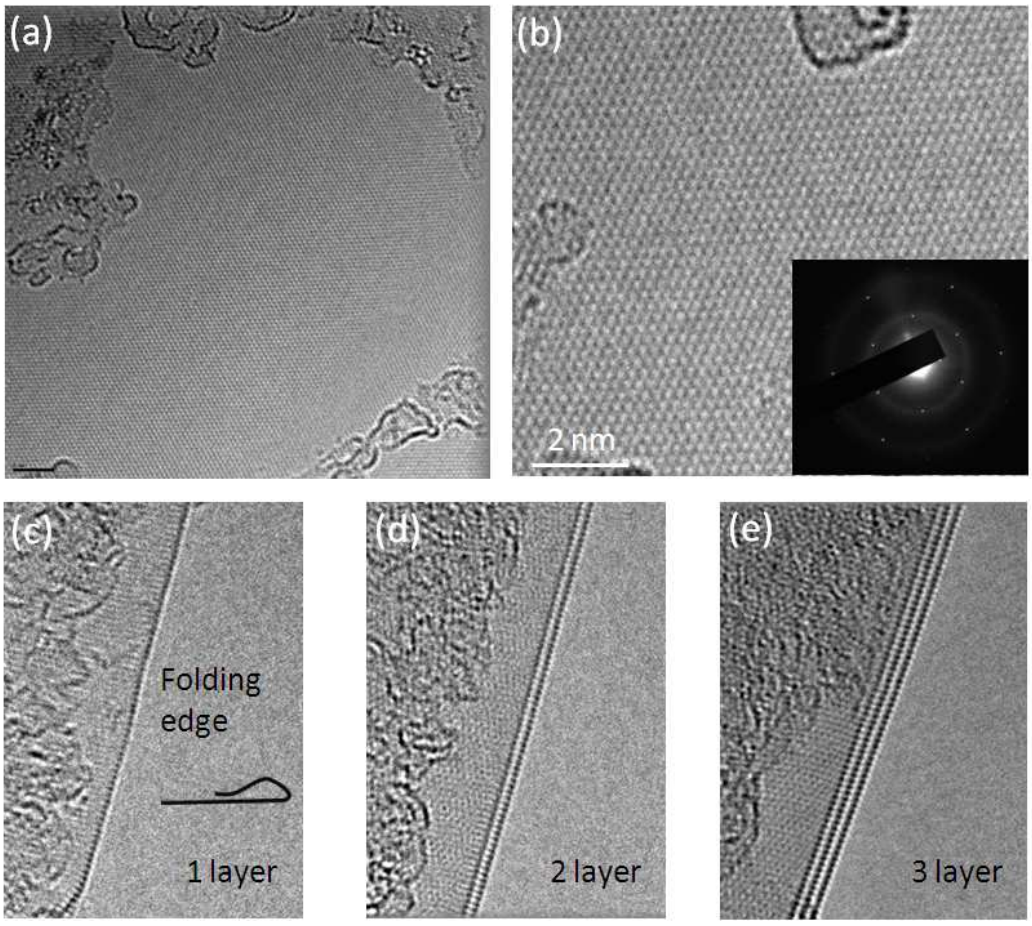

Figure S2 (a) and **(b)** show TEM images of our CVD graphene films used for making flexible FETs on PET. The inset of **S2 (b)** shows the selected-area electron diffraction pattern. **S2 (c)-(e)** show the folding edges of graphene layers, providing an alternative way to determine the number of layers. Very small portion of the film appears to be bi- or tri-layer graphene. For those FETs fabricated on bi- or tri-layer graphene, the mobility calculated using the formula described in main text is expected to be far below the mean mobility due to the screening of electric field applied by the gate.

3. AFM images of CVD Graphene on Si and PET substrates

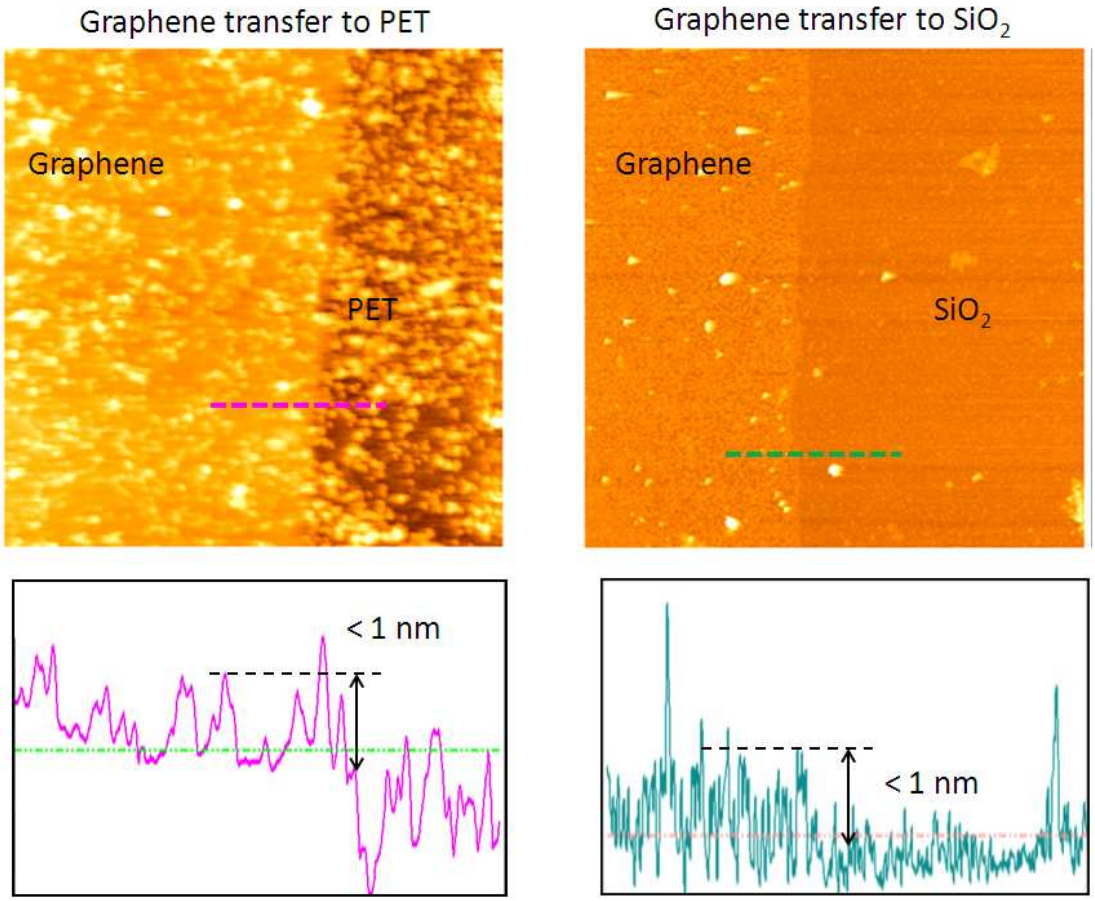

Figure S3 AFM images of the CVD graphene transferred to Si and PET substrates. The full scale of the image is 5 μm. The lower panels show the height profiles of the scans indicated by the dashed lines. A height step of ~1 nm can be clearly seen at the edge of graphene film. Although the PET surface is rougher than SiO_2 surface, the transferred CVD graphene remains continuous over large areas without apparent damage. The graphene film becomes semi-suspended on PET substrate.

4. Process flow of device fabrication

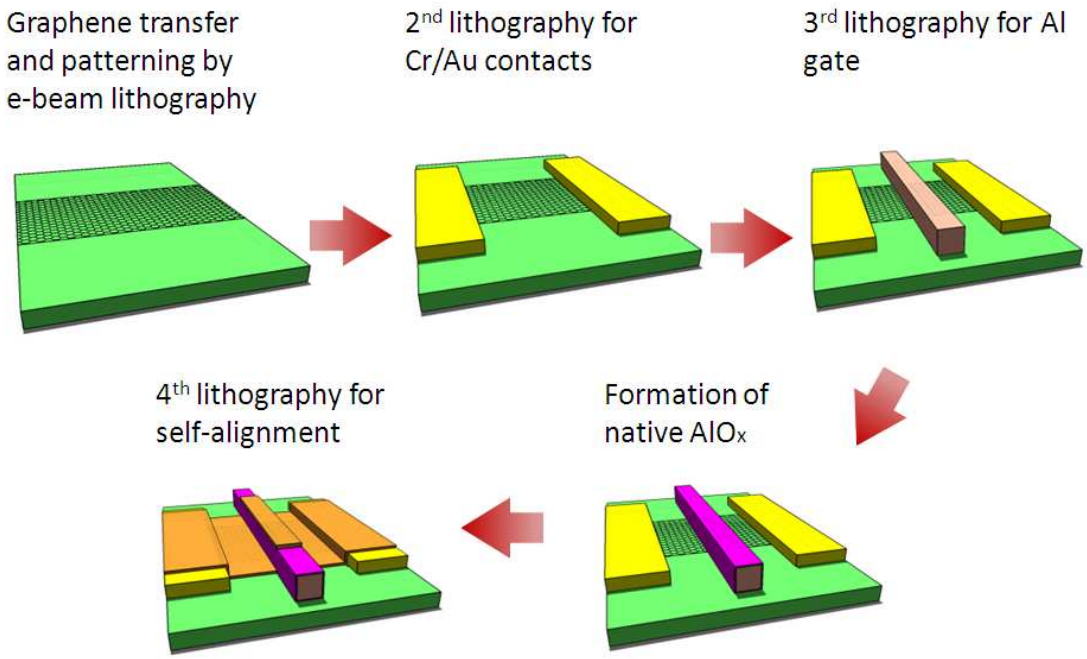

Figure S4 Schematic diagrams illustrating device fabrication process on PET substrate. Step 1, transfer CVD graphene on PET substrate, followed by e-beam lithography patterning. Graphene stripes are formed. Step 2, second e-beam lithography is applied to make the first layer of metal contacts (0.5 nm Cr/60 nm Au). Step 3, third e-beam lithography is used to define the Al gate on graphene. Step 4, exposure of the devices in air to form a thin layer of aluminum oxide around the Al gate. Step 5, the fourth e-beam lithography is used to open a deposition window, covering the graphene stripe. Then, self-aligned drain/source electrodes (0.5 nm Cr/10 nm Au) are deposited.

5. TEM images of AlO_x layer

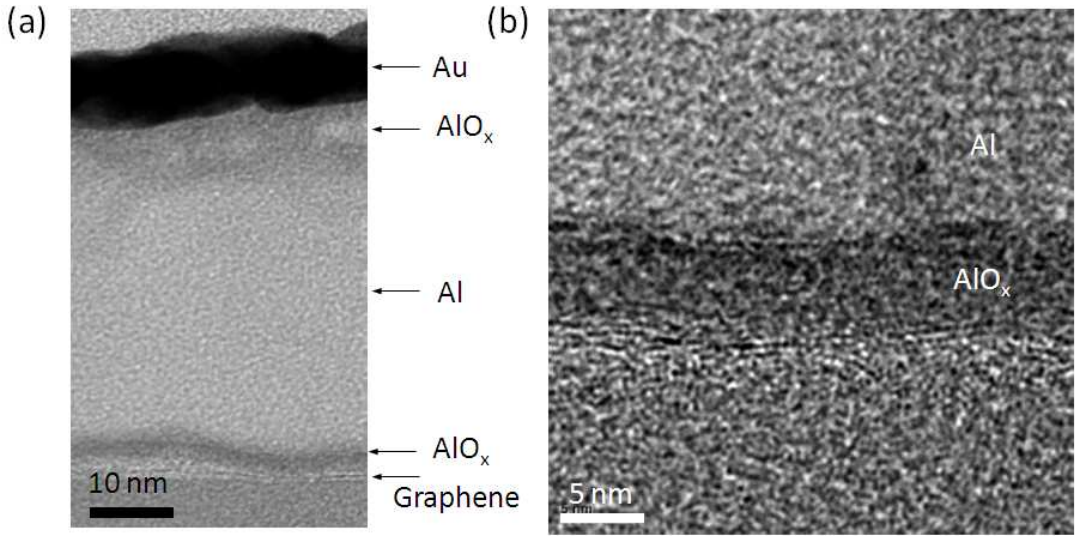

Figure S5 (a) Cross-sectional TEM image of the gate electrode. The AlO_x can grow deep into the Al/graphene interface. The part exposed to air can be as thick as 12 nm, while the part between the Al and graphene is only 5 nm. **(b)** High-magnification TEM image of the gate stack.

6. Comparison of device mobility in different flexible FETs

Table 1 Comparison of field-effect mobility in large-area flexible FETs

Channel/substrate materials	**Gate dielectrics**	**Mobility (cm^2/Vs)**	**On/Off ratio**	**Minimum bending radius (mm)**	**Operating voltage (V)**	**Year**
a-Si:H/Polyimide[1]	SiO_2-silicone hybrid	0.5	-	0.5	15	2010
Polycrystalline Silicon/Polyimide[2]	ECR-PECVD Oxide	50	10^6	-	-	2007
a-IGZO/ Polyethylene terephthalate[3]	Y_2O_3	7	10^3	30	10	2004
a-IGZO/Glass[4]	SiN_x	35.8	10^6	-	-	2007
Organic Single Crystals/PDMS[5]	PDMS	15	10^6	-	-	2004
Pentacene /Polyimide[6]	Polyimide	0.5	10^5	0.5	40	2005
Pentacene, Et-6T-Et, Dec-6T-Dec/PEN[7]	PVP, C10-PA, C14-PA /AlO_x	0.1	-	2.5	2.5	2009
Pentacene/ Polyimide[8]	SAM/Al_2O_3	0.5	10^6	0.1	2	2010
DNTT/PEN[9]	Parylene	0.2	10^6	8	20	2011
CNTs/Polyester[10]	Parylene	1	10^2	-	40	2005
CNTs/Polyimide[11]	SiO_2	150	10^2	-	-	2005
CNTs/Polyimide[12]	HfO_2	80	10^5	5	< 5	2008
CNTs/Polyimide[13]	Ion gel	50	10^3	-	< 3	2010
CNTs/PEN[14]	Al_2O_3	630	10^6	-	5	2011
Graphene/PET[15]	Ion gel	Hole: 203 Electron: 91	8	6	3	2010
Graphene/PET [this work]	AlO_x	Hole: 300 Electron: 230	< 4	>8	3	-

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7. Transfer characteristics of self-aligned graphene FETs on PET substrate

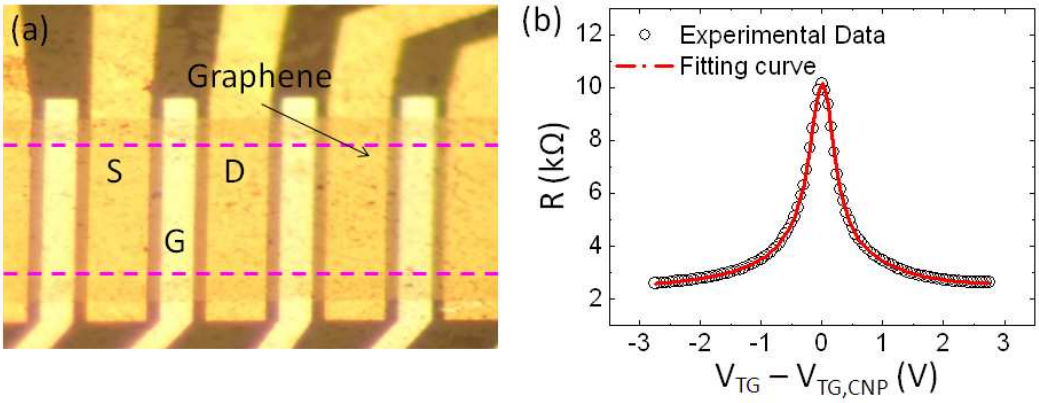
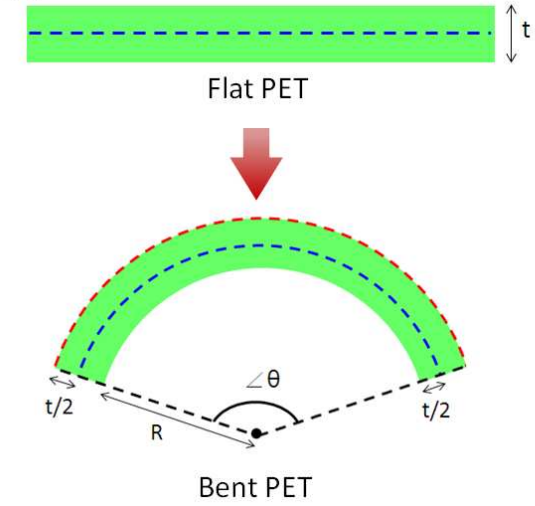


Figure S7 (a) Optical photograph of flexible graphene FETs on PET. The gate length is 2 μm, and the channel width is 5μm. **(b)** Transfer characteristics of the same device shown in Fig. 3c in main text, plotted in the form of R_{tot} versus $V_{TG} - V_{TG,CNP}$. The solid red curve is obtained by fitting using the equation described in the main text. The fitted curve agrees well with the experimental data, with the residual concentration of $n_0 = 7 \times 10^{11}$ cm^{-2}, $R_{contact}$= 2400 Ω, and the mobility of μ ~5000 cm^2/Vs.

8. Tensile strain caused by bending PET substrate

(a)



(b)

Radius (mm)	Tensile Strain (%)
40	0.16
30	0.21
20	0.31
10	0.62
7.5	0.83

Figure S8 (a) Schematic diagram of PET bending. **(b)** Table of tensile strains corresponds to different bending radii. Tensile strain was applied to the graphene sheet on the top surface of PET substrate while bending. We assume that the thickness of PET substrate remains unchanged and the mid level of the substrate (blue dashed line) is strain-free upon bending. The strain is derived by dividing the increase in length of the strained top surface (red dashed line) by the unstrained length (blue dashed line). From the simple calculation, we obtain the tensile strain of graphene to be $100t / (2R + t)$%, where t is the thickness of PET substrate (125 μm in this case) and R is the bending radius.

9. Self-healing by electrical annealing

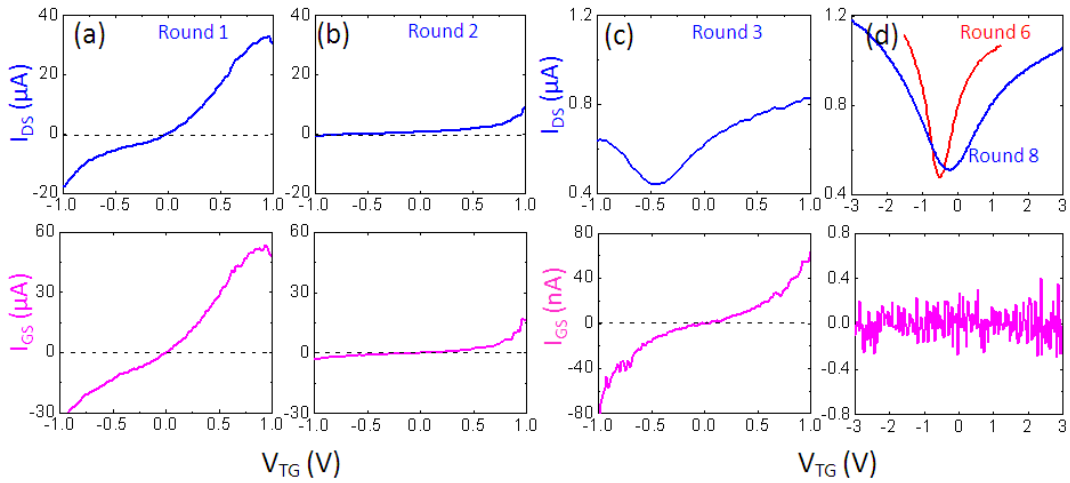


Figure S9 The self-healing rate can be expedited using electrical annealing. We found that sweeping the positive gate-source voltage can drive the oxide regrowth, and the tunneling current gradually decreases upon the gate sweeps. As shown in **(d)**, the transfer characteristics of the graphene FET can recover to their pristine state after 5-6 rounds. In the early stages of regrowth, the newly grown thin oxide layer results in a steeper I–V_{GS} curve (red), corresponding to a higher g_m in the graphene FETs. As the oxide thickness increases with increasing electrical annealing rounds, the gate capacitance decreases as does the slope of the I–V_{GS} curve (blue).

10. Electron tunneling through the Al/AlO$_x$/graphene junction

For a rectangular barrier, the current at low bias limit is given by $I \propto V_{ds} \exp(-2d\sqrt{2m\Phi_B}/\hbar)$, where m is the electron mass, d is the barrier width, Φ_B is the barrier height, and $\hbar$ is the reduced Planck's constant. Raising the bias, the barrier starts thinning at the Fermi energy, yielding a triangular barrier. Within the WKB approximation, the triangular barrier gives $I \propto V_{ds}^2 \exp(-4d\sqrt{2m\Phi_B^3}/3\hbar q V_{ds})$. To compare transport in the two distinct barrier profiles, the I–V_{ds} curves for low bias can be linearized in a logarithmic scale as

$$\ln(\frac{I}{V_{ds}^2}) \propto \ln(\frac{1}{V_{ds}}) - \frac{2d\sqrt{2m\Phi_B}}{\hbar}. \qquad \text{(S1)}$$

Similarly, the I–V_{ds} curves for high bias can be rearranged as

$$\ln(\frac{I}{V_{ds}^2}) \propto -\frac{4d\sqrt{2m\Phi_B^3}}{3\hbar q}(\frac{1}{V_{ds}}). \qquad \text{(S2)}$$

From the Eq. (1), it is obvious that a plot of $\ln(I/V_{ds}^2) - 1/V_{ds}$ will show a logarithmic growth which describes transport in terms of direct tunneling. In contrast, a plot of $\ln(I/V_{ds}^2) - 1/V_{ds}$ will yield a linear relation with slope proportional to $\Phi_B^{3/2}$ in Eq. (S2), which depicts transport via field emission (Fowler-Nordheim tunneling). Using Eq. (S1) and Eq. (S2), one can distinguish different tunneling behaviors in accordance with the specific barrier profile. In Fig. S10, the current-voltage characteristics of transport through the junction exhibit an inflection point on a plot of , providing evidence for a mechanistic transition from direct tunneling to field emission. The transition indicates a change of a rectangular barrier to a trianglular barrier at the junction. Electronic conduction is limited by the rate at which carriers with energy E_F can be injected from the metal and tunnel through the

triangular barrier into a defect level in the oxide. It should be note that field emission experiments generally involve barriers with both substantial width and height, so no measurable current flows prior to the onset of field emission. Therefore, a transition from direct tunneling to field emission will only be seen for the case of a small barrier height and width, such as is found in the metal/molecule/metal junctions and graphene/AlOx/Al junctions with hydrogen-induced defect level.

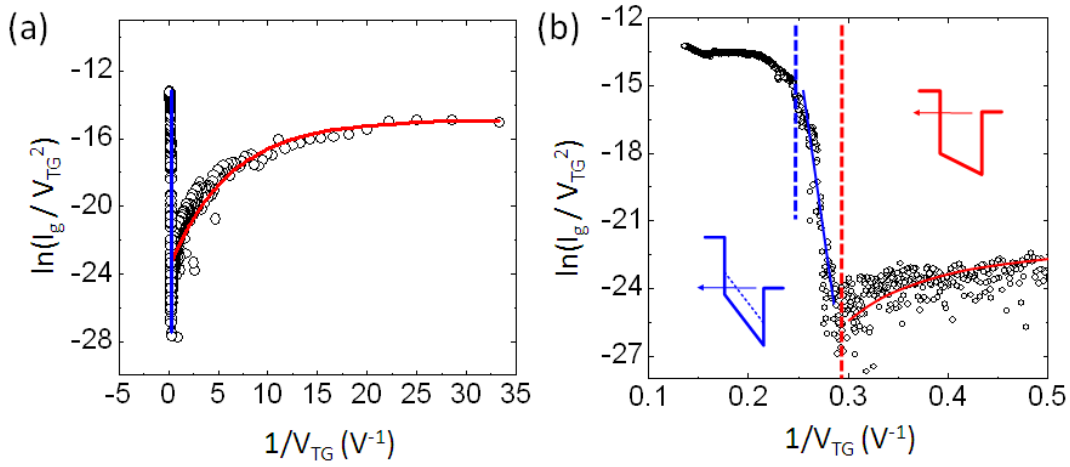


Figure S10 (a) $\ln(I_g / V_{TG}^2) - 1/V_{TG}$ plot of the I_g–V_{TG} curve shown in Fig. 4(b) in the main text. The blue line and red curve are the fits of linear and of logarithmic dependence of $1/V_{TG}$, respectively. **(b)** The zoom-in plot of (a) at the high voltage. The dotted red line denotes the transition point (V_{TG}~3.6 V), at which the tunneling mechanism changes. The blue line and red curve are the fits of linear and of logarithmic dependence of $1/V_{TG}$, respectively. Also shown are drawings of the barrier shape in the two different transport regimes. The dashed line in the blue barrier indicates the defect level.