Supporting Information

Integrated Circuits Based on Bilayer MoS_2 Transistors

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Methods

Device and integrated circuit fabrication: the fabrication of our devices and circuits starts with the exfoliation of MoS_2 thin films from commercially available bulk MoS_2 crystals (SPI Supplies) onto 285 nm SiO_2 on Si substrate, which has pre-patterned alignment grids (Cr/Au), using the micro-mechanical cleavage technique. The thickness of the SiO_2 was selected to provide the optimal optical contrast for locating MoS_2 flakes relative to the alignment grids and for identifying their number of layers[S1]. The number of MoS_2 layers was then confirmed by atomic force microscopy (AFM) based on its thickness and by Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode, respectively[S2]. The sample was then annealed at 350 C° in Ar 600 sccm/H_2 30 sccm for three hours to clean away the tape residue. The next step was to pattern the first metal layer (M1), which are the electrodes directly in contact with MoS_2, i.e. source and drain of the devices, using electron-beam lithography (Elionix F125) based on poly(methyl methacrylate) (950k MW PMMA) resist. We then evaporated 3 nm Ti/ 50 nm Au followed by lift-off to form the contacts. Subsequently, the samples were annealed again at 350 ℃, 600 sccm Ar/30 sccm H_2 for three hours. This annealing step reduces device resistance and also removes the PMMA residue to create a clean surface for subsequent atomic layer deposition (ALD) process. The top gate dielectric consisting of 20 nm HfO_2 was then deposited by ALD. To fabricate discrete transistors, the last step of the fabrication was to pattern the top gate electrode by electron-beam lithography, which was then formed by depositing the desired gate metal. The devices reported in this work (Fig. 2 in the main text) have L_G=1 μm and L_{DS}=1 μm. The gate is aligned to the channel using the standard alignment techniques in e-beam lithography. For the construction of integrated logic circuits (Fig. 2B in the main text), the second and third metal layers (M2 and M3) need to be connected to the

first metal layer (M1) at certain locations depending on the design. This was achieved by patterning and etching via holes through the HfO_2 dielectric using reactive ion etching (RIE) with BCl_3/Cl_2 gas chemistry. This etching step preceded the definition of the gate metal layers M2 and M3.

AFM and Raman spectroscopy: Atomic force microscopy (AFM) for identifying the thin film thickness was performed on a Veeco Dimension^{TM} 3100 system. Raman spectroscopy was performed with a 532 nm Nd:YAG laser. All optical micrographs were taken with a Zeiss Axio Imager.A1m microscope.

ALD and Via Hole Etching: the HfO_2 gate dielectric was deposited using ALD at 170 °C. The ALD deposition of HfO_2 was done on a commercial Savannah ALD system from Cambridge NanoTech using alternating cycles of H_2O and tetrakis(dimethylamido)hafnium (TDMAH) as the precursors. To fabricate the integrated circuits shown in this report, it is also necessary to etch via holes through the HfO_2 dielectric so that on-chip interconnections can be made between metal layer 1 and metal layers 2 and 3. We used a commercial Electron Cyclotron Resonance Reactive Ion Etcher (ECR/RIE) system (Plasma Quest) to perform this etch using BCl_3/Cl_2 gas chemistry. The ratio between the flow rates of BCl_3 and Cl_2 is 4:1. The etch rate of our low power recipe is around 6 nm/min.

Device and circuit characterization: Device characterization was performed using an Agilent 4155C semiconductor parameter analyzer and a Lakeshore cryogenic probe station with micromanipulation probes. The integrated circuits were characterized with an Agilent 54642A oscilloscope (1 MΩ input impedance) and the output signal power spectrum of the ring oscillator was measured with an Agilent N9010A Signal Analyzer (50 Ω input impedance). All measurements were done in vacuum (~10^{-5} Torr) at room temperature.

Identifying the number of layers in exfoliated MoS_2 thin film by AFM and Raman

The number of molecular layers in exfoliated MoS_2 thin film can be identified from measuring its thickness by atomic force microscope (AFM) and by Raman spectroscopy, based on the peak spacing between the E_{2g} mode and A_{1g} mode[S2]. Fig. S1 shows the correspondence between the AFM data and Raman data for 1-layer (1L) to 5-layer (5L) MoS_2 flakes. After exfoliating the MoS_2 thin film onto 285 nm SiO_2/Si substrate, the flakes were first located using optical microscope and the number of molecular layers was estimated based on their optical contrast[S1]. Then the number of layers was confirmed using both AFM and Raman spectroscopy. Bilayer MoS_2 thin films used in this report typically have a thickness around 13 Å as measured by AFM.

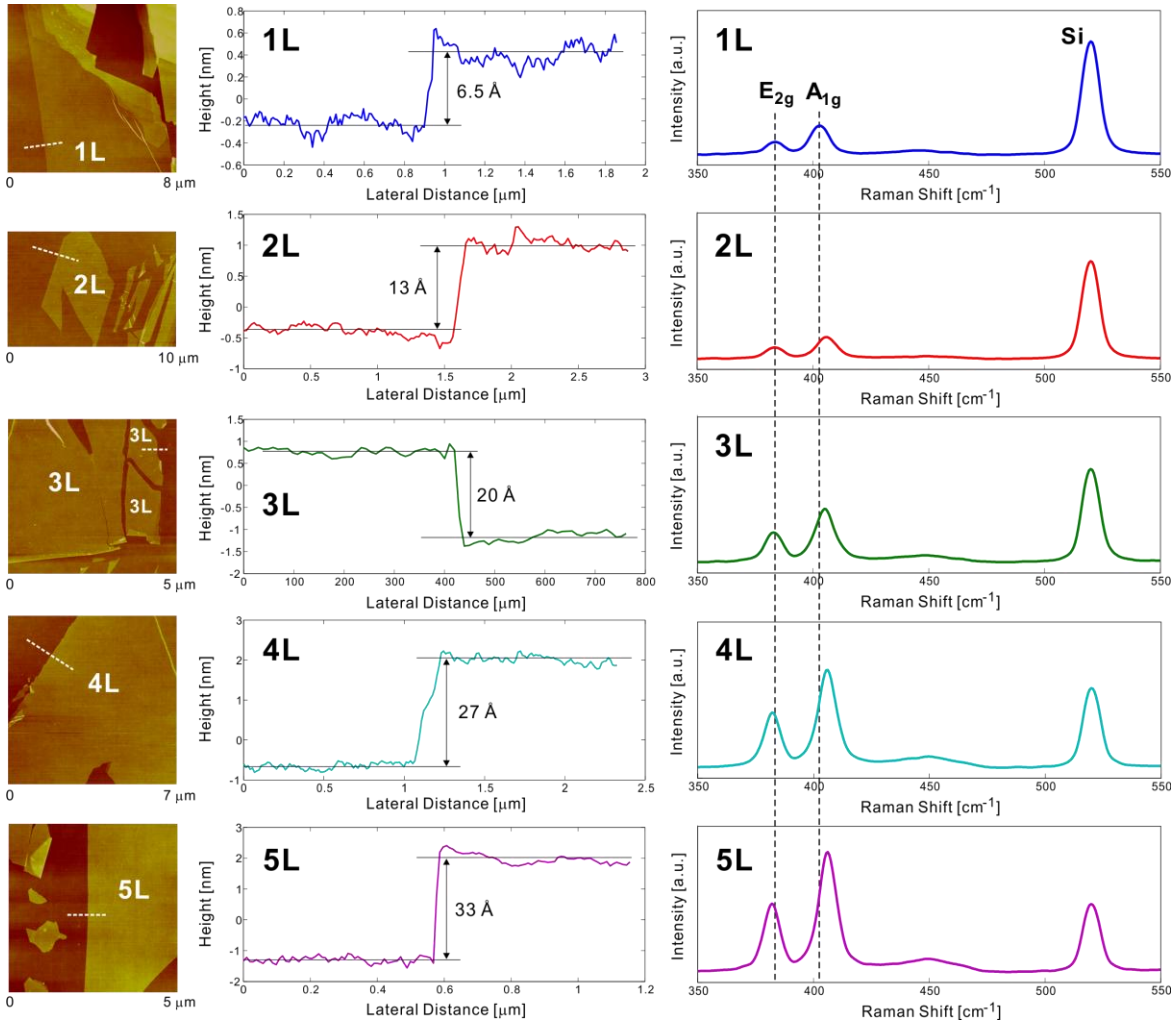

Fig. S1. Corresponding data from AFM and Raman spectroscopy measurements for one-layer to five-layer MoS_2 thin films. For each MoS_2 flake, the height information from AFM and Raman peak spacing between E_{2g} mode and A_{1g} mode are cross-checked to confirm the number of layers in the MoS_2 thin film.

Although single-layer MoS_2 FETs exhibits high on/off current ratio and low off-state current, which is important for minimizing the loss in the devices when they are turned off, it can only supply a very limited amount of current when the device is turned on (only 2.5 μA/μm at V_{ds}=0.5 V as reported in ref. S3). Since the speed of a logic circuit is often determined by the ratio between the charge required to change the voltage across the various capacitances in the circuits and the current that can be supported by the transistors, the low on-state current in single-layer MoS_2 may limit the operation speed of any electronic systems constructed from this material. On the other hand, by increasing the number of MoS_2 layers, the on-state current of MoS_2 FETs can be increased significantly (close to 20 μA/μm at V_{ds}=0.5 V V_{tg}=2 V for bilayer MoS_2 in this work) with only small degradation in terms of on/off current ratio. The higher on-state current in bilayer MoS_2 as compared to single layer MoS_2 can be due to several factors,

with the most important one being the increase in mobility with the number of MoS_2 molecular layers. The mobility of MoS_2 increases with the number of molecular layers, as reported in ref. S4. This is also evidenced by other recent results in the literature. For example, ref. S5 reported a mobility of 517 $cm^2 V^{-1} s^{-1}$ for a 23 layer flake (15 nm thick). In this work, the bi-layer MoS_2 flake shows a mobility of 313 $cm^2 V^{-1} s^{-1}$ while the best mobility reported for single layer MoS_2 flake is 217 $cm^2 V^{-1} s^{-1}$ [S3]. For these reasons, we select bi-layer MoS_2 thin film as the material on which we demonstrate integrated logic circuits. For real electronic applications in the future, the selection of the number of layers may depend on the type of application. If better frequency performance is needed, then multi-layer MoS_2 may be used. If ultra-low power performance is necessary, then single-layer MoS_2 may be a better choice. And bi-layer and tri-layer MoS_2 thin films may offer good trade-off in between. In short, the capability to control the number of molecular layers in the 2D crystal and the consequent control of the electronic properties enables added flexibility in this material system. In the future, it may be possible to build integrated circuits where different sections of the IC use different number of layers of MoS_2 thin films. The high performance sections (e.g. analog to digital converters, high speed oscillators) can use multilayer MoS_2 thin films while the low loss section (e.g. memory units) can use fewer layer of MoS_2 thin films.

Work function Difference between Al and Pd

To build both depletion-mode and enhancement-mode FETs on the same sheet of MoS_2, we use metals with different work functions, w_M, as the gates to control the threshold voltages of the FETs. Fig. S2 shows the band diagram of FETs with gate metal work function either greater than the semiconductor work function, i.e. $w_M > w_S$, or smaller than the semiconductor work function, i.e. $w_M < w_S$. A low work function metal tend to induce electrons in the channel, tuning the channel to the charge accumulation regime; while a high work function metal can induce the channel into the charge depletion regime, all at zero gate bias. For the Al-gate and Pd-gate MoS_2 FETs reported in this work, the shift in threshold voltage is around 0.76 V, which changes the threshold voltage from negative to positive and confers MoS_2 both enhancement-mode and depletion-mode FETs (Fig. 2C and 2D in the manuscript).

The difference between the work functions of two metals on a dielectric is generally different from that in vacuum. This phenomenon may be characterized quantitatively by the *S* parameter, which accounts for dielectric screening. It can be calculated as the ratio between the effective metal work-function difference on a dielectric to that in vacuum:

$$\Phi_{M,eff} = \Phi_{CNL,d} + S\,(\Phi_{M,vac} - \Phi_{CNL,d})$$

where $\Phi_{M,eff}$ is the effective work function of the metal in a dielectric and $\Phi_{M,vac}$ is the work function of the same metal in vacuum. $\Phi_{CNL,d}$ is the charge neutrality level of the dielectric. The difference between the effective work functions of two metals can then be related to their difference in vacuum: $\Delta \Phi_{M,eff} = \Delta \Phi_{M,vac}$. Since $\Delta \Phi_{M,eff}$ and $\Delta \Phi_{M,vac}$ are about 0.76 and 1.04 eV, respectively, we have $S \sim 0.7$ for the metals on HfO_2, which agrees closely with the value reported in ref. S6**.**

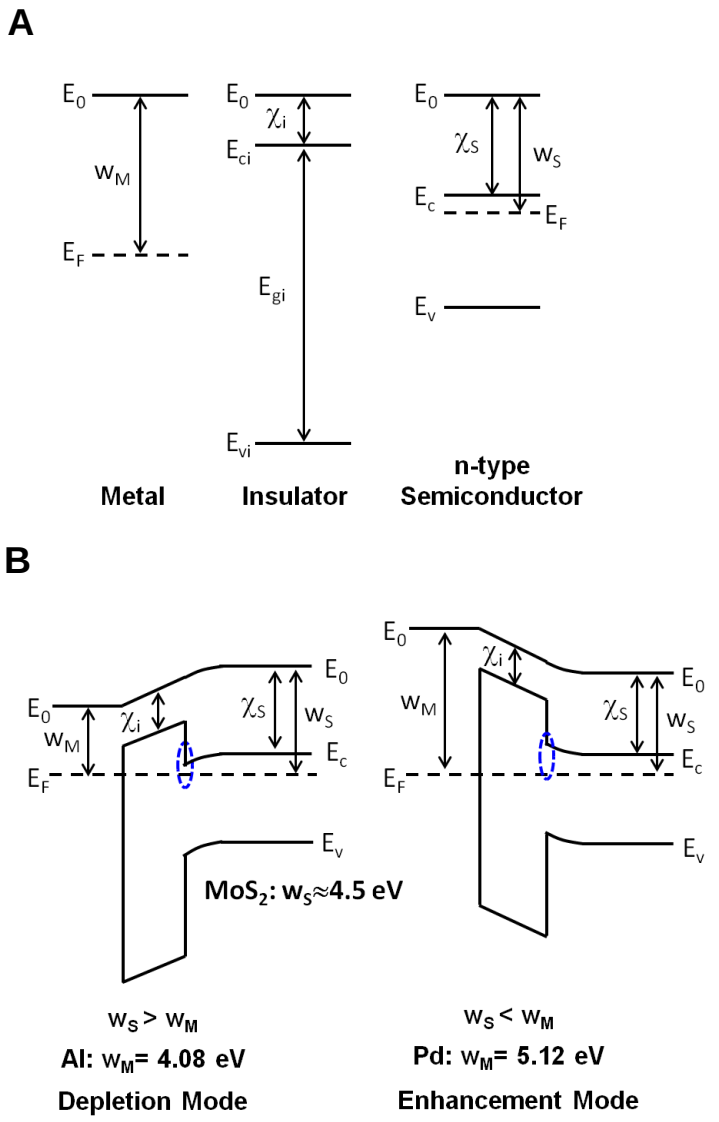

Fig. S2. Energy band diagrams **(A)** for isolated metal, insulator and semiconductor, and **(B)** after bringing them in intimate contact and thermal equilibrium is established. Depending on the different pairing of metal and semiconductor work functions, the metal-oxide-semiconductor (MOS) structure can induce the channel into either accumulation regime (for depletion mode FET) or depletion regime (for enhancement mode FET).

Mobility Extraction

The mobility of the bilayer thin films is extracted using the back-gate characteristics based on the expression $\mu = [dI_{ds}/dV_{bg}] \times [L/(WC_gV_{ds})]$. W=4 μm is the width of the device. L= 1 μm is the gate length. C_g is the gate capacitance per unit area, which is based on 285 nm SiO_2 for the back gate. V_{ds}= 1V is the bias applied at the drain electrode relative to the source electrode.

Typical field effect mobility measured based on this two-contact method is around 5-15 $cm^2\ V^{-1}\ s^{-1}$ for bilayer MoS_2. After the deposition of HfO_2, the extracted mobility increases to above 300 $cm^2\ V^{-1}\ s^{-1}$ (Fig. S3). This significant increase in mobility after the deposition of high-k dielectric agrees with the observation in ref. S3, which is attributed to the suppression of Coulomb scattering by the high-k dielectric environment[S7] and spatial-confinement-induced modification of the acoustic phonon spectrum in bilayer MoS_2[S8]. The complete understanding of this improvement will, however, need further theoretical and experimental studies. The field-effect mobility extracted using this method represents a conservative estimate of the mobility value because of effect of contact resistance[S3,S5], which was not de-embedded in the measurements.

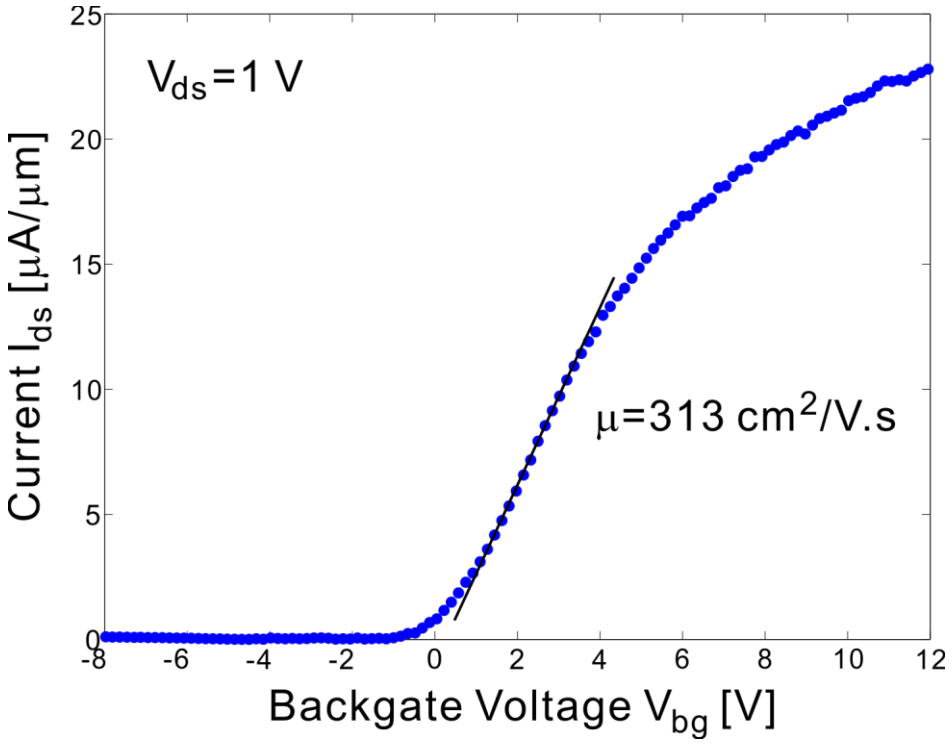

Fig. S3. Extraction of field-effect mobility based on back-gate characteristics of the device. The measurement is done at room temperature in vacuum (~10^{-5} Torr).

Estimation of the Ring Oscillator Speed

We can estimate the expected oscillation frequency for the ring oscillator at V_{dd}=2 V based on the parasitic capacitances present at various parts of the circuit and the driving current supported by the FETs as follows[S9,S10]:

a. The average driving current I_{ds} can be estimated from Fig. 3A of the report. Each inverter stage operates along the load line defined by the depletion-mode FET. Since the width of the FETs in the ring oscillator circuit is about 11 μm, we have $I \approx 22$ μA for V_{dd}=2 V.

The parasitic capacitance in the circuit is mainly contributed by two parts:

b. capacitances due to the overlap area between the top gate layers (M2 and M3) and the source/drain layer (M1). This capacitance is mainly due to the gate capacitance of the 12 FETs in the circuit as well as the overlap between the interconnects in the gate metal layers (M2 and M3) and that in the M1 layer. The gate capacitance of the 12 FETs are estimated based on their device width (about 11 μm on average for each FET), and their gate length (1μm for each FET) with 20 nm HfO_2 (dielectric constant ~22) as the dielectric material. This leads to capacitances of 1.285 pF. The remaining overlap area between the interconnects is around 5.3 μm^2, which gives an additional 0.051 pF. The total gate overlap capacitance is hence:

$$C_{ov\_gate} = 1.336 \text{ pF}$$

c. capacitances contributed by the conductive Si substrate with 285 nm SiO_2:

$$C_{ov\_Si} = 2.138 \text{ pF}$$

Hence, the estimated total parasitic capacitances per stage is equal to:

$$C \approx (C_{ov\_gate} + C_{ov\_Si})/6 = 0.579 \text{ pF}$$

The propagation delay per stage is estimated to be: $\tau_{pd} = CV_{dd}/I = 52.6$ ns.

Thus, at V_{dd}=2 V, the expected frequency for a 5-stage ring oscillator is equal to: $f = 1/(2n\tau_{pd}) = 1.9$ MHz.

This is very close to the measured value of the oscillation frequency, which is 1.6 MHz.

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