Supporting Information

Visualizing and Quantifying Charge Distributions Correlated to Threshold Voltage Shifts in Lateral Organic Transistors

*Thomas J. Dawidczyk,[1#] Josué F. Martínez Hardigree,[1#] Gary L. Johns,[2] Recep Ozgun,[3] Olivia Alley,[1] Andreas G. Andreou,[3] Nina Markovic,[2] and Howard E. Katz[1]**

[1]Department of Materials Science and Engineering, Johns Hopkins University, Baltimore, Maryland 21218

[2]Department of Physics and Astronomy, Johns Hopkins University, Baltimore, Maryland 21218

[3]Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, Maryland 21218

[#]contributed equally to this work

Correspondence and requests for materials should be addressed to Howard E. Katz[1] (email hekatz@jhu.edu).*

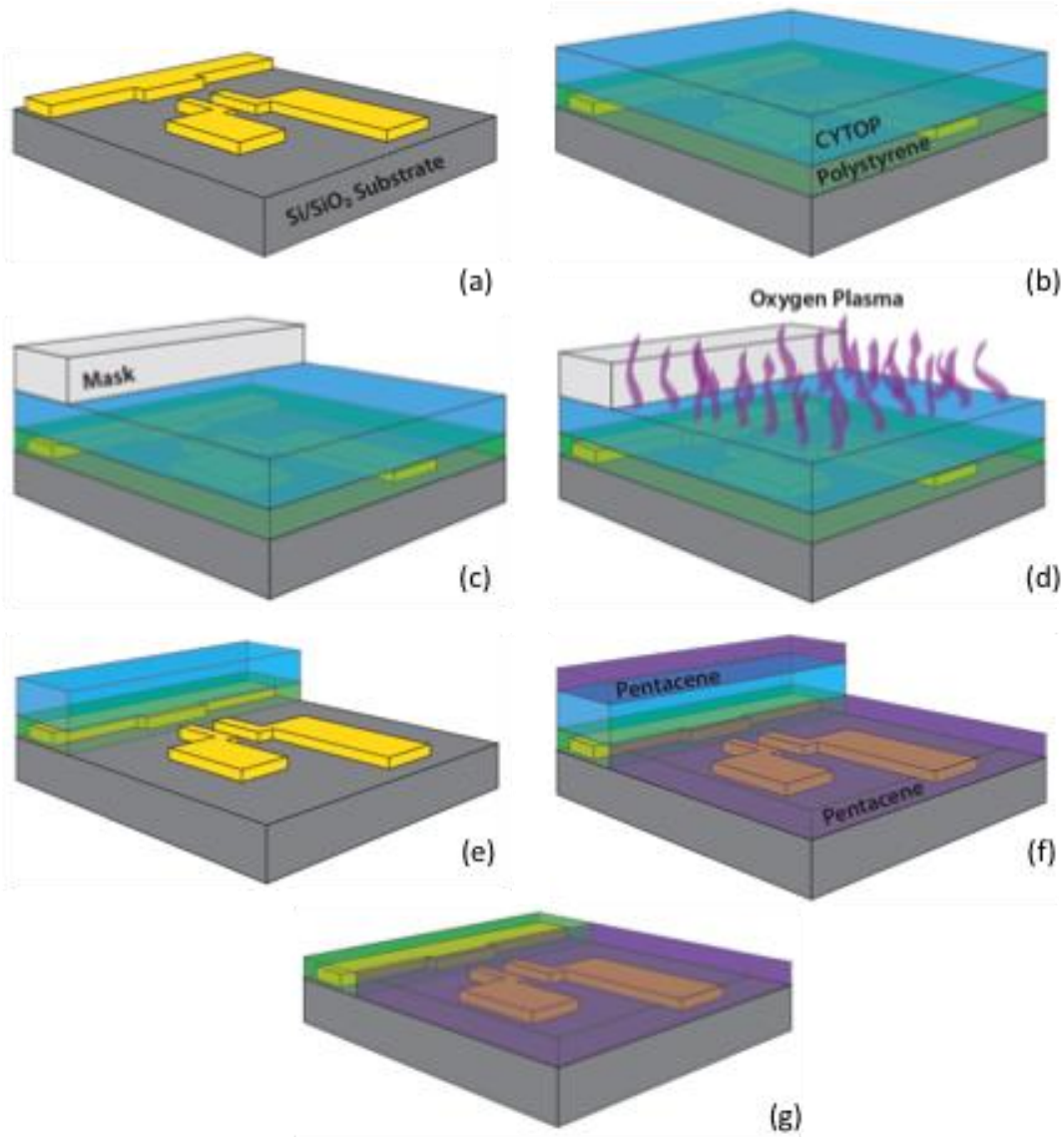

Figure S1. Schematic of the fabrication process for the lateral OFETs. First, 50 nm gold electrodes with a 5 nm Cr adhesion layer are deposited on the Si/300 nm SiO_2 substrate via photolithography (a). Atactic polystyrene (MW 50,000g/mol) (20 mg/mL in toluene) or poly (3-trifluoromethyl)styrene, (F-PS, 10 mg/mL in tetrahydrofuran) or poly(methyl methacrylate) (PMMA, 20 mg/mL in chlorobenzene, heated at 80 °C to dissolve) is then deposited via spin coating at 2000 RPM for PS and PMMA, and 1000 RPM for F-PS. The sample is annealed at 95°C for 10 minutes and allowed to cool to room temperature. Then Cytop is deposited via spin coating at 2000 RPM and annealed at 95°C for 10 minutes (b). A physical mask is placed on the substrate so that the edge of the mask is in the gap between the source/drain electrodes and the gate electrode (c). Oxygen plasma at medium power is used to remove the unmasked polymer layers (d). Once the organic layer has been removed from above the source/drain electrodes the OSC can be deposited (e). 50 nm of pentacene is thermally evaporated at 0.3 Å/s (f). The Cytop layer is then removed with perfluorodecalin, exposing the interface between the polymer and pentacene (g).

Experimental Procedure

Multiple samples were prepared on the same Si wafer, so the wafer was cleaved to get one or two samples per section. All KPM scans had 256 points and the retrace height for the surface potential was 100 nm. After the KPM scans the transistor measurements were performed. Each lateral OFETs was tested in the same manner, with the output curves taken first, followed by the transfer curves. Only these two measurements were taken, to keep the charges injected in the PS dielectric more consistent.

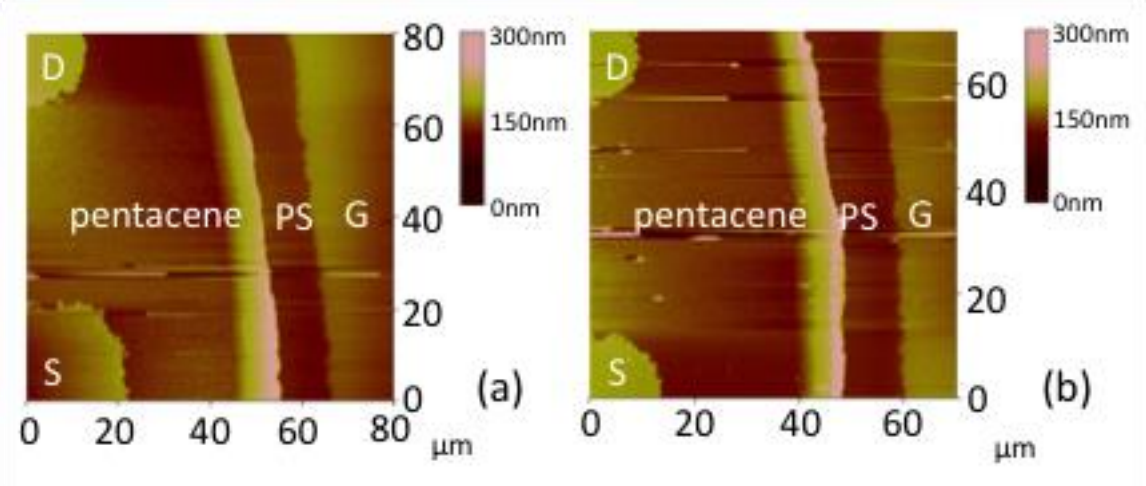

Figure S2. Height scans of the two samples from Figure 2 in the main text. The source (S), drain (D) and gate (G) are indicated in addition to pentacene and PS. Note that the edge of the pentacene closest to the PS has a slight height increase.

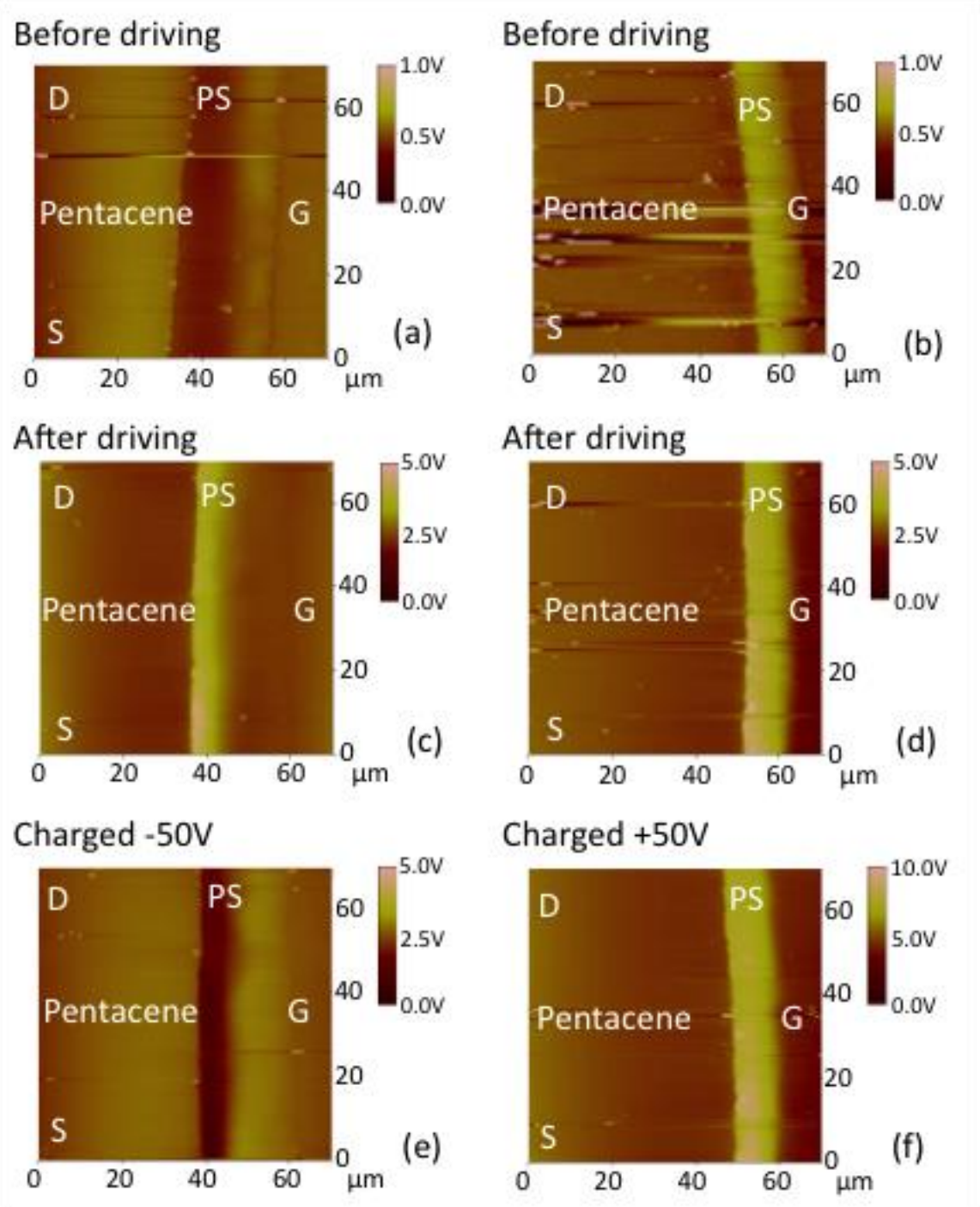

Figure S3. KPM scans of two separate samples (a,c,e) (b,d,f). In all images the source and drain electrodes are on the top and bottom of the left side while the gate electrode is on the right side. The samples are first imaged before electrical testing (a,b). After the transistor electrical measurements the samples are scanned (c,d). The samples were then charged to -50 V (e) and +50 V (f) for 10 minutes and rescanned.

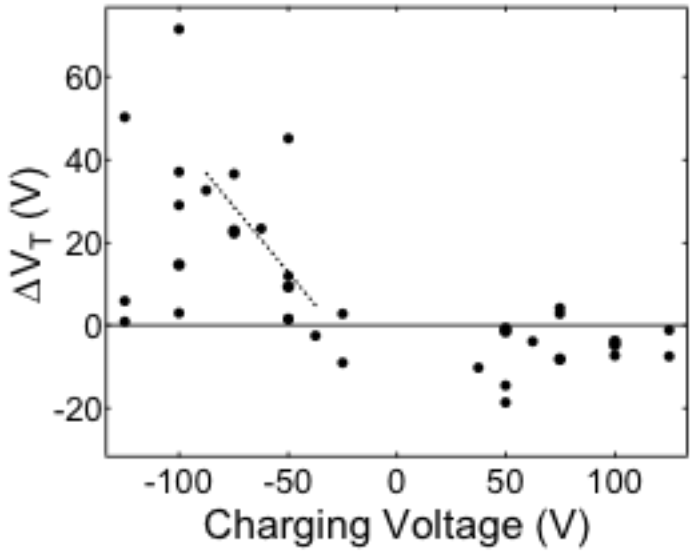

Figure S4. Dependence of V_T shift on charging voltage. The dotted line indicates the region where the correlation is strong. Above 100 V, the devices break down. At positive charging voltages, the correlation is poorer than for negative charging voltages.

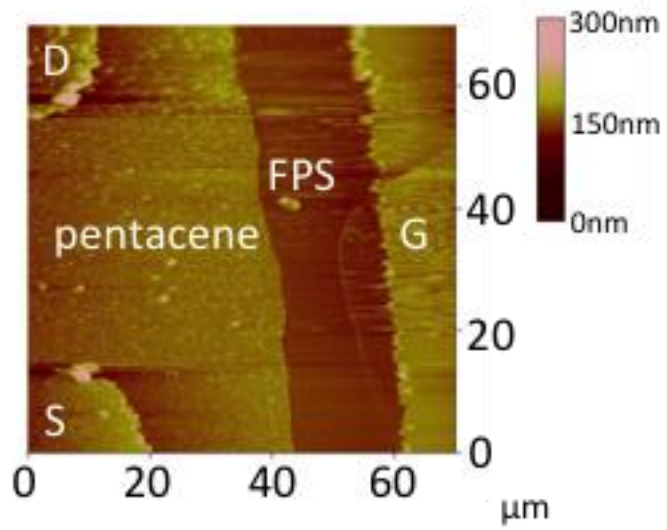

Figure S5. KPM height scan from the F-PS sample (Figure 9 main text) with all the features labeled.

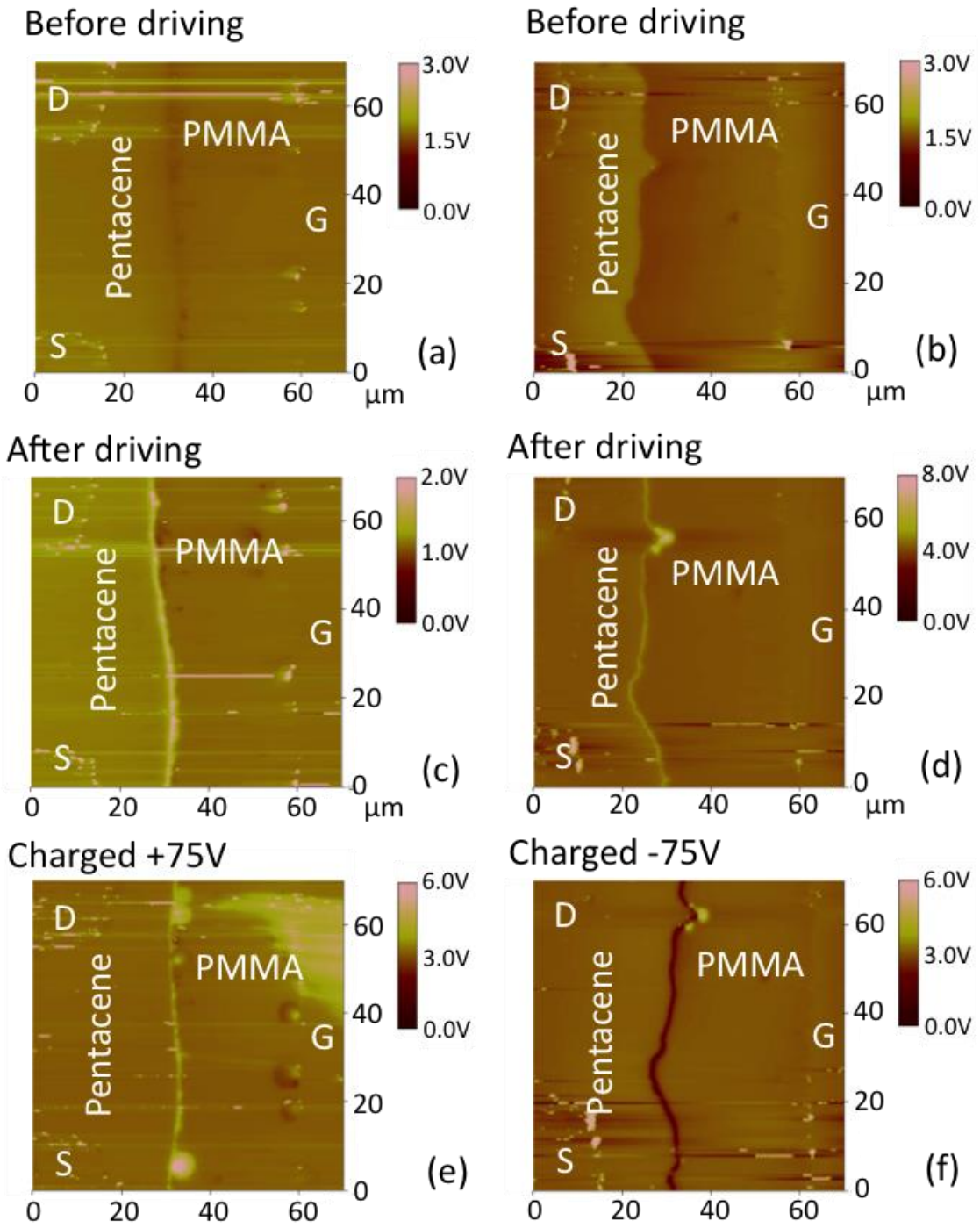

Figure S6. KPM scans of two separate PMMA samples (a,c,e) (b,d,f). In all images the source and drain electrodes are on the top and bottom of the left side while the gate electrode is on the right side. The samples are first imaged before electrical testing (a,b). After the transistor electrical measurements the samples are scanned (c,d). The samples were then charged to +75 V (e) and -75 V (f) for 10 minutes and rescanned.

Bias stress experimental procedure

Conventional "vertical" OFETs were fabricated to see the bias stress behavior of pentacene on PS and F-PS. Polymer dielectric solutions were deposited by spin coating on heavily n-doped Si wafers with 100nm thermally grown oxide. PS and F-PS were deposited by spin coating at 2000 RPM for PS and 1000 RPM for F-PS, the same manner as with the lateral transistors. To pre-charge the dielectrics the samples were corona charged with the indicated grid potential as in out previous work [6]. 50 nm of Pentacene was thermally evaporated at a rate of 0.3 Å/s. Top contacts of 50 nm of gold were thermally evaporated using a shadow mask at a rate of 0.5 Å/s. The OFET transfer and output curves were taken, then the device was subjected to a bias stress with V_g and V_d held at -45 V while V_s was grounded.

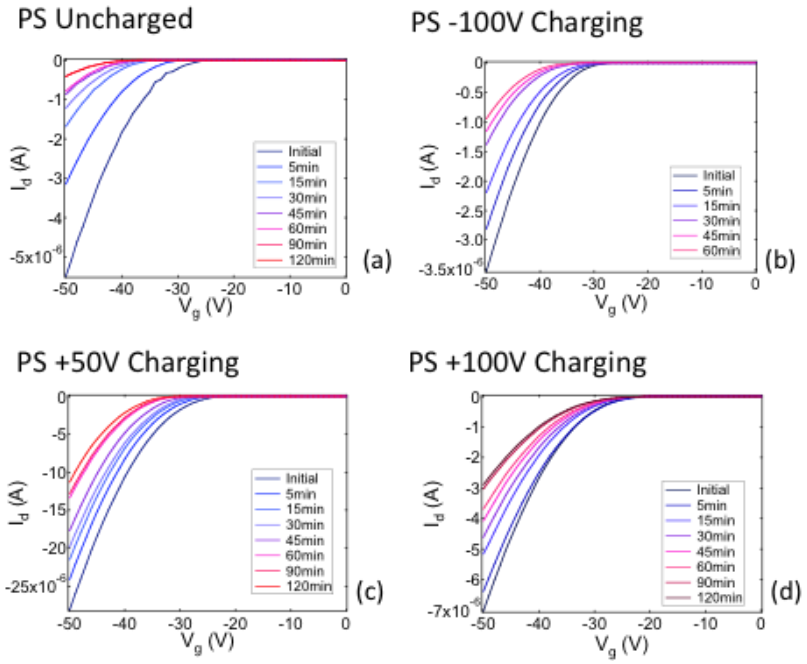

Figure S7. Bias stress behavior of PS dielectrics at various charging levels: uncharged (a), -100 V (b), +50 V (c), and +100 V (d). Note the difference in scales.