Two-Dimensional Pattern Formation Using Graphoepitaxy of PS-*b*-PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication

Hsinyu Tsai[*1], *Jed W. Pitera*[2], *Hiroyuki Miyazoe*[1], *Sarunya Bangsaruntip*[1], *Sebastian U. Engelmann*[1], *Chi-Chun Liu*[3], *Joy Y. Cheng*[2], *James J. Bucchignano*[1], *David P. Klaus*[1], *Eric A. Joseph*[1], *Daniel P. Sanders*[2], *Matthew E. Colburn*[3] *and Michael A. Guillorn*[1]

[1]IBM Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, New York 10598, United States

[2]IBM Research Almaden, 650 Harry Road, San Jose, California 95120, United States

[3]IBM Albany Nanotech Research Center, 257 Fuller Road, Albany, New York 12203, United States

* Address correspondence to htsai@us.ibm.com .

Supporting Information – Characteristics for FinFET Logic Circuits

The basic structure of the FinFET features a thin Si fin repeated at a given pitch, as shown in Figure 1S (a). It follows naturally that arranging a set of devices into a circuit will generate a grating-like pattern. However, it is inaccurate to characterize this pattern as a uniform, large area or single pitch grating. Breaks between groups of devices are required to facilitate CMOS device integration as well as accommodate local interconnects and other technology elements. Consequently, the resulting fin pattern is best described as a set of local small area or "structured" gratings with well-defined yet variable spacing or breaks between adjacent grating constructs.

Examples of FinFET logic and SRAM designs are shown in Figure 1S (b) and (c) respectively showing the gate and fin patterning. These designs were taken from a 9 Track unidirectional

FinFET standard cell library developed to explore tradeoffs with unidirectional layout topologies.[8] While specific implementations of FinFET logic and SRAM circuits may vary from the designs shown here, these layouts provide an example of the requisite constructs required for patterning basic FinFET circuits. The fin constructs are shown in Figures 1S (d) and (e) with labeling that indicates specific pattern requirements including (1) 3 fin blocks (2) 4 fin blocks (3) 2 fin blocks (4) breaks between groups of fins (5) transitions between different numbers of fins and (6) semi-isolated fins.

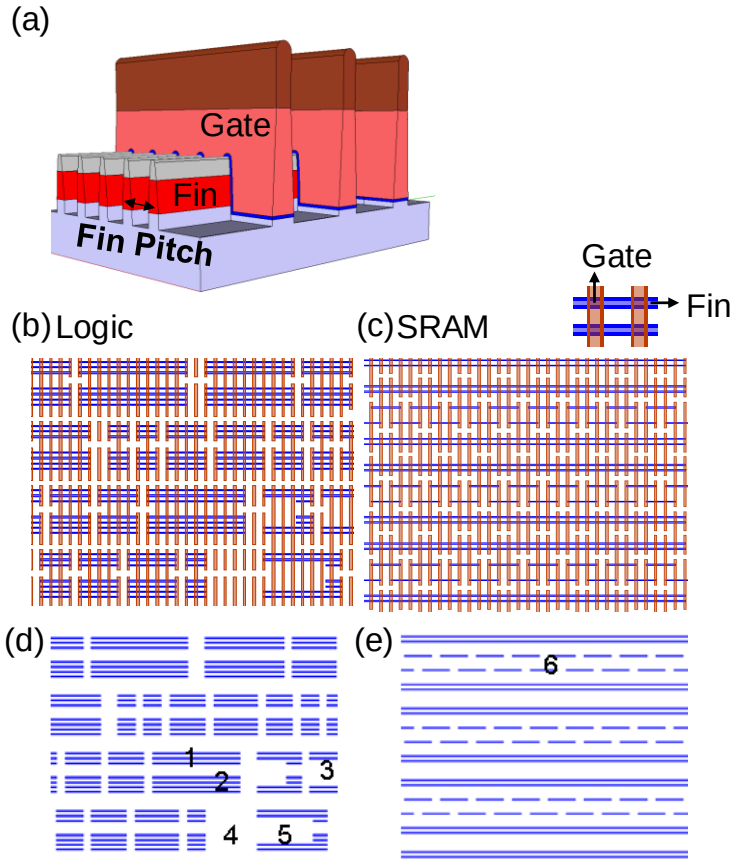

Figure 1S FinFET structure and FinFET circuit pattern examples. (a) shows a three-dimensional drawing of a basic FinFET device that consists of a group of fins spaced with a certain fin pitch and a common gate line that controls the fin channels. One FinFET device can contain multiple fins to drive more current and the spacing between groups of fins ensures that neighboring devices does not merge during source drain epitaxial growth. (b) FinFET logic and (c) SRAM design examples. The gate pattern is oriented along the vertical direction. The fin pattern is oriented in the horizontal direction. Basic fin pattern constructs in these examples include 3 fin blocks, 4 fin blocks, 2 fin blocks, breaks between groups of fins, transitions between different numbers of fins, and semi-isolated fins.

The process for introducing the fin free regions transverse to the long axis of the fin is shown in Figure 2S. The fin constructs are extracted from a circuit layout and decomposed into two patterns: the template pattern and the cut mask pattern. Following formation of the grating-like fin features in SOI, the vertically oriented breaks in the fin pattern are introduced using a subsequent lithographic exposure and plasma etch process. Details of this process are presented in another work.[8]

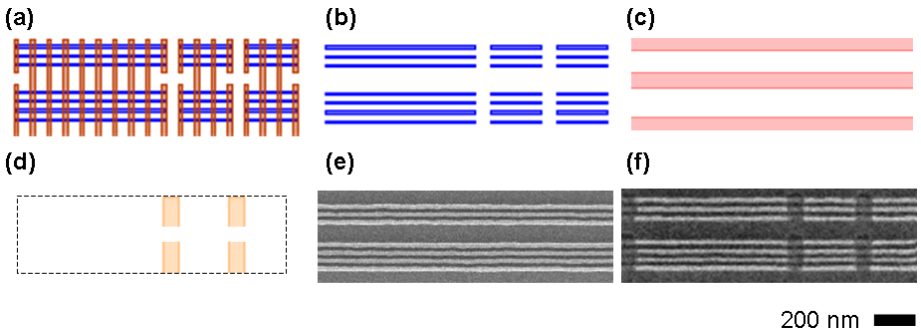

Figure 2S Circuit patterning process overview. (a) FinFET logic cell design (b) extraction of fin constructs (c) generation of template pattern (d) generation of cut mask pattern (e) SOI fins after DSA and (f) after cut mask. The pitch of all dense lines is 29 nm.