# Support Information

# Ternary Bulk Heterojunction Photovoltaic Cells Composed of Small Molecule Donor Additive as Cascade Material

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**Figure S1.** Transfer characteristic of DTDCTB Bottom-gated field-effect transistors using dielectric layer of $SiO_2$.

**Figure S2.** Atomic force microscopy (AFM) images of (a) P3HT: $PC_{61}BM$ (1: 1), (b) P3HT: DTDCTB: $PC_{61}BM$ (0.9: 0.1: 1), (c) P3HT: DTDCTB: $PC_{61}BM$ (0.8: 0.2: 1), (d) P3HT: DTDCTB: $PC_{61}BM$ (0.7: 0.3: 1), and (e) P3HT: DTDCTB: $PC_{61}BM$ (0.6: 0.4: 1).

**Figure S3.** *J-V* characteristics of the ternary devices of P3HT/DTDCTB/$PC_{61}BM$ with various weight ratios and binary device of P3HT/$PC_{61}BM$ fabricated without DIO as solvent additive.

**Figure S4**. *J-V* characteristic of the binary blend device of DTDCTB/$PC_{61}BM$ fabricated as the same process of the device of P3HT/$PC_{61}BM$.

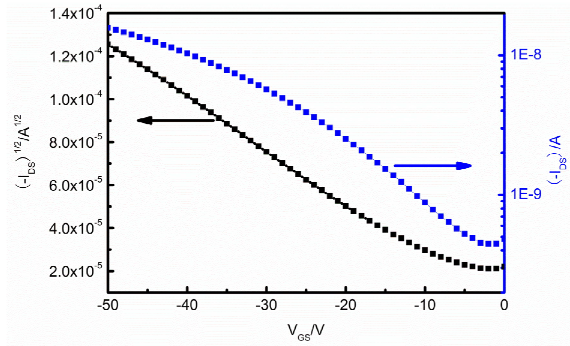


**Figure S1** Transfer characteristics of DTDCTB TFT using dielectric layer of $SiO_2$. ($V_{DS}$ =-50 V, W=1 mm, and L=150 μm.)

To fabricate the FET device based DTDCTB, a heavily n-doped silicon wafer with a 300 nm thickness $SiO_2$ was chosen as the substrate. The substrate was firstly cleaned ultrasonically in acetone and isopropyl alcohol (IPA) for 10 minutes, respectively. A thin film of DTDCTB was stun cast on the top of $SiO_2$, then evaporated under a high vacuum. Finally, gold source-drain electrodes with a thickness of 40 nm were evaporated with a shadow mask to get a channel length of $L$ = 150 μm and channel width of $W$ = 1 mm.

As shown as figure S1, the bottom-gate field-effect transistor of DTDCTB is investigated, and the hole mobility in extracted saturation regime is $1.18\times10^{-4}$ $V^{-1}$ $s^{-1}$.

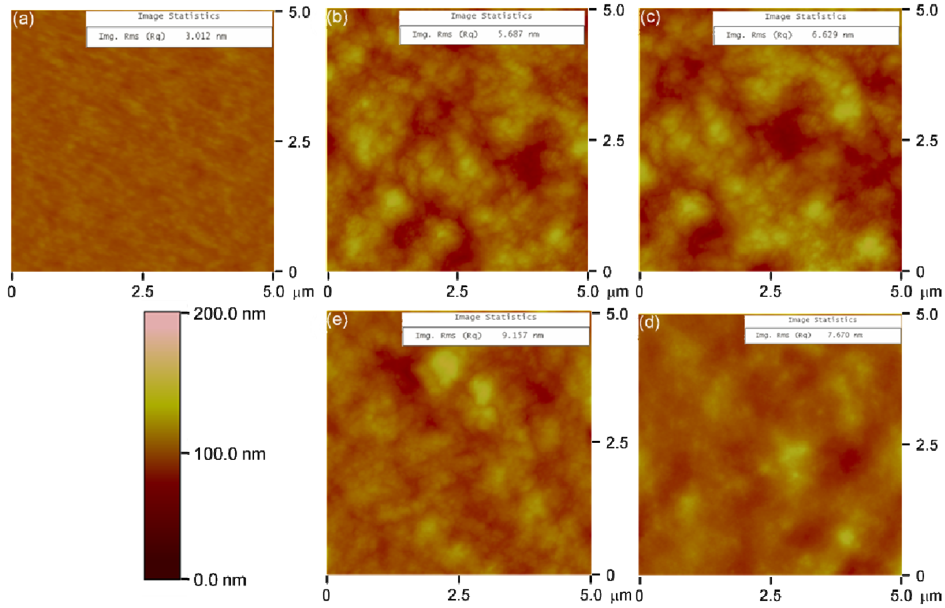


**Figure S2** Atomic force microscopy (AFM) images of (a) P3HT: $PC_{61}BM$ (1: 1), (b) P3HT: DTDCTB: $PC_{61}BM$ (0.9: 0.1: 1), (c) P3HT: DTDCTB: $PC_{61}BM$ (0.8: 0.2: 1), (d) P3HT: DTDCTB: $PC_{61}BM$ (0.7: 0.3: 1), and (e) P3HT: DTDCTB: $PC_{61}BM$ (0.6: 0.4: 1)

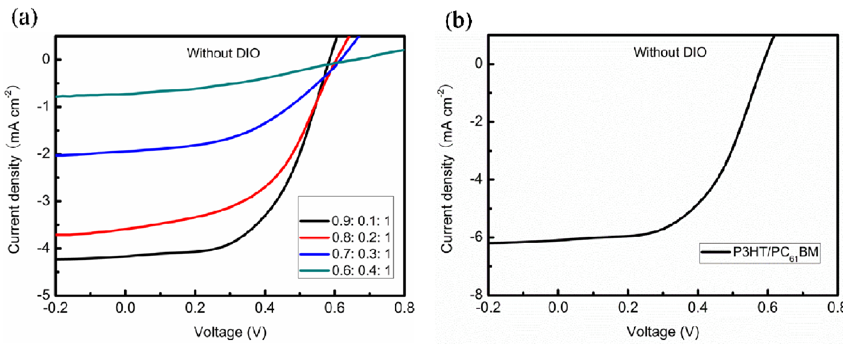


**Figure S3.** (a) *J-V* characteristic of the ternary device of P3HT/DTDCTB/$PC_{61}BM$ with various weight ratios fabricated without DIO as solvent additive. (b) *J-V* characteristic of the binary device of P3HT/$PC_{61}BM$ (1: 1) fabricated without DIO as solvent additive.

The ternary P3HT/DTDCTB/$PC_{61}BM$ and binary P3HT/$PC_{61}BM$ solar cells were fabricated following the methods reported previously for P3HT-based solar cells with solvent additives. [1-5] In these solar cells, the DIO solvent additive helps to control the morphology and nanoscale phase separation of the donor/acceptor interpenetrating network in the active layer. [4, 5]

As shown in Figure S3, the devices without DIO solvent additive demonstrate low performances.

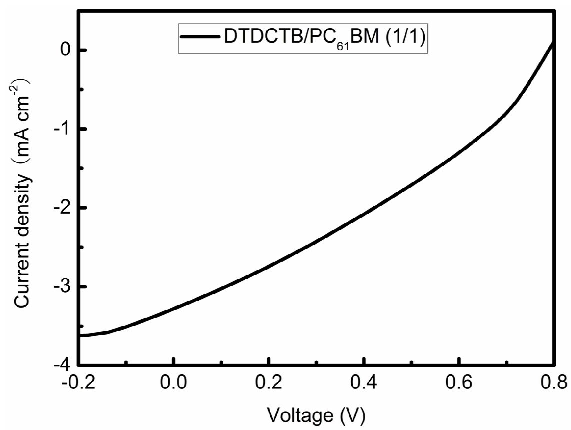


**Figure S4**. *J-V* characteristic of the binary blend device of DTDCTB/$PC_{61}BM$ fabricated as the same process of the device of P3HT/$PC_{61}BM$.

The binary blend device of DTDCTB/$PC_{61}BM$ demonstrated a PCE of 0.85%, with an open circuit voltage ($V_{OC}$) of 0.78 V, a short circuit current ($J_{SC}$) of 3.28 mA/cm$^2$ and FF of 0.33.

## References

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