Supporting Information for

Integration of SrTiO₃ on Crystallographically Oriented Epitaxial Germanium for Low-power Device Applications

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1. Synthesis and x-ray diffraction studies of SrTiO₃ target

The synthesis of the SrTiO₃ (STO) target was performed using a conventional solid state reaction method. For this, high purity $SrCO_3$ and TiO_2 was ball-milled under ethanol for 24h followed by drying at 80°C for 6h. The powder thus obtained was calcined at 800-1000°C for 2h and then subjected to ball milling for 48h under ethanol. After drying, powder thus obtained was pressed in to a cylindrical target using uniaxial press followed by cold-isostatic pressing to achieve high green density. The pressed target was sintered at 1350°C for 2h to achieve high relative density (>98%). In order to confirm the formation of pure perovskite phase of STO target, x-ray diffraction (XRD) spectrum was recorded at room temperature (Figure S1). The XRD spectrum clearly indicates that STO target was crystallized in pure perovskite phase. The high relative density and absence of secondary phase suggests high quality of STO target. This STO target was used for the deposition of thin STO layer on crystallographic oriented (100)Ge, (110)Ge and (111)Ge using pulsed laser ablation.
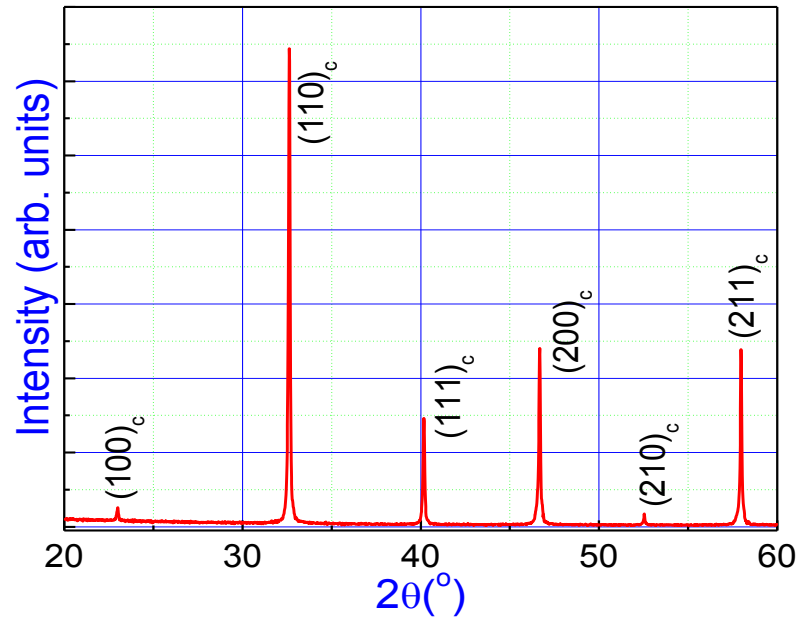
Figure S1. Shows the XRD spectrum recorded from the sintered SrTiO$_3$ ceramics target at room temperature. It clearly indicates that STO target was crystallized (c) in pure perovskite phase.

2. Process flow for fabricating metal/STO/Ge metal-insulation-semiconductor (MIS) contacts

The following process steps were used to fabricate metal/STO/Ge metal-insulator-semiconductor (MIS) contacts:

1) Solvent Clean: 1 min in acetone followed by1 min in isopropyl alcohol (IPA) followed by 1 in min deionized water (DI H$_2$O) and followed by 30 sec in DI H$_2$O faucet rinse.

2) Level 1 Lithography (Negative photoresist) → *Define the contact area prior to metallization*

The contact areas were defined prior to metal deposition.

3) Metallization → *50 nm Ti followed by 50 nm Au*

Deposit 50nm Ti/50nm Au using Kurt J. Lesker E-beam 250 system at 6e-6 Torr deposition pressure.

4) Lift-off → *Remove the unwanted metals, leaving only the contact pads*

Sonicate each samples (while in acetone) for *1 min*, continuing in *1 min* intervals as needed to remove the remaining metal.

3. Process flow for transmission line measurement (TLM)

The following process steps were used to fabricate metal-insulator-semiconductor (MIS) contacts:

1) Solvent Clean: 1 min in acetone followed by1 min in isopropyl alcohol (IPA) followed by 1 in min DI H_2O and followed by 30 sec in DI H_2O faucet rinse.

2) Level 1 Lithography (Positive) → *Define the mesa region that will be etched and protect the area to be contacted*

AZ 5214 E-IR positive photoresist was used for mesa areas and the spin parameters 5 sec /55 sec / 5 sec @ 500 RPM / 3000 RPM / 500 RPM were used during the contact fabrication process. AZ 400K [diluted in DI H_2O to a 1:3 volume ratio] developer was used for the fabrication process. The detailed process steps were used in this study:

a) *1 min* dehydrate bake at 110°C followed by a *30 sec* cool down;

b) Spin the resist using the above parameters and allow to 'set' for *30 sec* after spinning;

c) *1 min 20 sec* hard bake at 110°C followed by a *30 sec* cool down;

d) Expose for *7 sec* under UV (405 nm wavelength) using a hard-contact alignment mode with a 120 μm final alignment gap between wafer and mask;

e) Develop for *50 sec* using the above developer;

f) *1 min* hard bake at 110ºC prior to wet etching.

3) Mesa Etch → Etch the STO layer, then etch the epitaxial Ge layer down to the GaAs

- STO etchant: (6:1) BOE [diluted in DI H_2O to a 1:3 volume ratio] was used in this process.

- Ge etchant: [2:1:200 volume ratio of $NH_4OH:H_2O_2:H_2O$] (SC-1) was used to etch the ge epilayer.

a) *10 sec* STO etch in dilute BOE followed by a standard solvent clean as listed in **Step 1** above;

b) Measured the depth using Dektak (surface profilometer) prior to removing resist.

4) Solvent Clean: See **Step 1**. Double check etch depth using Dektak (surface profilometer) after removing resist.

5) Level 2 Lithography (Negative) → Define the contact area prior to metallization.

i) Same resist/spin/develop parameters used in **Step 1**. ii) Repeat process steps a) through d) as indicated in **Step 1**; iii) *2 min* reverse bake at 110ºC followed by a 30 sec cool down; iv) *40 sec* flood exposure under UV (405 nm) using no mask; v) Develop for *13 sec* using the developer as listed in **Step 1**.

6) Metallization → Deposit 50 nm Ti followed by 50 nm Au

Deposit 50nm Ti/50nm Au using Kurt J. Lesker E-beam 250 system at 6e-6 Torr deposition pressure.

7) Lift-off → Remove the unwanted metals, leaving only the contact pads

 a) Sonicate the samples (while in acetone) for *1 min*, continuing in *1 min* intervals as needed to remove the remaining metal.

b) Follow the standard solvent clean procedure as listed in **Step 1**. The optical image of the fabricated TLM sample is shown in Figure S2.
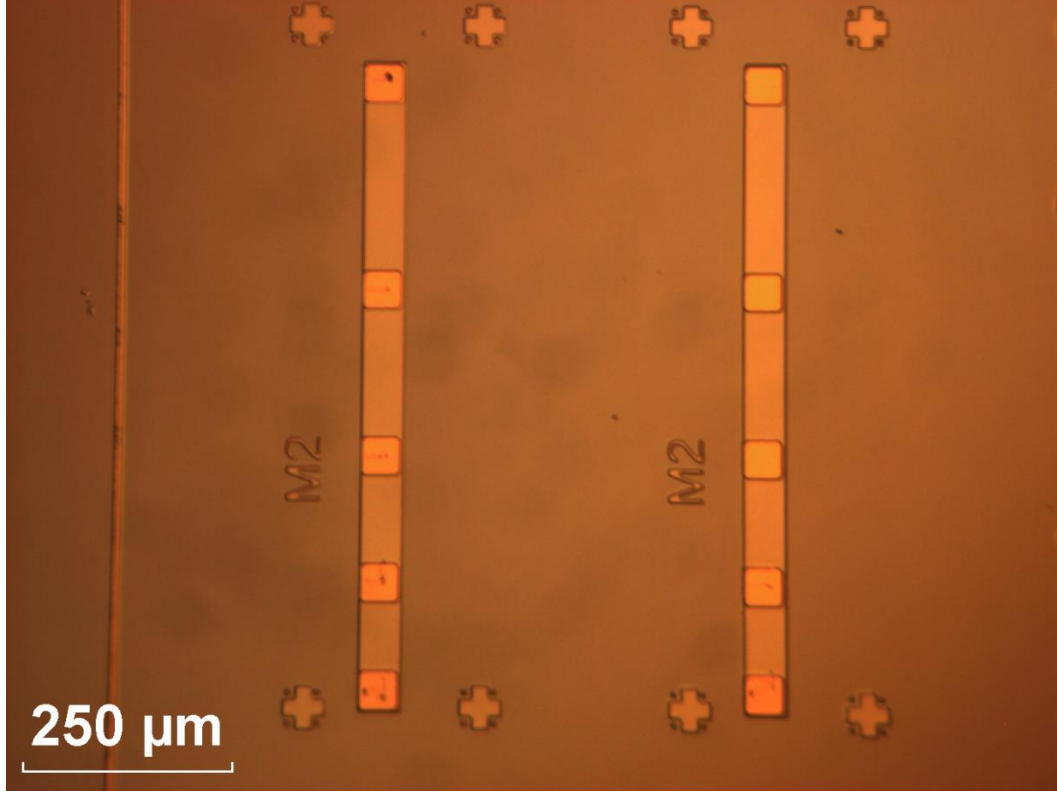

Figure S2. Optical image of fabricated TLM pattern for contact resistance measurement.

3. MOS capacitor electrical characteristics

In order to validate whether STO can be used as a gate dielectric on n-Ge besides being used as a MIS contact, we have fabricated Al/STO/Ge metal-oxide-semiconductor (MOS) capacitors with and without interfacial layers inserted in between the STO and the n-Ge. If the STO can be used as a standalone gate dielectric on n-Ge, the gate leakage should be kept to a minimum. Figure S3a shows the gate leakage current density as a function of gate voltage with standalone 8nm

STO/Ge and 8nm STO/3nm Al_2O_3/0.8nm GeO_2 layer on n-Ge. One can find from this figure that the leakage current density for the standalone STO gate stack is the same order of magnitude as the 3 nm STO MIS contact due to the lower ΔE_c of STO on n-Ge. The insertion of the 0.8nm GeO_2 and 3 nm Al_2O_3 dielectric layers into the gate stack creates an additional ~4 nm thick interfacial layer with high ΔE_c, thereby increasing the tunneling barrier height at the interface, and thus reducing the tunneling current of the device by 10^8 as compared to the standalone STO/n-Ge gate stack.

We have further evaluated the applicability of STO as a gate dielectric through capacitance-voltage (C-V) measurements as a function of frequency. Figure S3b and S3c shows the measured C-V data for a fabricated 8nm STO/n-Ge and 8nm STO/3nm Al_2O_3/0.8nm GeO_2/n-Ge MOS capacitors, respectively. As shown in Fig. S3b, the gate stack without the interfacial layer exhibits a large frequency dispersion (~44%) and substantial contribution of leakage current to the capacitance. On the other hand, the inclusion of 0.8nm GeO_2 and 3nm Al_2O_3 interlayers in between the STO and n-Ge passivates the n-Ge interface and reduces the leakage current contribution to the C-V characteristics, as supported by Fig. S3a. Moreover, these interlayers significantly reduces the frequency dispersion from 44% down to ~10%. Hence, STO can only be used as a MIS contact to the source/drain of n-Ge and is not suitable as a standalone gate dielectric to n-Ge.
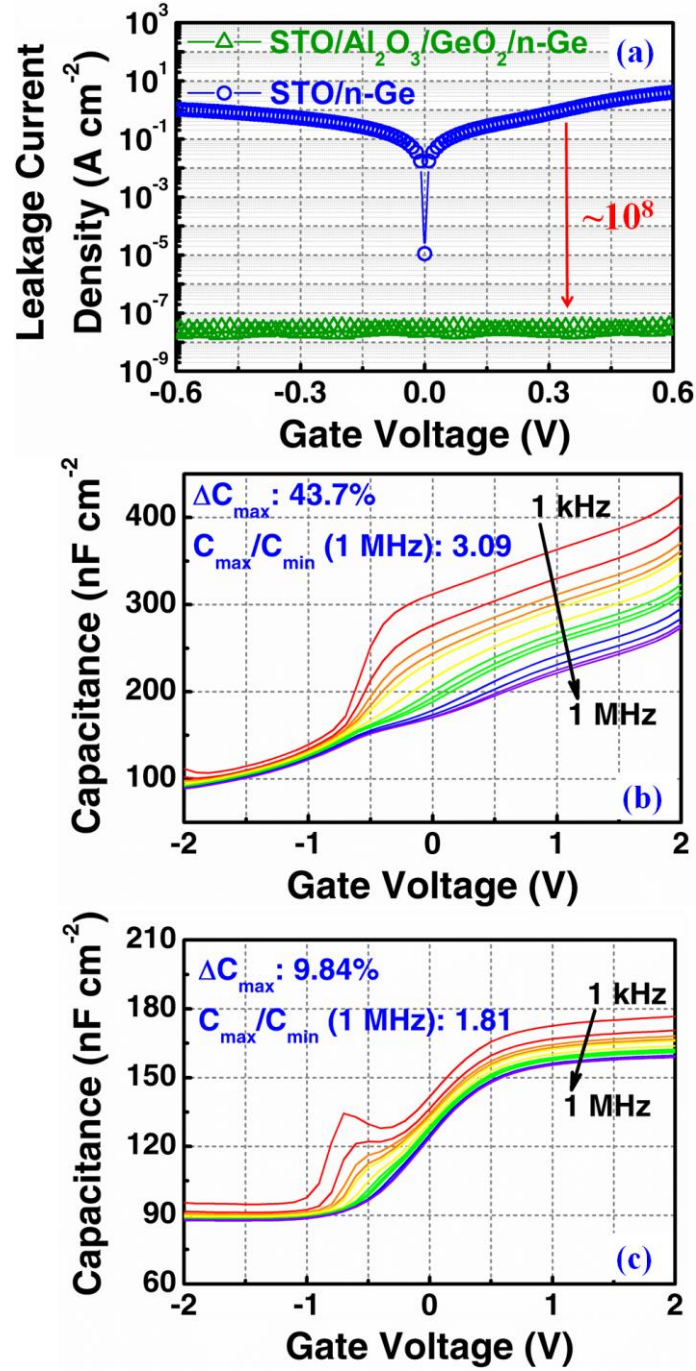
Figure S3. (a) Leakage current density as a function of gate voltage with standalone 8nm STO/Ge and 8nm STO/3nm Al_2O_3/0.8nm GeO_2 layer on Ge, (b) capacitance-voltage (C-V) characteristics of 8nm STO/Ge, and (c) C-V characteristics of 8nm STO/3nm Al_2O_3/0.8nm GeO_2 on Ge, respectively.