Supporting Information for "Scaling and graphical transport-map analysis of ambipolar Schottky-barrier thin-film transistors based on a parallel array of Si-nanowires"

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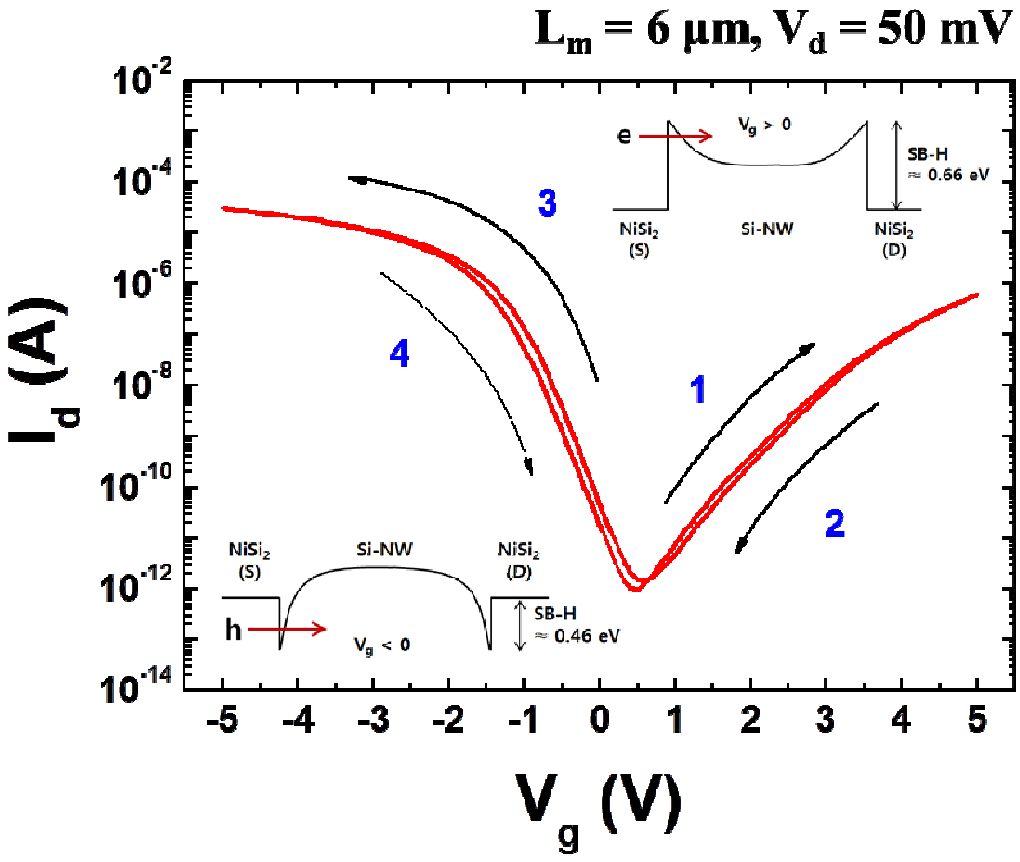


Figure S1. Transfer curve of the ambipolar SB-TFTs showing insignificant hysteresis effects. The hysteresis effects were also mostly vanished after annealing process in N_2 atmosphere at 300 ºC. The numbers in the plot denote a sweep direction of V_g (1 → 2 → 3 → 4) and the illustrations with the inset describe the injection probability of hole or electron strongly affected by a bias condition of V_g.

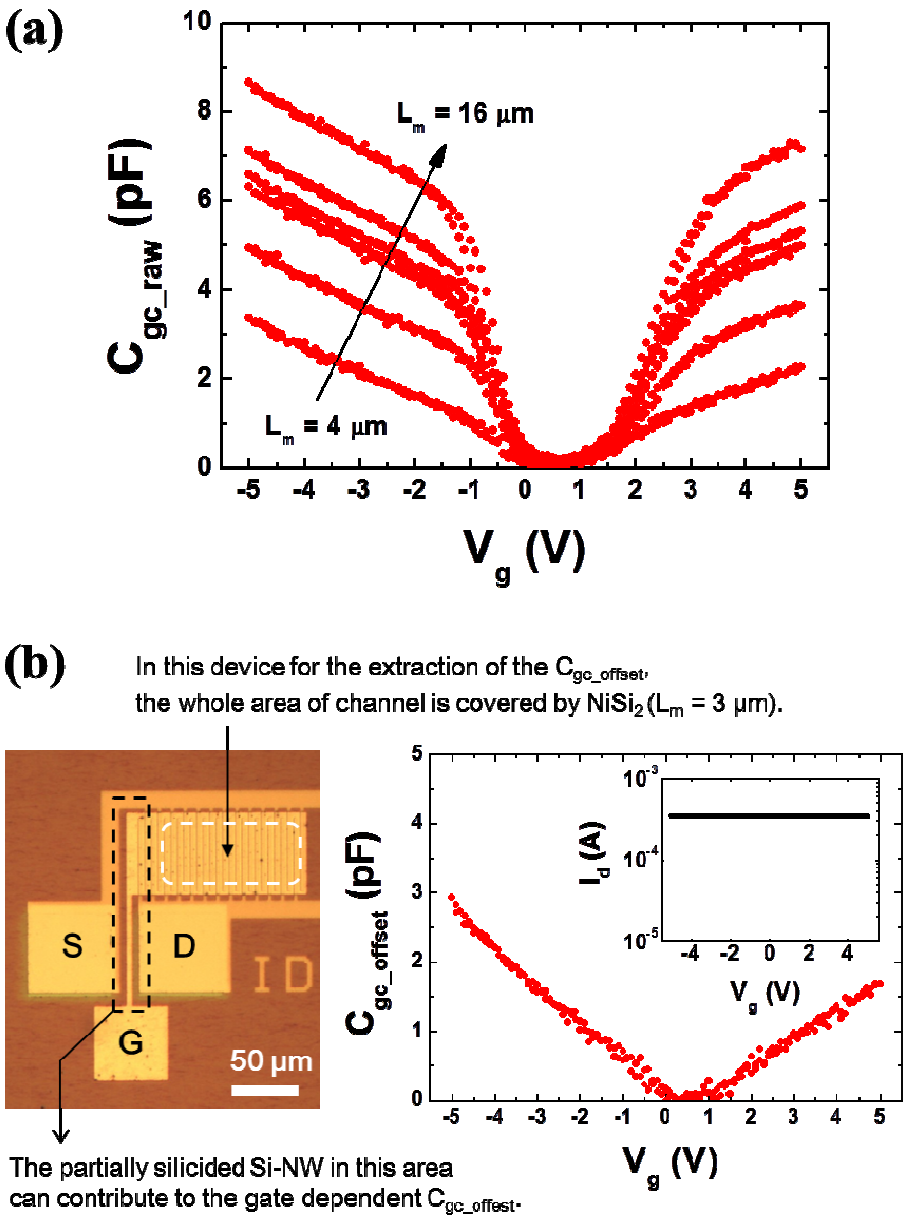
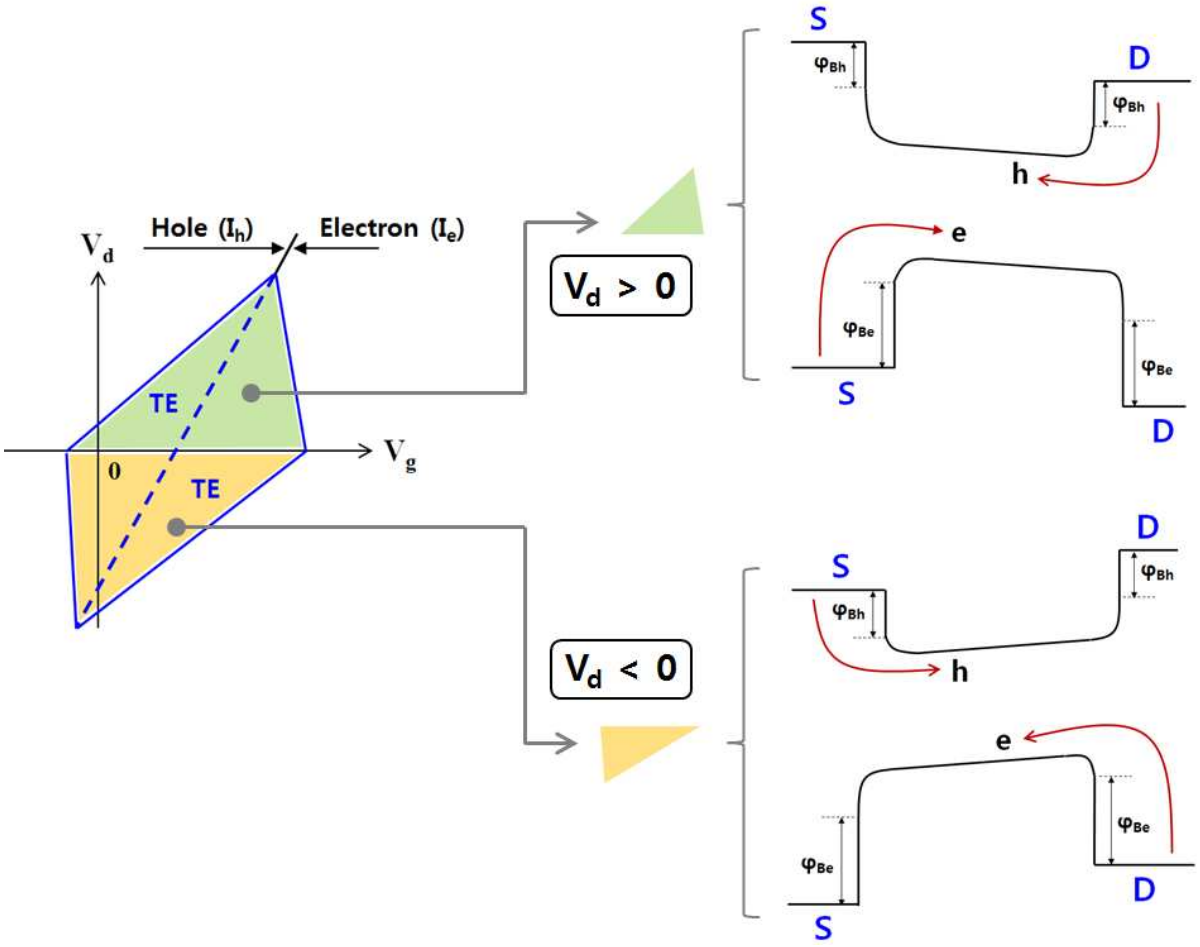


Figure S2. (a) The raw data of C_{gc} vs V_g as varying L_m. The capacitance isn't saturated even at high $|V_g|$ due to the gate dependent off-set capacitance (C_{gc_offset}) stemming from the particular structure of the device. (b) Optical microscope (OM) image of an ambipolar SB-TFTs, where the whole channel (the dotted white square) could be fully silicided with $NiSi_2$ and corresponding I_d and C_{gc} as a function of V_g. Constant I_d against V_g was observed in the inset, since I_d current mostly flows through a shortest path of $NiSi_2$ in the channel. Whereas, the gate dependent C_{gc} was interestingly obtained with the same device. Si-NW in parallel could exist on the whole area of substrate. This allows that the partially silicided Si-NW in the dotted black square can cause the C_{gc_offset}, even though it hardly contributes to I_d.



Figures S3. Schematic illustrating I-V map of thermionic emission (TE) dominant regime and possible band-diagram for I_h or I_e transport according to the sign of V_d bias. For $V_d > 0$ in the TE regime, I_h and I_e can be given as, individually: [1,2]

$$I_e \approx A^* T^2 \times \exp\left(\frac{-\varphi_{Be}}{kT/q}\right) \times \exp\left(\frac{V_g - V_s - V_c}{kT/q}\right) \quad \text{(S1)}$$

$$I_h \approx B^* T^2 \times \exp\left(\frac{-\varphi_{Bh}}{kT/q}\right) \times \exp\left(\frac{V_d - V_g + V_c}{kT/q}\right) \quad \text{(S2)}$$

With assumption of $I_h = I_e$ on the border line of transition in the I-V map, a linear function of V_d vs V_g can be obtain by:

$$V_d = 2V_g + (\varphi_{Bh} - \varphi_{Be}) - 2V_c + V_s + \frac{kT}{q}\ln\left(\frac{A^*}{B^*}\right) \quad \text{(S3)}$$

Finally, one can get a simple equation as followings, since $V_s = 0$ and $kT/q \times \ln(A^*/B^*)$ can be neglected at room temperature:

$$V_d \approx 2V_g + (\varphi_{Bh} - \varphi_{Be}) - 2V_c \quad \text{(S4)}$$

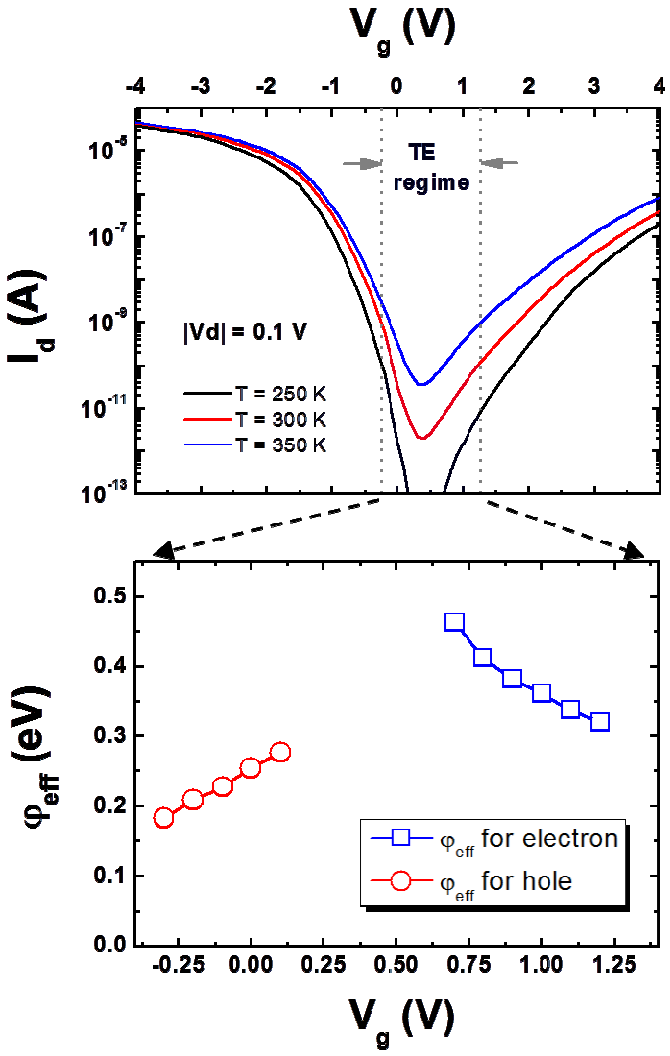
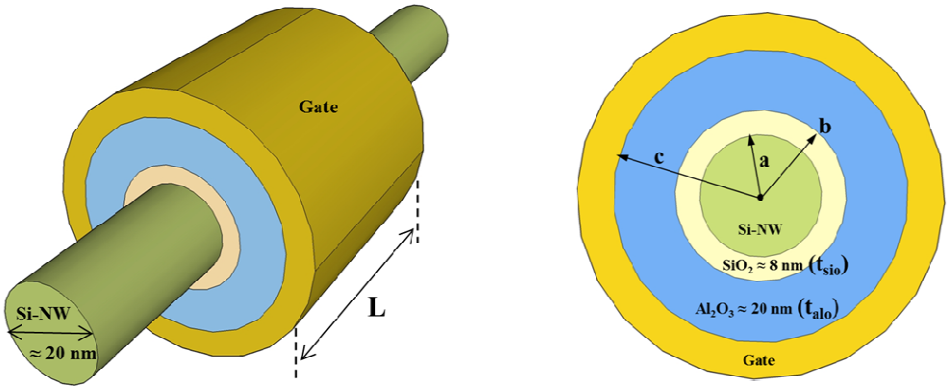


Figure S4. Temperature dependence of I_d vs. V_g (upper) and the effective barrier height φ_{eff} values extracted by $\ln(I_d/T^2) \approx -q/kT \times \varphi_{eff}(V)$ in the TE regime (lower), L_m = 6 μm. The φ_{eff} is still modulated by even V_g slightly beyond flat-band voltage within the TE regime where a very small amount of tunneling current is expected, due to the image force induced lowering of the effective barrier height.[1]



$$\frac{C}{L} = \frac{Q}{\Delta V} = \frac{2\pi}{\frac{1}{\varepsilon_{sio}} \cdot \ln\left(\frac{b}{a}\right) + \frac{1}{\varepsilon_{alo}} \cdot \ln\left(\frac{c}{b}\right)}$$

- a = radius of Si-Nanowire
- b = a + t_{sio} and c = b + t_{alo}
- ε_{sio} and ε_{alo} are permittivity of SiO_2 and Al_2O_3, respectively.

Figure S5. Illustration of a Si-NW transistor with a perfect surrounded gate. The equation denotes capacitance per unit gate length with two dielectric materials.[3,4] One can calculate a capacitance per unit area of nanowire surface ($C_{ox\_calcul.}$) as:

$$C_{ox\_calcul.} = \frac{C}{A} = \frac{C}{2a\pi \times L} = \frac{1}{a \times \left(\frac{1}{\varepsilon_{sio}} \times \ln\left(\frac{b}{a}\right) + \frac{1}{\varepsilon_{alo}} \times \ln\left(\frac{c}{b}\right)\right)} \quad \text{(S5)}$$

Then, the number of Si-NWs connected to source or drain was estimated as ≈ 1.6 × 10^3 with $C_{ox\_calcul.} = C_{ox\_meas.} = S/(2\pi a \times N)$, where A, S and N represent surface area of a single nanowire, slope of C_{gc} vs. L_m in the figure 3(b) and the number of Si-NWs, respectively. The value is comparable to that (≈ 1.0 × 10^3) from a statistical analysis using SEM, with considering variation of nanowire diameters and assumption regarding gate geometry.

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