Supporting Information

Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices

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I. Fabrication sequence and TEM image

A. Fabrication sequence

1. An 80-nm-thick TiN metal layer was deposited on a bulk silicon substrate via DC magnetron sputtering.
2. A solvent of methyl ethyl ketone was used to prepare a 1 wt% solution of $P(VDF_{0.75}\text{-}TrFE_{0.25})$ ferroelectric material.
3. The $P(VDF_{0.75}\text{-}TrFE_{0.25})$ solution was heated on a hot plate (at 60 °C) for more than 1 h.
4. This sample was spin coated on top of the TiN layer at 1500 rpm for 30 s.
5. It was then annealed on a hot plate at ~140 °C for approximately 1 h.
6. A top gold electrode was deposited via a thermal evaporation method.

B. TEM image

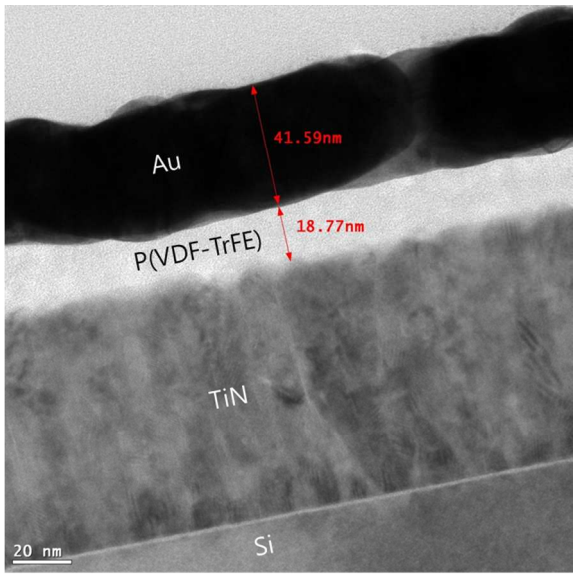

Figure S1. A cross-sectional TEM image of a $P(VDF_{0.75}\text{-}TrFE_{0.25})$ organic/ferroelectric capacitor. Gold electrode thickness = 41.59 nm, $P(VDF_{0.75}\text{-}TrFE_{0.25})$ ferroelectric insulation layer = 18.77 nm, TiN metal layer = 80 nm.

II. Coercive voltages of the fabricated organic/ferroelectric capacitor

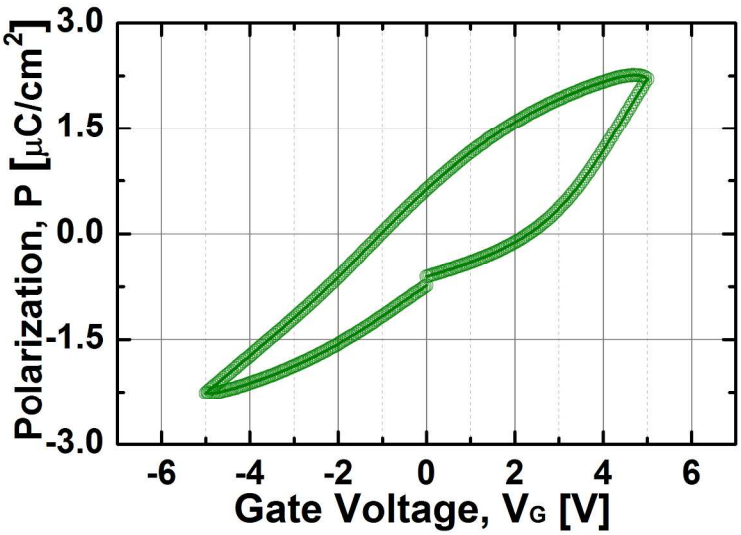

Figure S2. Polarization vs. gate voltage curve of a P($VDF_{0.75}$-$TrFE_{0.25}$) organic/ferroelectric capacitor.

- The coercive voltages of the organic/ferroelectric capacitor are −1 V and +2.3 V.
- In order to achieve the phase transition in the ferroelectric material, the gate voltage was varied from − 5 V to + 5 V, thus exceeding the positive and negative coercive voltages.

III. Input transfer characteristic of the NMOS transistor used in this study

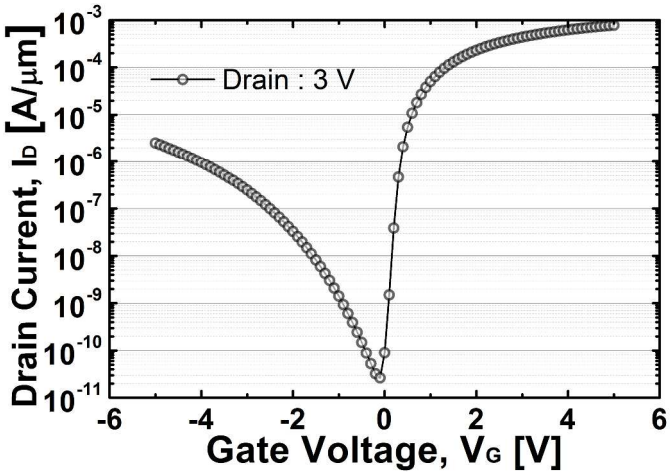

Figure S3. Drain current vs. gate voltage of the NMOS transistor.

- The subthreshold slope of the NMOS transistor is **92 mV/decade** at 300 K.

IV. Measurement setup

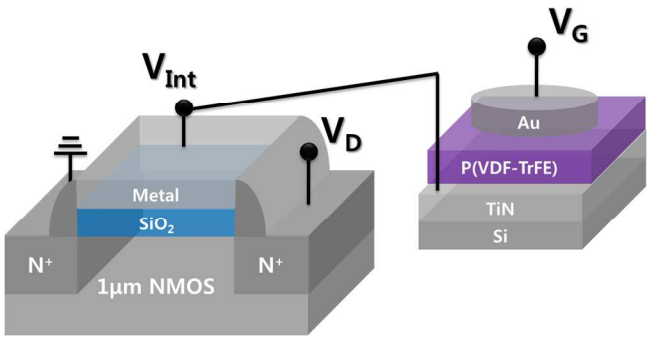

Figure S4. Series connection of the "ferroelectric capacitor plus MOS device."

- In order to confirm the negative capacitance of the ferroelectric capacitor, the organic/ferroelectric capacitor was connected in series with the gate electrode of the NMOS transistor using a gold wire.

V. Reproducibility of negative capacitance effect in the MOS transistor

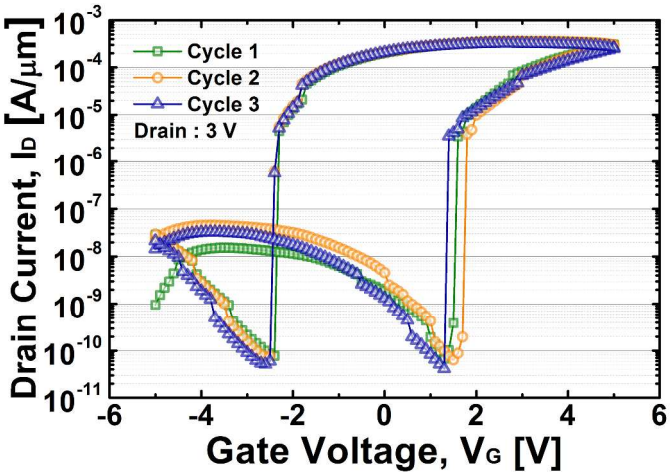

Figure S5. Drain current vs. gate voltage.

- The negative capacitance effect in the MOS device was observed and confirmed repeatedly. **Subthreshold slope less than 60 mV/decade was demonstrated over five decades of drain current** (i.e., 10^{-10} A/μm to 10^{-5} A/μm).

VI. Hysteresis

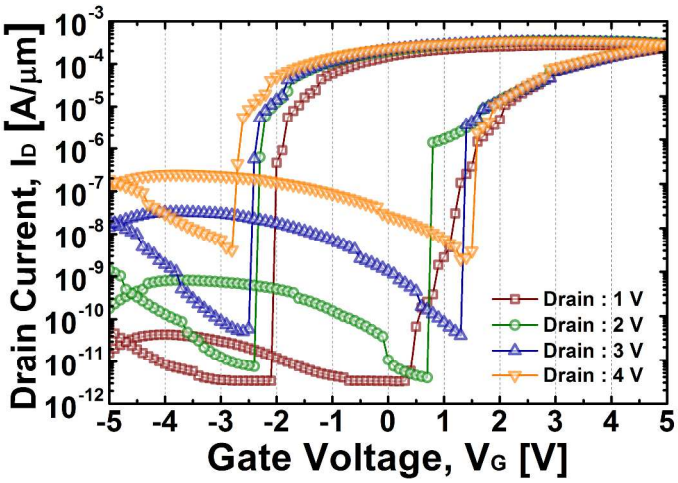

Figure S6. Hysteresis in drain current vs. gate voltage with different drain voltage

- As shown in **Fig. S6**, a threshold voltage window was observed because of the remnant polarization of the organic/ferroelectric capacitor. In previous studies, methods to reduce or remove the hysteresis were suggested: If the dielectric capacitor [1] or resistance [2] is connected in series with the organic/ferroelectric capacitor, the negative capacitance can be achieved in a stable state. In addition, by connecting a nanoelectromechanical system (NEMS) in series with a ferroelectric capacitor, the energy state of the combined device (i.e., NEMS plus capacitor) can be stabilized [3].

[1] Salahuddin, S.; Datta, S. *Nano Lett.* 2008, 8, 405−410.

[2] Khan, A.; Chatterjee, K.; Wang, B.; Drapcho, S.; You, L.; Serrao, C.; Bakaul, S.; Ramesh, R.; Salahuddin, S. *Nat. Mat.* 2015, 14.2, 182-186.

[3] Masuduzzaman, M.; Alam, M. *Nano Lett.* 2014, 14, 3160−3165.

VII. Gate leakage current

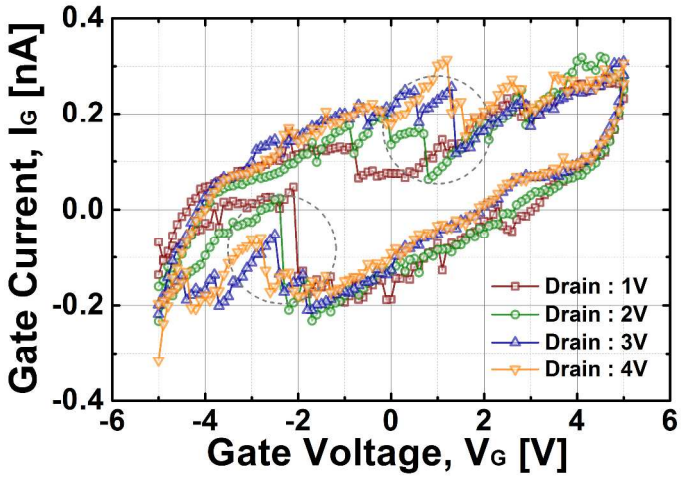

Figure S7. Gate leakage current vs. gate voltage in the NMOS transistor with the organic/ferroelectric capacitor.

- As shown in **Fig. S7**, the gate leakage current is sharply varied in the negative capacitance region (see the two dashed-line circle regions in Fig. S7). In addition, the gate leakage current of the NMOS transistor with the organic/ferroelectric capacitor is approximately − 0.3 to + 0.3 nA in the NMOS transistor. This result indicates that the steep switching behavior does not originate from the breakdown of the gate insulation layer. By comparing the internal voltage gain (see Fig. 3) with the measured gate leakage current, we can conclude that the steep switching behavior does not result from tunneling, insulation layer breakdown.