Supporting Information: "Si donor incorporation in GaN nanowires"

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Supplementary information 1:

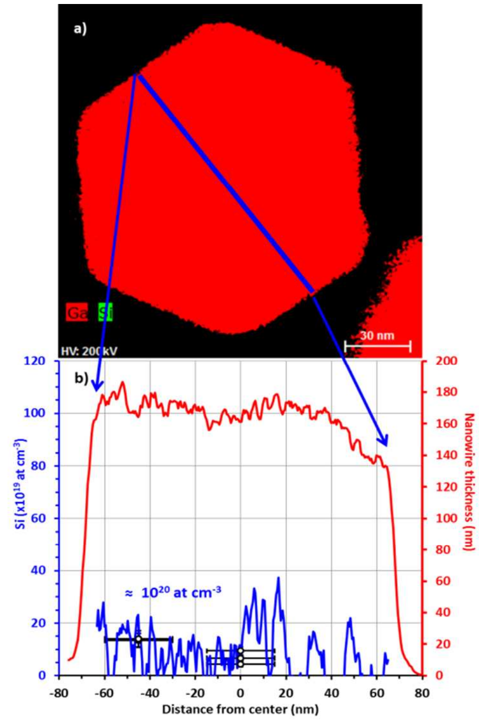

Figure S1: TEM-EDX (blue line profile in (b)) and SEM-EDX data (white circles in (b)) on sample 5, TEM-EDX shows a relatively constant Si concentration throughout the NW with an average value of 1 x 10^{20} at/cm^3, and it is consistent with concentrations measured by SEM-EDX with the FlatQuad annular detector (0.5~1.5 x 10^{20} at/cm^3). Two elements are highlighted in (a), with green and red corresponding Si and Ga, respectively. The NW thickness of the STEM observation is shown on the red curve in (b).

Supplementary information 2:

In our simulation, the device is modeled as a cut in the (y, z) cross section plane direction. GaN NW was modeled as a hexagon. The oxide, BG and LG were modeled as rectangles with the corresponding dimensions (see Figure 6(f) and (g)). The device is simulated at Vsd = 0 V to electrostatically model the charge depletion at a certain gate voltage. Firstly we presume a doping level of the NW as an input parameter, and then by applying a small voltage sweep of either BG or LG, the NW is gradually depleted as shown in Figure 6 (h, j, l) and (i, k, m), respectively. Thanks to NextNano[3], the 2D electron density in the NW at each voltage sweep step can be visualized by considering all the device geometry and materials properties, as well as solving the Poisson equation self-consistently. As shown in Figure 6, the electron density in the NW cross section at zero gate voltage is 1 x 10^{18} at / cm^3, which is the input doping level. The NW is gradually depleted of carriers when applying a negative gate bias with the BG or the LG. Noticeably, The depleted region starts from the bottom of the NW, and gradually increases when applying a BG; whereas, the NW is depleted starting from the right side when using a LG. When applying a small gate voltage, we have

$$C\,(N_d) = \frac{dQ(N_d)}{dV} \tag{S1}$$

Where dQ/dV is extracted as the slope of 2D electron density in the NW versus the gate voltage curve, from Nextnano[3] simulation result at an assumed doping level N_d, and C is the gate-NW capacitance. Assuming that C does not vary while changing the gate voltage, we have

$$C(N_d)V_{th} = Q_{total} = N_d\,(\frac{3\sqrt{3}}{2}r^2) \tag{S2}$$

Where V_{th} is the threshold voltage determined experimentally when the I_{sd} is below the measure limit, Q_{total} is the total charge in the NW. Numerically solving these two equations, N_d can be determined.