Supporting Information

Interface Passivation and Trap Reduction via a Solution-Based Method for Near Zero Hysteresis Nanowire FETs

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Experimental Section

Hydrous *N, N*-Dimethylformamide (319937) and anisole (123226) were purchased from Sigma-Aldrich Chemicals and used for dispersing the nanowires as received.

Device's fabrication: Bottom-gated FETs were fabricated following the "bottom-up" approach. The n++-doped Si/SiO_2 substrates, with thermally-grown SiO_2 gate dielectric, 230 nm thick, were solvent cleaned by sonication in acetone, IPA and methanol for 10 minutes each and O_2 plasma cleaned (100W) for 5 minutes. The patterning of the source/drain bottom-electrode contacts was performed via photolithography (lift-off). Gold (Au) micro-electrodes, were prepared by first sputtering 2 nm titanium (Ti) adhesion layer followed by 50nm gold on the substrate (JLS MPS 500 Loadlocked Sputter Coating). NWs dispersions were prepared with anisole and *N, N*-dimethylformamide (DMF). The NW were aligned via dielectrophoresis (DEP), by applying an AC field (10 $V_{peak-peak}$) across the two parallel source and drain electrodes with 10 μm gap. A NW "ink" drop was deposited using a syringe and nanowires were aligned across the source/drain electrodes. After the NW deposition, Au top-contacts (80 nm thick) with same channel gap were deposited on the NWs, using a second photolithography (lift-off) stage. Then, the devices were annealed at 250 °C for 1 hour in a N_2-filled glove box, to improve the integrity of the electrode contacts over the NWs and to evaporate residual water/solvents trapped on their surfaces. During the I-V FET measurements highly doped Si substrate served as the gate electrode.

For the XPS measurements, Si/SiO_2 substrates were cut into pieces and cleaned using solvents and O_2 plasma ash method as described previously. 50 nm thick palladium (Pd) was sputtered (JLS MPS 500 Loadlocked Sputter Coating) on top of the SiO_2 to

remove the substrate background signal. Silicon nanowires samples were prepared by drop-casting NW in anisole and DMF dispersions onto the substrates. 'Dry' NW samples were prepared by transferring NW powder with a spatula straight onto the substrates. XPS analysis was repeated three times on different samples of Si nanowires to confirm the reproducibility of results.

Nanowire hysteresis measurements: Electrical measurements were performed with a Keithley 4200 Semiconductor Characterisation System (SCS). The FETs transfer characteristics were measured in the linear regime with the gate voltage (V_G) swept from +10 V to -40 V (forward scan) and immediately back to +10 V (reverse scan) in 500 mV steps. This type of V_G scan corresponds to a p-type FET being driven from the 'off' state to 'on' state and back. The value of hysteresis was extracted from the voltage difference between the reverse voltage sweep threshold voltage $V_{th\_reverse}$ and the forward voltage sweep threshold voltage $V_{th\_forward}$ as shown in Figure S1. Transistor measurements were performed in a dry N_2-filled glove box and in ambient air environment at reactive humidity level of about 46%, as described in the main manuscript.

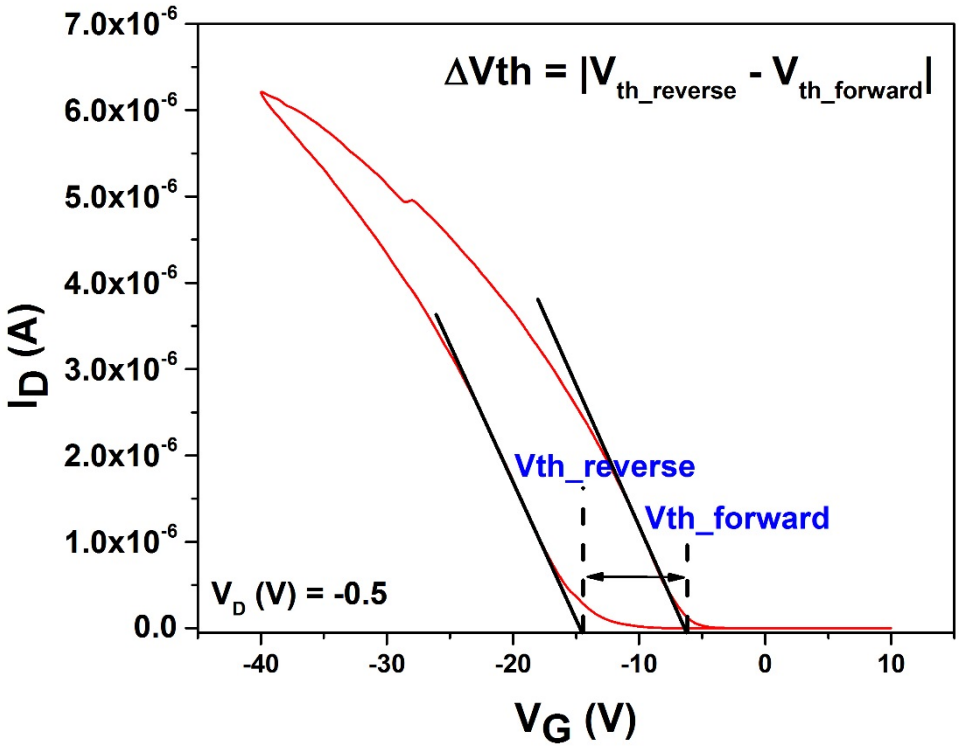


Figure S1. The linear regime transfer characteristic of a Si NW bottom-gated FET device. The difference between the reverse and forward voltage sweep threshold voltages quantifies the magnitude of hysteresis $\Delta Vth = |V_{th\_reverse} - V_{th\_forward}|$.

Nanowire characterisation: XPS analysis was performed using ThermoFisher Scientific (East Grinstead, UK) Theta Probe spectrometer. XPS spectra were acquired using a monochromated Al Kα X-ray source (hν = 1486.6 eV). An X-ray spot of ~400 μm radius was employed. Survey spectra were acquired using pass energy of 300 eV. High resolution, core level spectra were acquired using a pass energy of 50 eV except for the high resolution core level spectra of Na1s where a pass energy of 100 eV was employed. All spectra were charge referenced against the C1s peak at 285 eV to correct for charging effects during acquisition. The manufacturer's software (Avantage) was used to calculate the atomic percentages for the surface chemical composition. This software incorporates the appropriate sensitivity factors and

corrects for the electron energy analyser transmission function. Peak fitting Si2p chemical shifts from the core Si peak were employed, where ($Si^{1/2}$, Δ0.6) (Si^{1+}, Δ0.85) (Si^{2+}, Δ1.7) (Si^{3+}, Δ2.7) (Si^{4+}, Δ3.8), or in terms of binding energy were 99.6 eV, 99.9 eV, 100.7 eV 101.4 eV 102.5 eV and 103.9 eV. All ±0.2 eV for the resolution of the data and the fit. All of the peaks were fitted using Gaussian-Lorentzian (30:70) line-shape, and the background was subtracted using the Shirley method. XPS Peak 4.1 was the software used for the fitting.

The TEM microscopy of the nanowires was performed using a HRTEM microscope (HITACHI HD-2300A STEM). The samples were prepared by drop casting the Si NWs from anisole and DMF dispersions on a holey-carbon grids (Agar Scientific).

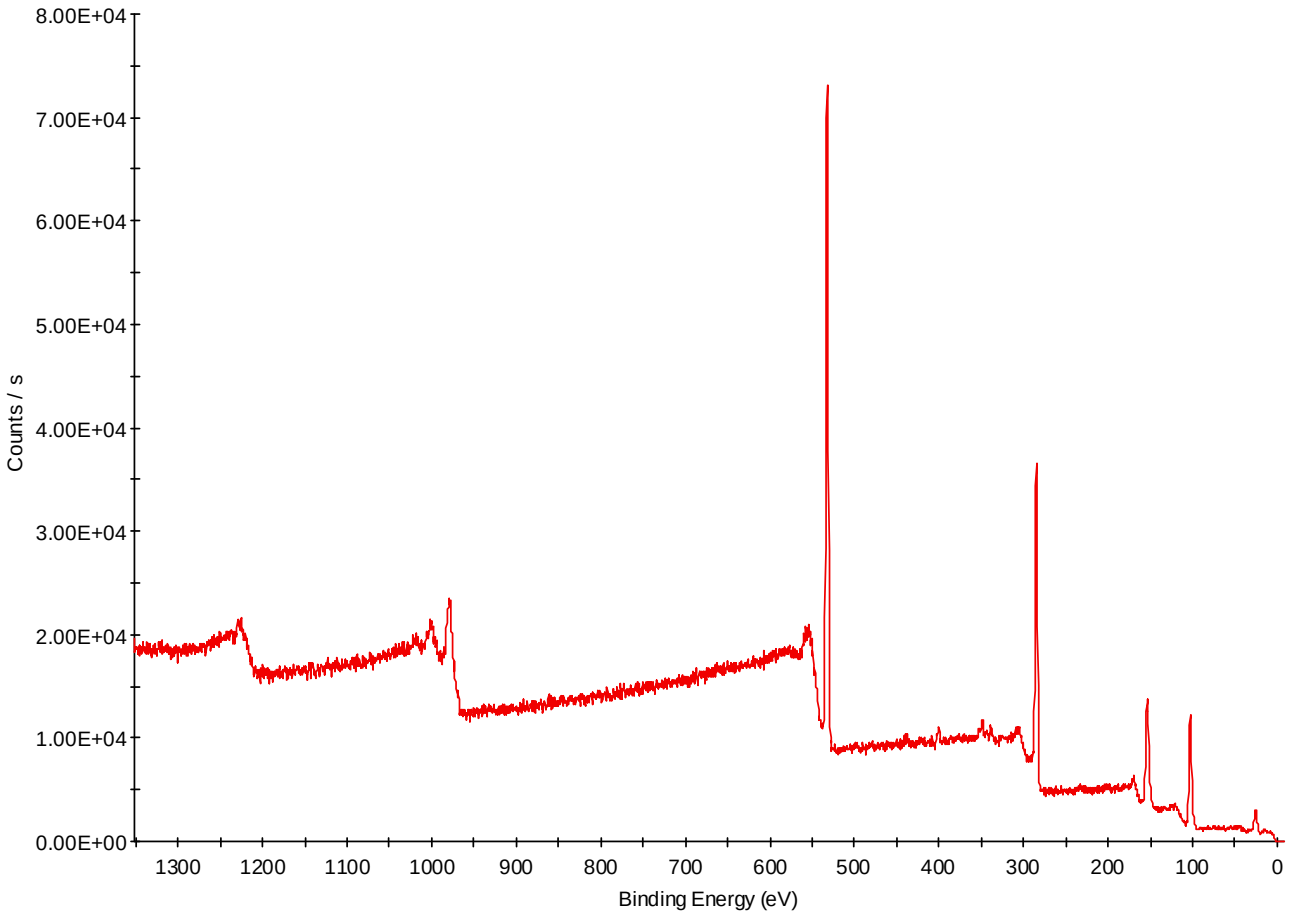
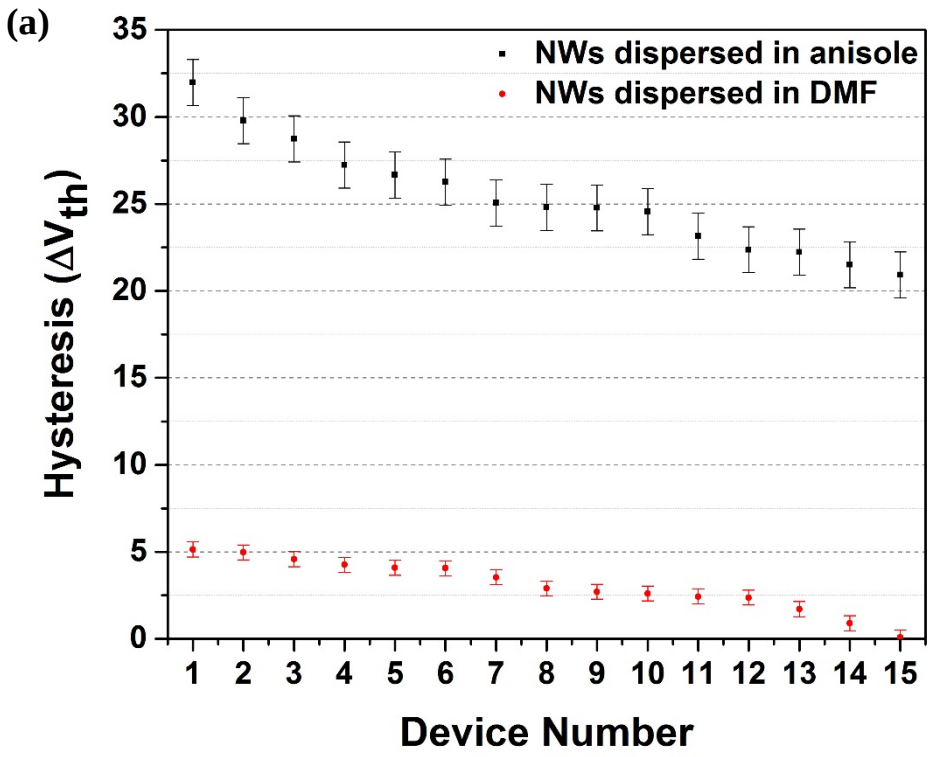
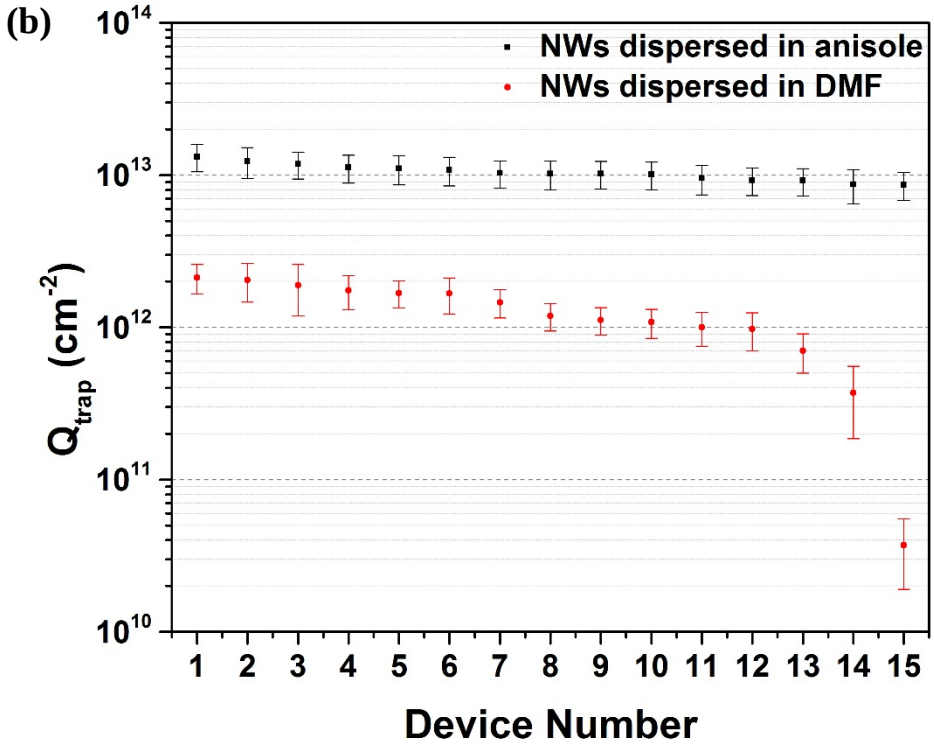


Figure S2. XPS Survey spectrum of SFLS grown Si NWs on a palladium (Pd) coated Si/SiO_2 substrate, showing all elements present (C1s, Ca2p, N1s, O1s, Pd3d, Si2p) at the surface of the Si NWs.

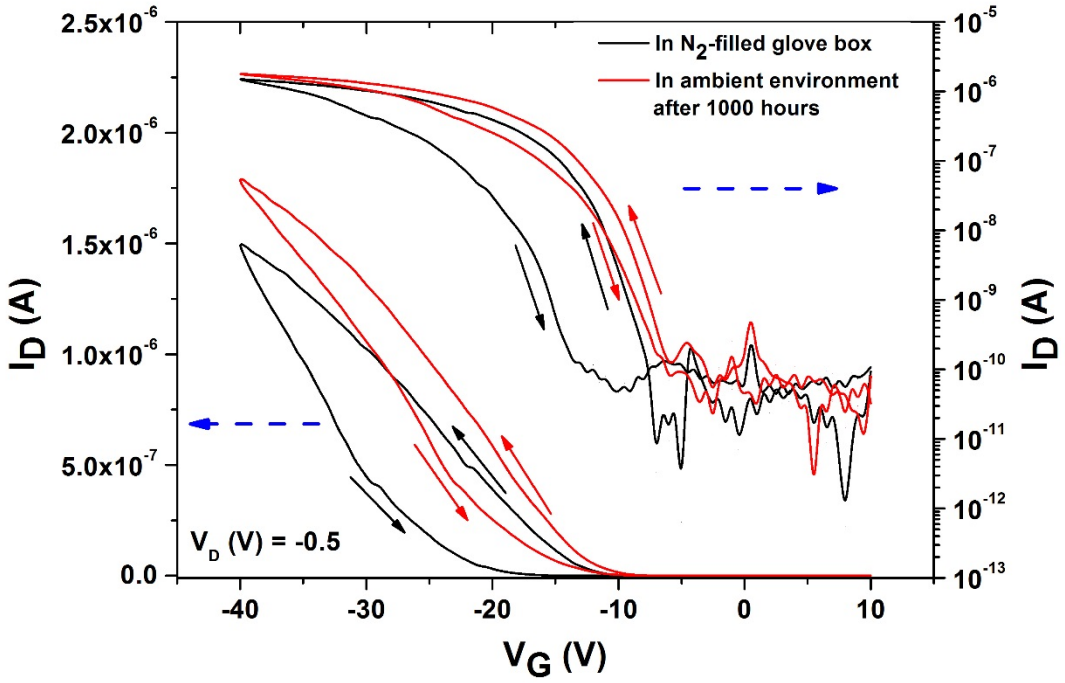
Table S1. XPS concentration contents of the SFLS grown Si NWs.

Name	Start BE	Peak BE	Height CPS	Area (N)	At. %
C1s	289.8	285.0	281.6	214.6	43.7
Ca2p	355	348.7	346.2	3.2	0.6
N1s	405.4	404.1	397.2	7.9	1.6
O1s	537.9	532.9	529.1	192	39
Pd3d	346.4	339.4	336.8	0.7	0.1
Si2p	107.5	103.3	96.6	71.9	15

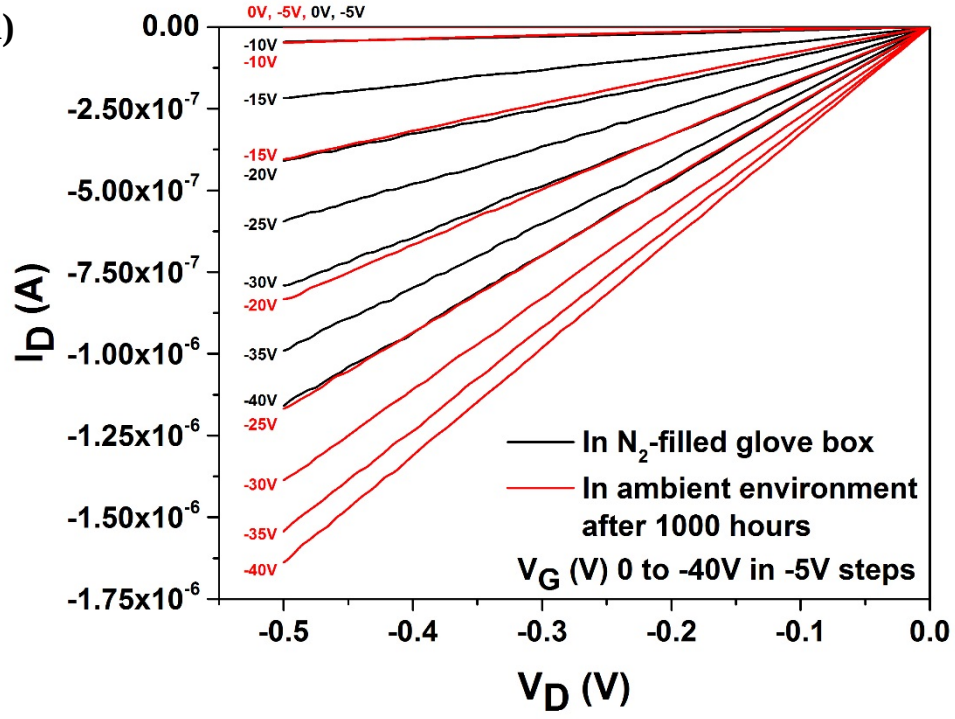

(a)
NWs dispersed in anisole
NWs dispersed in DMF
Hysteresis (ΔV_{th})
0
5
10
15
20
25
30
35
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Device Number


(b)
NWs dispersed in anisole
NWs dispersed in DMF
Q_{trap} (cm^{-2})
10^{10}
10^{11}
10^{12}
10^{13}
10^{14}
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Device Number

(c)


In N2-filled glove box
In ambient environment after 1000 hours
VD (V) = -0.5
ID (A)
VG (V)

(d)


0V, -5V, 0V, -5V
-10V
-15V
-20V
-25V
-30V
-35V
-40V
In N2-filled glove box
In ambient environment after 1000 hours
VG (V) 0 to -40V in -5V steps
ID (A)
VD (V)

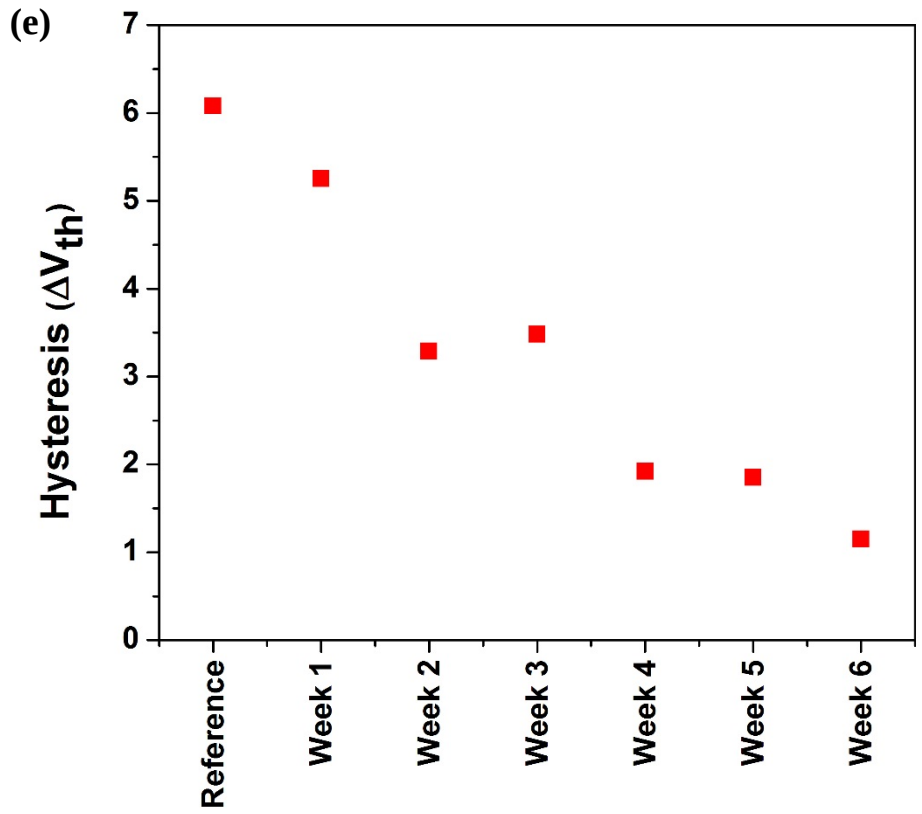


Figure S3. (a-b) Statistical analysis of the degree of hysteresis and trap density of bottom-gated FET devices with Si NWs dispersed in DMF and anisole. 15 different devices data for each solvent is presented. The DMF-treated NWs exhibited significant hysteresis reduction compared to anisole-treated nanowire devices. (c-d) Transfer and output characteristic of the DMF-treated FET device measured in N_2-filled glove box and in ambient air environmental conditions after 1000 hours of exposure. (e) Change of the hysteresis for DMF-treated FET as measured in air. Refrence measurement is conducted in a dry N_2-filled glove box.

Table S2. Hysteresis (ΔVth) and trap density (Q_{trap}), for Si NWs dispersed in anisole and DMF.

Device Number (anisole)	**Hysteresis in Anisole (ΔVth)**	**Q_{trap} in Anisole (cm^{-2})**	**Device Number (DMF)**	**Hysteresis in DMF (ΔVth)**	**Q_{trap} in DMF (cm^{-2})**
1	32	1.3E+13	**1**	5	2.1E+12
2	30	1.2E+13	**2**	4	2.1E+12
3	29	1.2E+13	**3**	5	1.9E+12
4	27	1.1E+13	**4**	4	1.8E+12
5	27	1.1E+13	**5**	4	1.7E+12
6	26	1.1E+13	**6**	4	1.7E+12
7	25	1.0E+13	**7**	4	1.5E+12
8	25	1.0E+13	**8**	3	1.2E+12
9	25	1.0E+13	**9**	3	1.1E+12
10	25	1.0E+13	**10**	3	1.1E+12
11	23	9.5E+12	**11**	2	1.0E+12
12	22	9.2E+12	**12**	2	9.8E+11
13	22	9.2E+12	**13**	2	7.0E+11
14	22	8.7E+12	**14**	1	3.7E+11
15	21	8.6E+12	**15**	0.1	3.7E+10

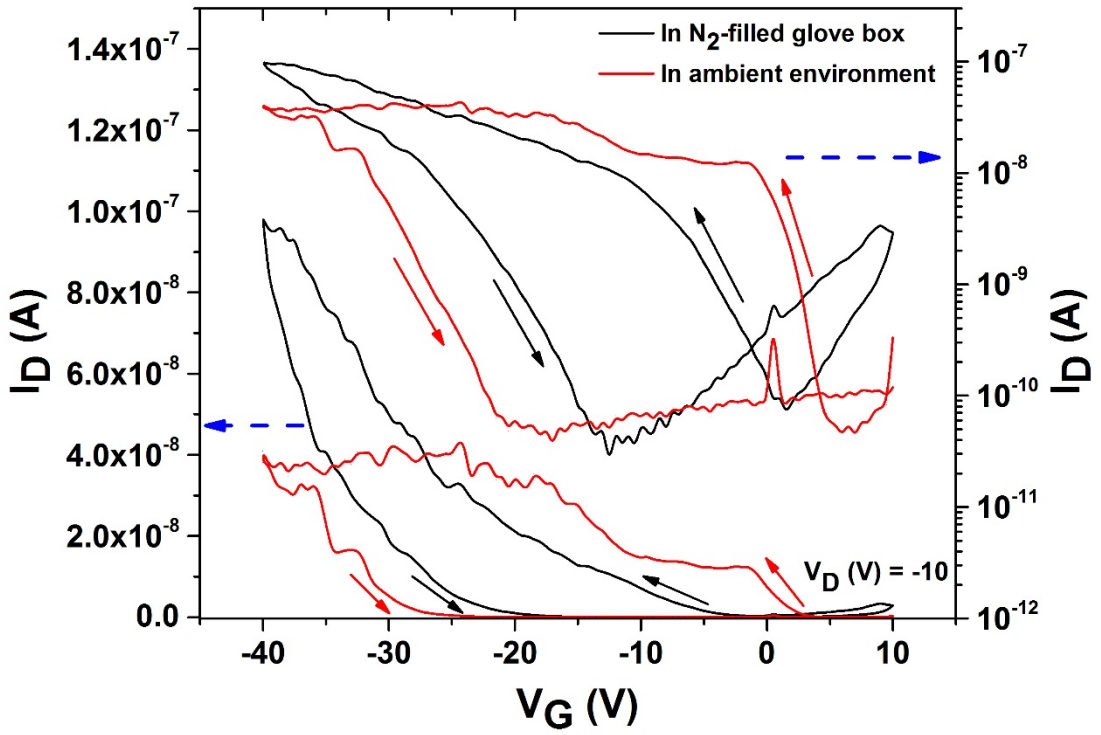
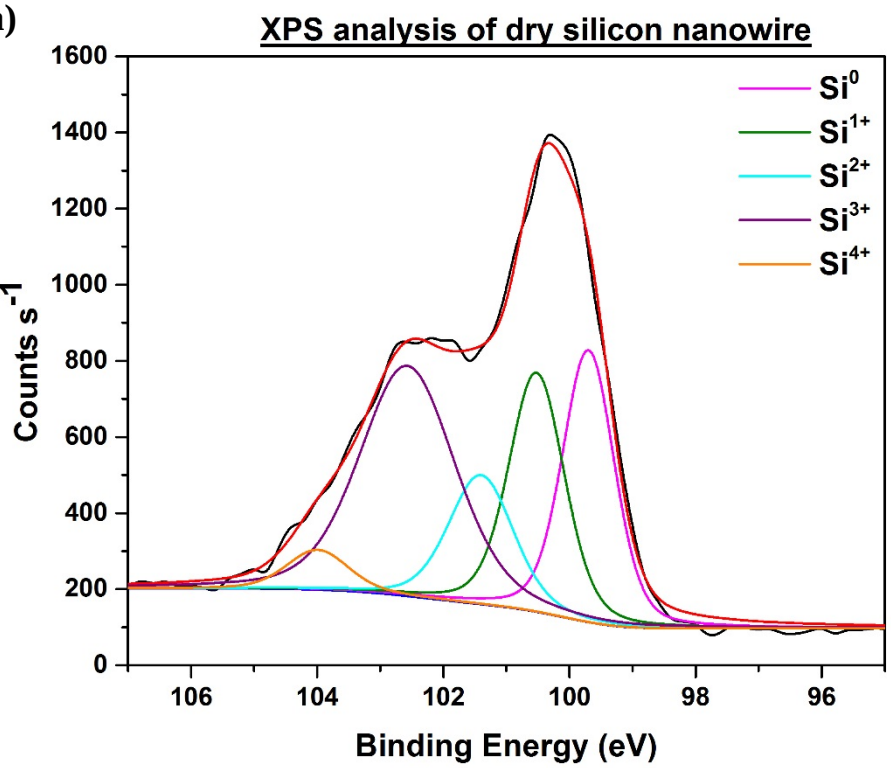


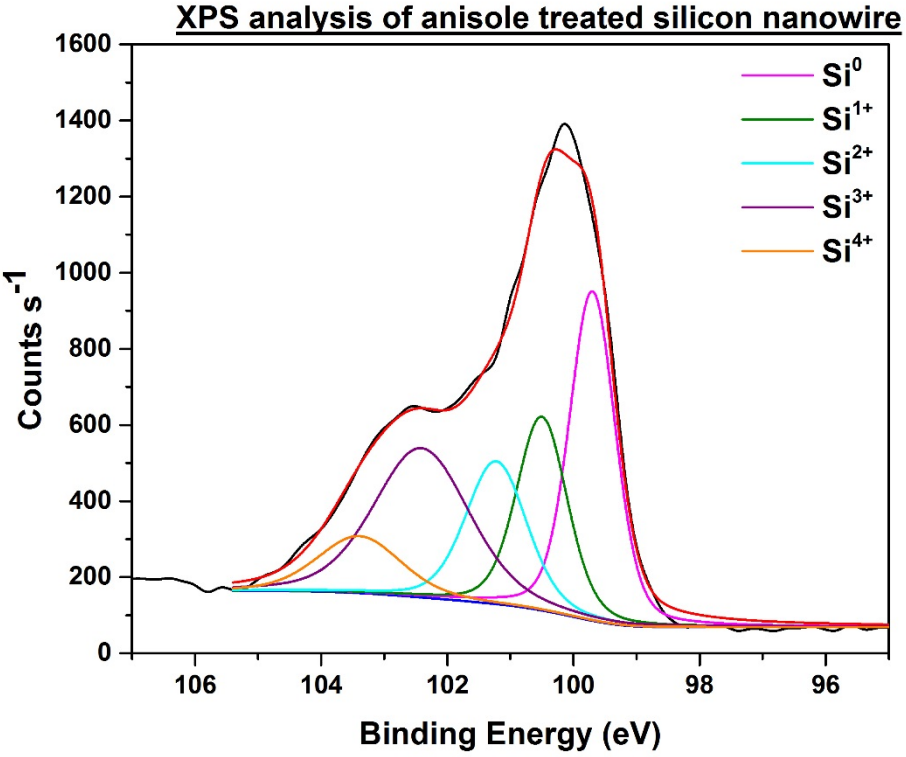
Figure S4. Transfer characteristic of the FET devices with NWs dispersed in anisole and measured in N_2-filled glove box and ambient air environmental conditions after 24 hours of exposure.

The hysteresis increased from 18 V to 33 V. The measurement is conducted in air 24 hours after FET removal from the glove box. The device was unmeasurable after one week of ambient air exposure, showing no detectable FET characteristics.

(a)


XPS analysis of dry silicon nanowire
Si0
Si1+
Si2+
Si3+
Si4+
Counts s-1
Binding Energy (eV)
1600
1400
1200
1000
800
600
400
200
0
106
104
102
100
98
96

(b)


XPS analysis of anisole treated silicon nanowire
Si0
Si1+
Si2+
Si3+
Si4+
Counts s-1
Binding Energy (eV)
1600
1400
1200
1000
800
600
400
200
0
106
104
102
100
98
96

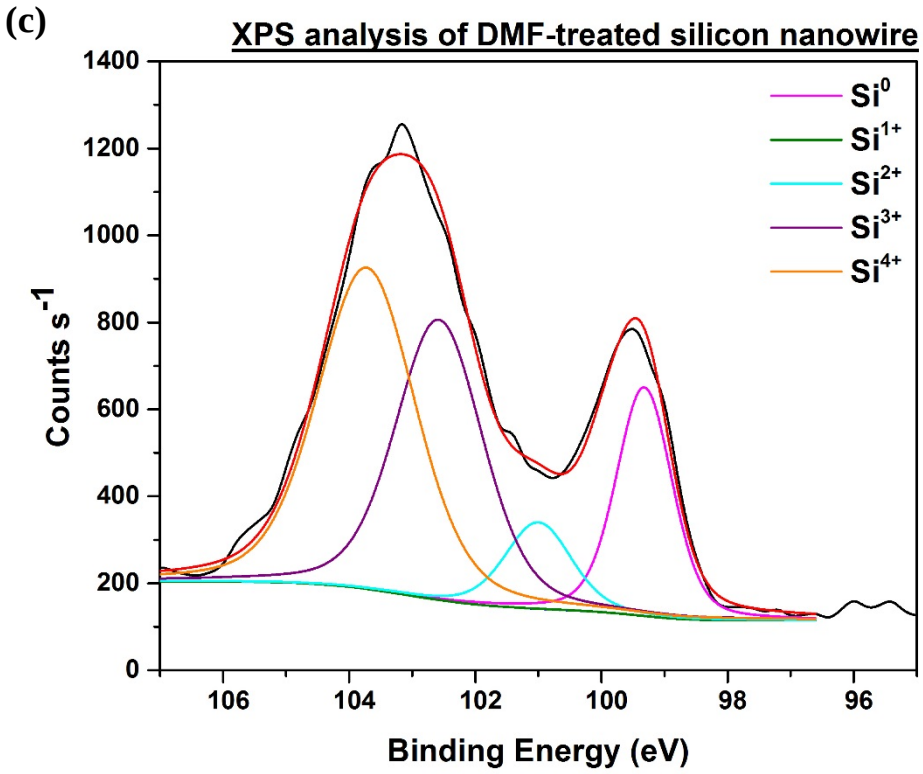


Figure S5. XPS spectra of the Si2p region for (a) dry Si NW, (b) anisole-treated Si NW and (c) DMF-treated Si NW. The line shape of each sample (black) was fitted by the peak deconvolution with Si^{0}, Si^{1+}, Si^{2+}, Si^{3+} Si^{4+} components, fitted using the Gaussian/Lorentzian function. The black curves show the experimental data and the red curves show the data fits.

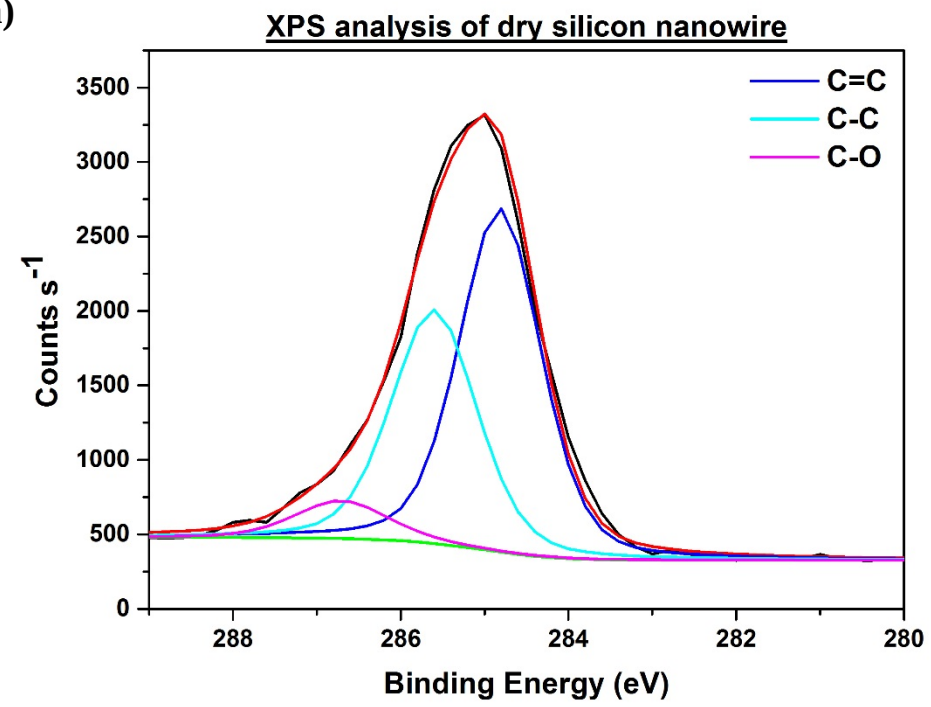
Table S3. XPS peak areas for dry Si NWs and Si NWs dispersed in anisole and DMF.

Silicon NW Treatment	**Overall XPS Peak Areas**	**Si^{0}**	**Si^{1+}**	**Si^{2+}**	**Si^{3+}**	**Si^{4+}**
Dry	19500	6200	3900	2400	6300	700
Anisole-treated	17300	6600	2900	2500	4000	1300
DMF-treated	20400	4800	0	1500	6200	7900

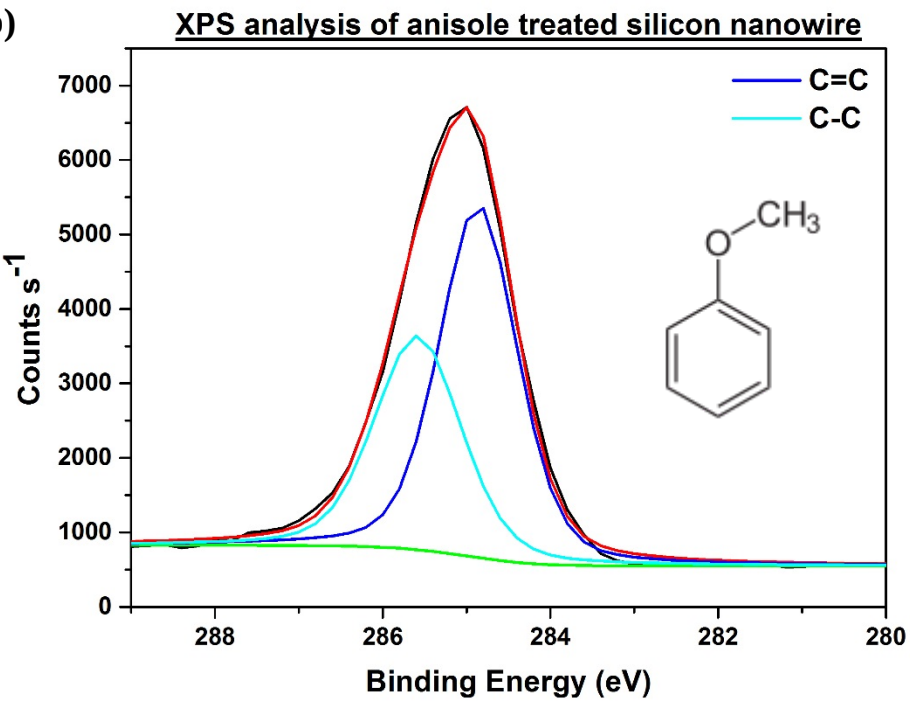
Table S4. XPS percentage atomic concentrations of dry Si NWs and Si NWs dispersed in anisole and DMF.

Silicon NW Treatment	**Si^{0}**	**Si^{1+}**	**Si^{2+}**	**Si^{3+}**	**Si^{4+}**
Dry	32%	20%	12%	32%	4%
Anisole-treated	38%	17%	14%	23%	8%
DMF-treated	24%	0%	7%	30%	39%

(a)


XPS analysis of dry silicon nanowire
C=C
C-C
C-O
Counts s-1
3500
3000
2500
2000
1500
1000
500
0
288
286
284
282
280
Binding Energy (eV)

(b)


XPS analysis of anisole treated silicon nanowire
C=C
C-C
CH3
O
Counts s-1
7000
6000
5000
4000
3000
2000
1000
0
288
286
284
282
280
Binding Energy (eV)

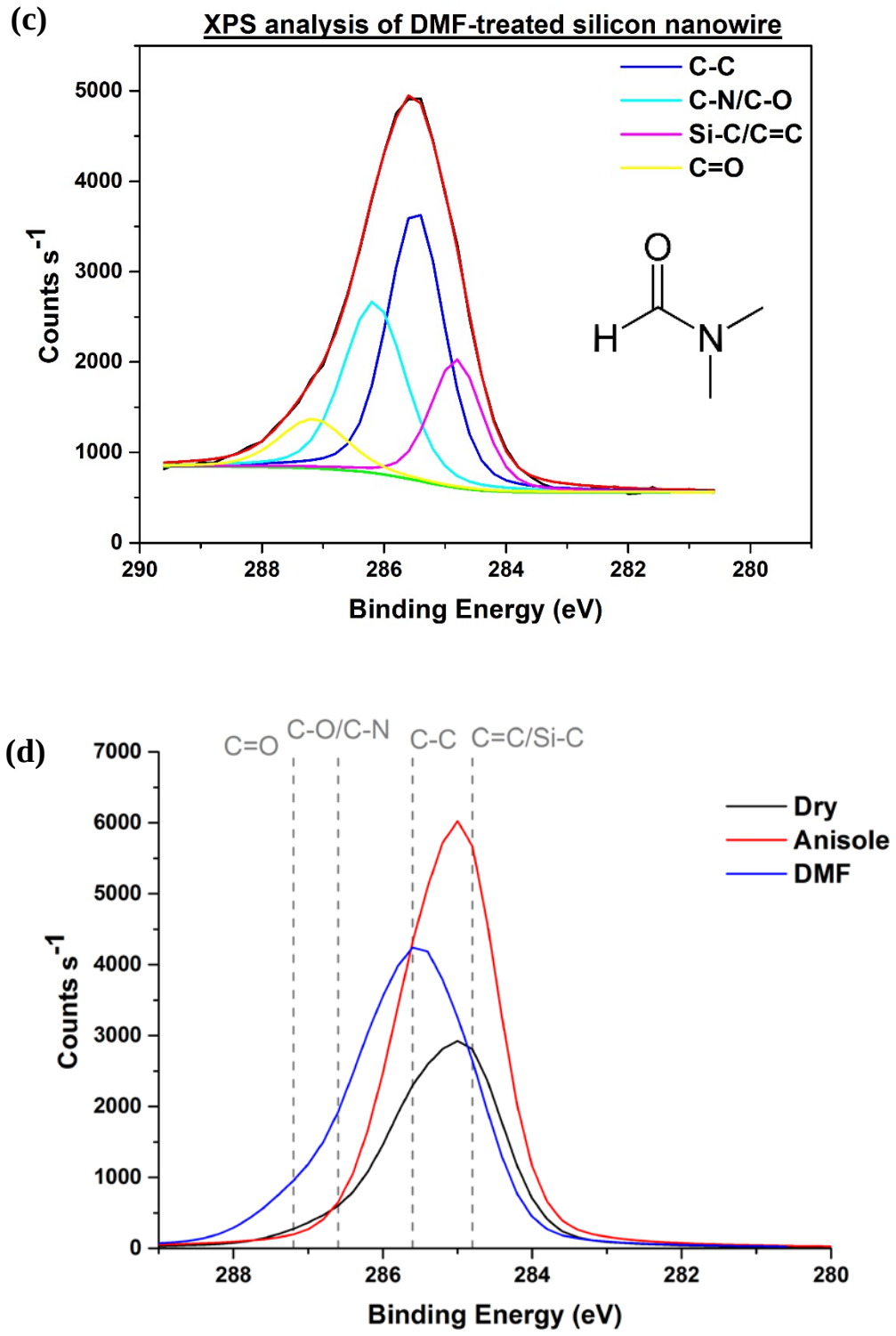


Figure S6. XPS spectra of the C region for (a) dry Si NW, (b) anisole-treated Si NW and (c) DMF-treated Si NW. The line shape of each sample was fitted by the peak deconvolution with C-O, C=O, C-C, C-N/C-O and Si-C/C=C components, fitted using the Gaussian/Lorentzian. (d) XPS survey spectrum of the C region of Si NWs.

According to the C1s XPS spectra, the residue of anisole (b) and DMF (c) can be observed. The increase of C-C and C=C peaks in (b) is associated with the presence of the anisole benzene ring, and the C=O peak in (c) is associated with DMF**.** The black curve shows the experimental data and the red curve shows the data fits.

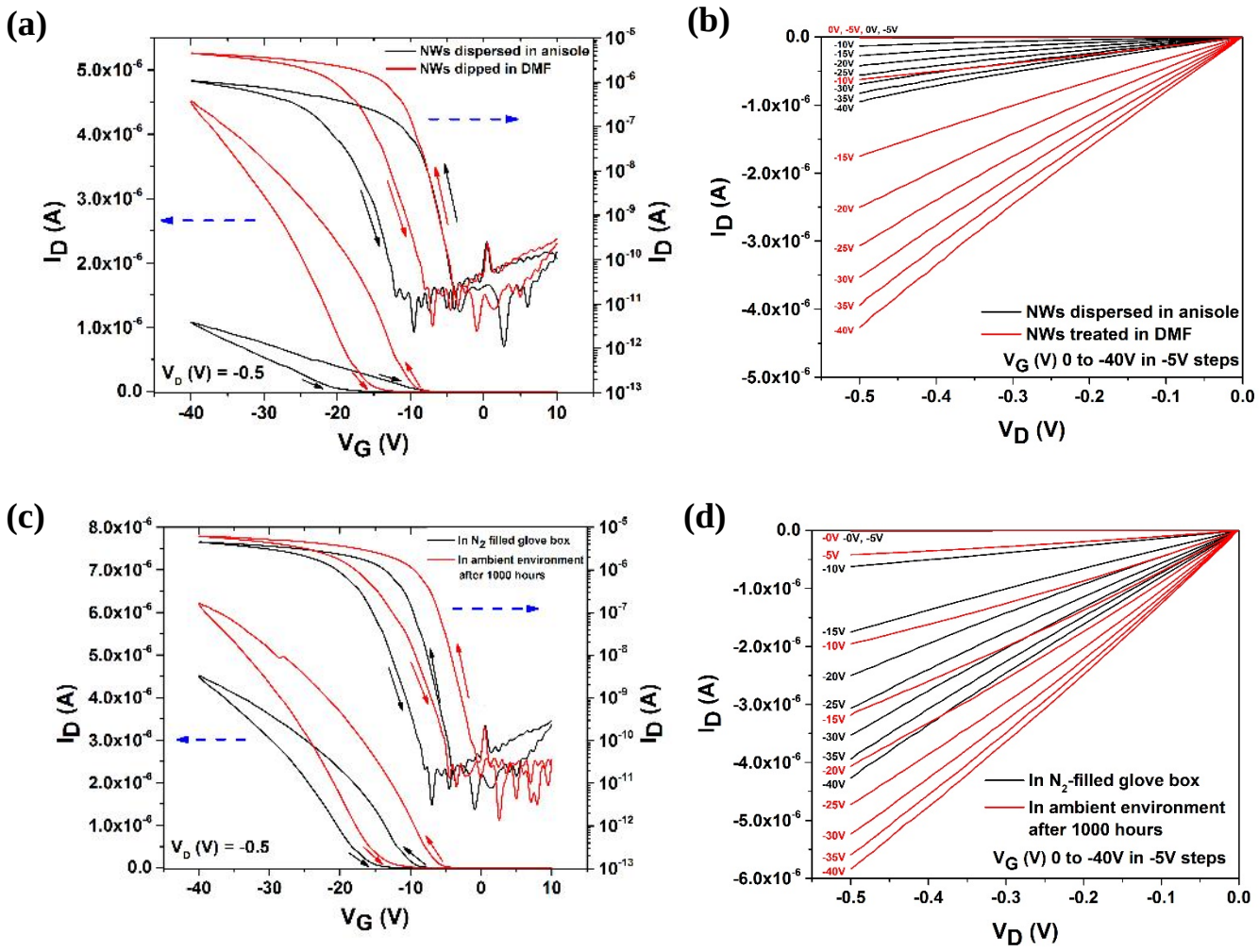


Figure S7. (a) Transfer and (b) output characteristics of bottom-gated FETs with SFLS grown Si NWs. Devices were prepared using anisole, and then treated with DMF. Black curves correspond to FETs fabricated using *only* anisole solvent. Red curves correspond to the *same* devices that were later functionalized in DMF for 10 seconds and re-measured. As transistor devices are identical, and the measurements correspond to different solvent treatments, the effect of the number of nanowires in the transistor channel on the FET performance can be completely ruled out.

The hysteresis decreased from 11 V to 6 V following DMF treatment. The increase of the on/off ratio ($I_{ON/OFF}$) and the output current (I_{OUT}) (from ~0.95 μA to ~4.3 μA) after DMF treatment underlines the effect of the DMF solvent on the nanowire shell interface providing lower trap density. Also an increase in the device mobility (μ) was observed from 1 $cm^2\ V^{-1}\ s^{-1}$ to 8 $cm^2\ V^{-1}s^{-1}$ after DMF treatment. (The device was measured in a N_2-filled glove box).

(c) Transfer and (d) output characteristic of the same device after 1000 hours of exposure to ambient air environment. The hysteresis was only increased by 0.6 V with a further increase in the output current (I_{OUT}) to ~5.8 μA and the devices mobility to 9 $cm^2\ V^{-1}\ s^{-1}$.

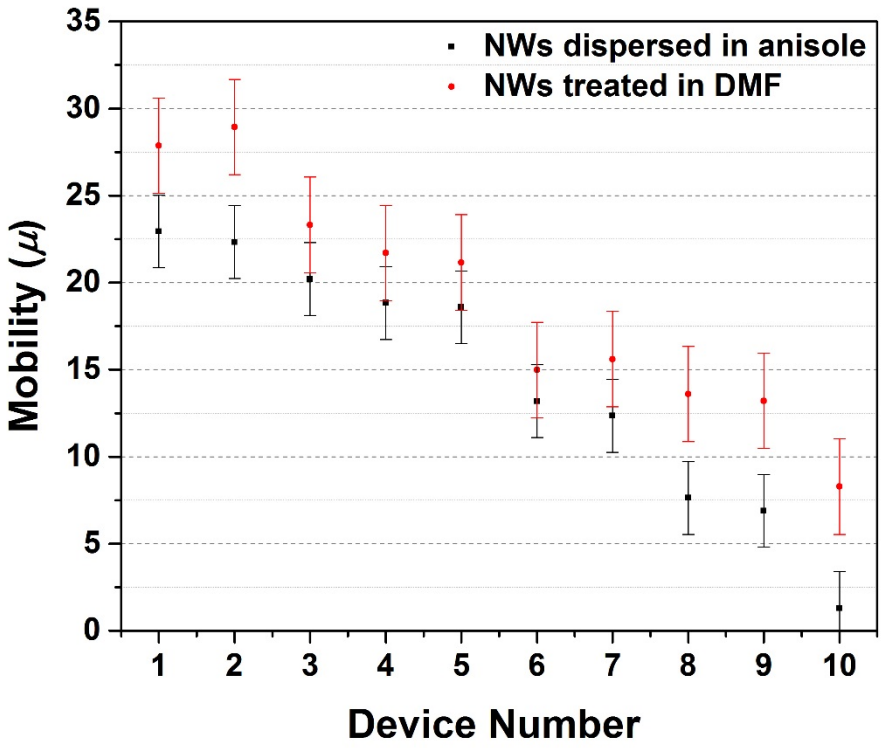


Figure S8. Statistical analysis of the increase of the device mobility (μ) of bottom-gated FET devices with Si NWs dispersed in anisole and then treated in DMF. The increase in the device's mobility (μ) is attributed to the NWs shell passivation via DMF mild oxidation. The device No 10 data is shown in Figure S7.

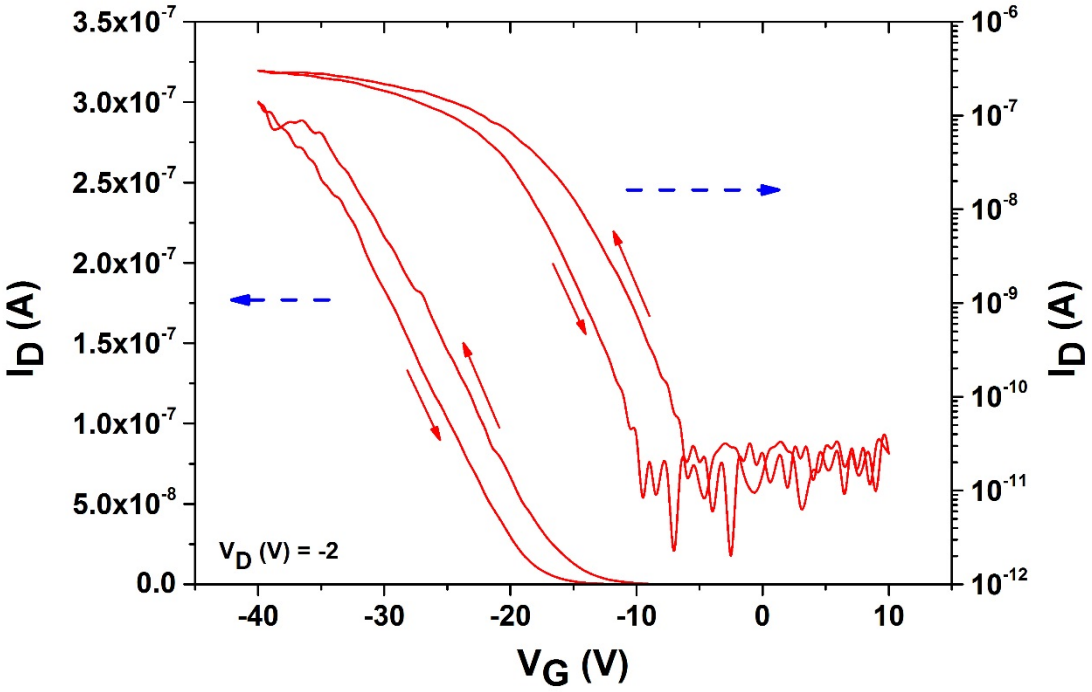


Figure S9. Transfer characteristic of the DMF-treated FET device fabricated on plastic substrate (Kapton) with paryelene N as a gate dielectric (measured in N_2-filled glove box). The device demnstrated hysteresis of ~2.5 V.