

Supporting Information

Ferroelectric Single-Crystal Gated Graphene/Hexagonal-BN/Ferroelectric Field-Effect Transistor

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P-E curve of PMN-PT in the different V_G sweep ranges from ± 70 V to ± 20 V

The polarization *versus* electric-field (P-E) curves for the ferroelectric single-crystal PMN-PT ((1-x)[Pb(Mg_{1/3}Nb_{2/3})O₃]-x[PbTiO₃]) are presented in Figure S1 in the different V_G sweep ranges from ± 70 V to ± 20 V.

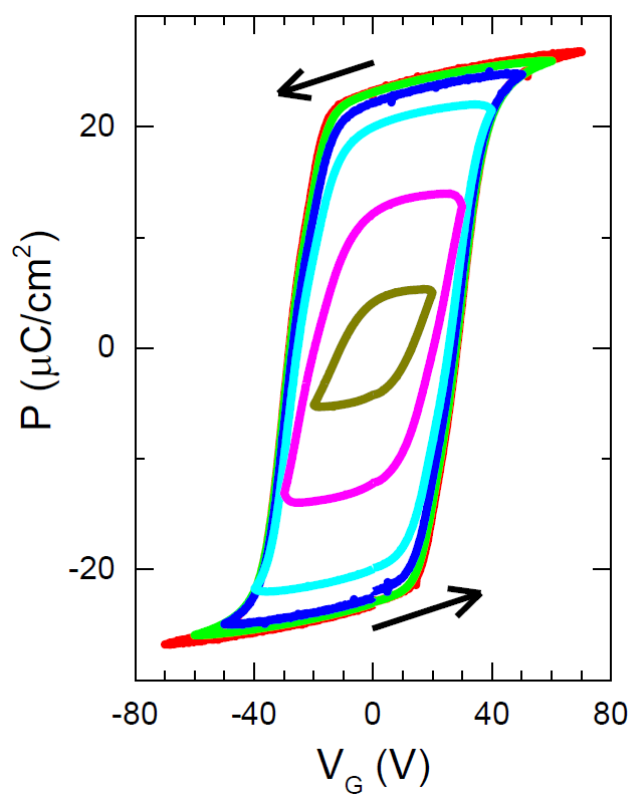


Figure S1. The polarization *versus* electric field (P-E) curves at different V_G sweep ranges from ± 70 V to ± 20 V.

Discussion on the channel conductance variation during the transition from antihysteresis to normal ferroelectric hysteresis

In Figure 5, we developed a general model for the explanation of antihysteresis and the reduction of carrier density in the Graphene/Dielectric (hBN)/Ferroelectric (PMNPT) configuration. Unlike the case of direct contact between graphene/ferroelectric, the insertion of another dielectric layer (*i.e.* hBN) between graphene and ferroelectric resulted in the antihysteresis and the reduction of carrier density simultaneously as discussed in Figure 5d. In the experimental data, the transition from antihysteresis to normal hysteresis occurs as the V_G sweep range decreases.

To check the improvement in carrier concentration during transition, we collected the data in the different V_G sweep range and plot them as a function of $V_G - V_{CNP2}$ in Figure S2. When the V_G sweep range is within the normal ferroelectric hysteresis ($\pm 20V$, $\pm 30V$, $\pm 40V$), the current level is not changing much. But, as the V_G sweep range increases ($\pm 50V$, $\pm 60V$, $\pm 70V$), the reduction of current occurs. These results directly confirm that the carrier concentration in the normal hysteresis region is higher than that in the antihysteresis region at the same V_G .

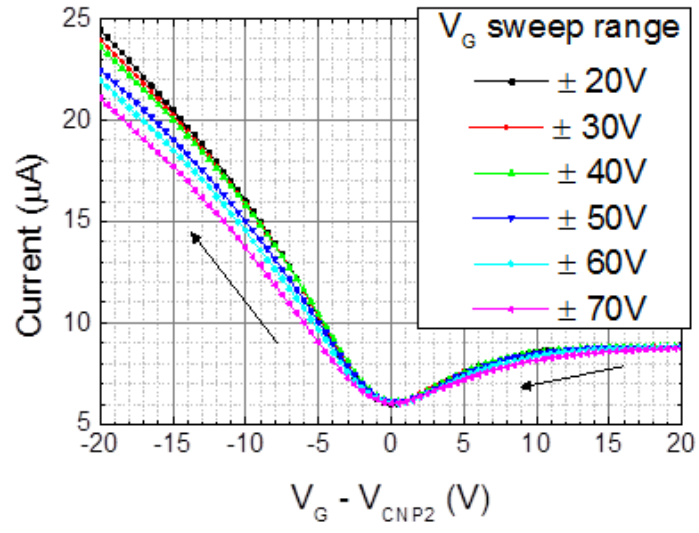


Figure S2. Comparison of channel conductance variation depending on the V_G sweep ranges from ± 70 V to ± 20 V.

Surface morphology of polished PMN-PT substrate

The surface morphologies of PMN-PT (001) substrate were examined using the atomic force microscope (AFM) in a tapping mode. As in Figure S3a, a clear contrast in the image indicates that the surface of PMN-PT has many domains with different heights in the level of a few to several nanometers even though it is polished. However, the facts that the height changes quite sharply at the domain boundary and does not change much within the domain explain that the height difference is directly related to the ferroelectric domain structure at the surface of PMN-PT. For another surface area presented in Figure S3b, a quite regular pattern was observed in a large scale with herringbone or tire-track shape. In the literature,³⁰⁻³³ such regularity had been already discussed and known to represent the rhombohedral domain pattern having the $\langle 111 \rangle$ oriented ferroelectric polarization of PMN-PT pseudocubic cell in the (001)-oriented substrate. We examined many polished PMN-PT substrates in different polishing conditions, and found out that this feature always exists and gives the height difference among domains. The correlation between the polishing process and the resulting domain structure is beyond the scope of this work.

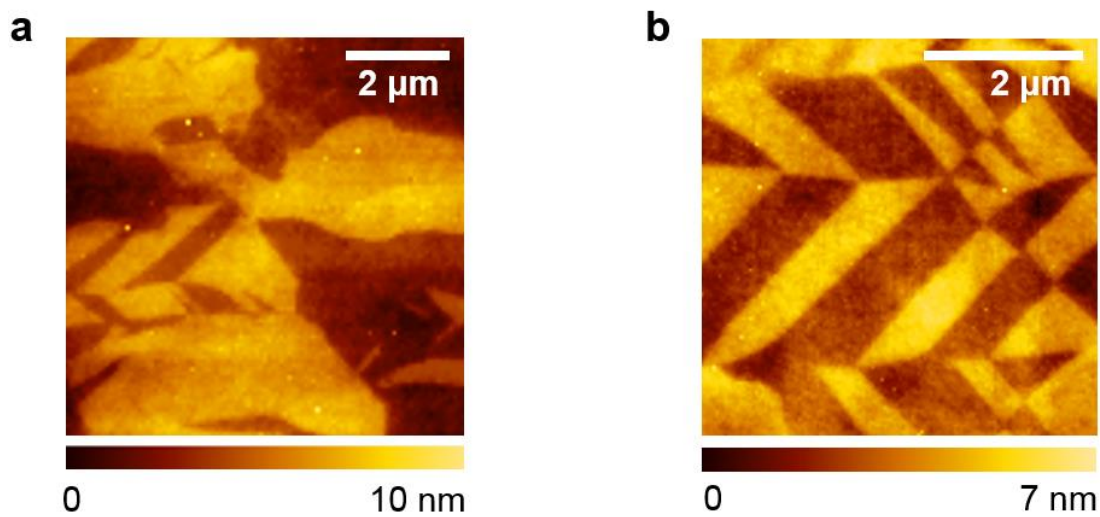


Figure S3. Atomic force microscope (AFM) image of surface morphology of bare PMN-PT substrate. (a) Typical image of irregular, large-area domain shape found overall in the sample. (b) Typical image observed in some areas showing strong regularity of a rhombohedral domain pattern. The color scale bar shows the height of the surface area.

Discussion on charge traps at the interface between PMN-PT and hBN

For the study of electrical transport through monolayer-graphene under the influence of ferroelectric polarization field, the GBFeFET (Graphene/hexagonal-BN/Ferroelectric Field-Effect Transistor) device structure was constructed, where an hBN flake was inserted between ferroelectric PMN-PT and monolayer graphene to minimize the effect of surface roughness of PMN-PT substrate. In the device fabrication processes, the dielectric hBN is mechanically transferred to the surface of PMN-PT substrate. Consequently, the interface between hBN and PMN-PT can have many possibilities of charge-trapping for the compensation of ferroelectric polarization at the surface of PMN-PT substrate, not only due to the surface adsorbates during the sample preparation, but also due to the imperfection of interface between hBN and PMN-PT originated from the surface roughness of the substrate. In addition, a local fluctuation can occur in the density of interfacial charge traps within the sample. However, if we consider the small size of the graphene channel area (which is 10 μm wide and 2.5 μm long (defined by the gap between electrodes)) and the thick hBN layer (which is 50 nm), the effect of charge density fluctuation can be mitigated. Therefore, in our analysis presented in Figure 5 and Figure 6, a homogeneous interfacial surface-charge layer between PMN-PT and hBN is considered as a first order approximation for the real situation.

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