Supporting Information

Strain-Gated Field Effect Transistor of a MoS_2-ZnO 2D-1D Hybrid-Structure

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Supplementary Figures

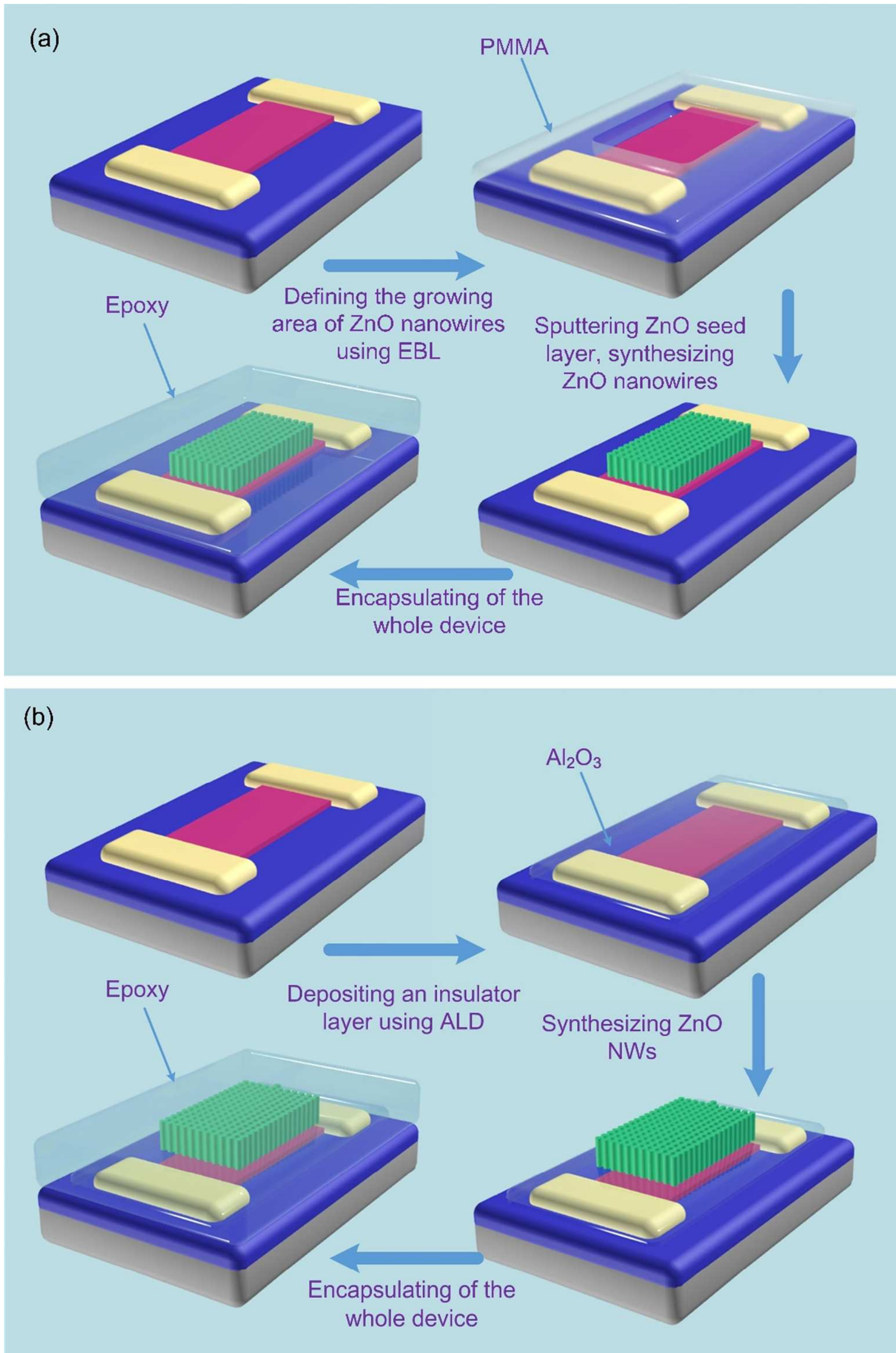

Figure S1. Schematic cartoon graphs showing the fabricating process of the Dev. 1 (a) and Dev. 2 (b).

The micro-fabrication process of the Dev. 1 is first stated below. The as-fabricated MoS_2 transistors was first coated a layer of electron beam resist (PMMA, 200 nm). A precise location and region (3 um in width, 30 um in length) of synthesized ZnO NWs was defined by electron beam lithography. Then we used magnetron sputtering to deposit a ZnO seed layer as a nucleation site for following grown ZnO NWs. The sputtering power and time were precisely controlled at 60 W and 300 s respectively, which is not enough to reduce the atomic layers of MoS_2 flakes as shown in Supplementary Fig. 2. Next, the devices were placed in a precursor solution containing $Zn(NO_3)_2 \cdot 6H_2O$ and HMTA and after four hours taken out. The MoS_2 flakes are very sensitive to the alkalinity and humidity[1], yielding the degraded output and transfer characteristics as indicated in Fig. 2 in the main text and Supplementary Fig. 4. Finally, PMMA were slightly lifted off in the acetone, preventing the synthesized ZnO NWs in the defined region from washing away. A layer of epoxy was used to encapsulate the entire transistor to keep its stability.

The distinct difference of the micro-fabrication processes of the Dev. 2 is that a layer of insulator (Al_2O_3) was pre-deposited on the device by ALD before synthesizing ZnO NWs.

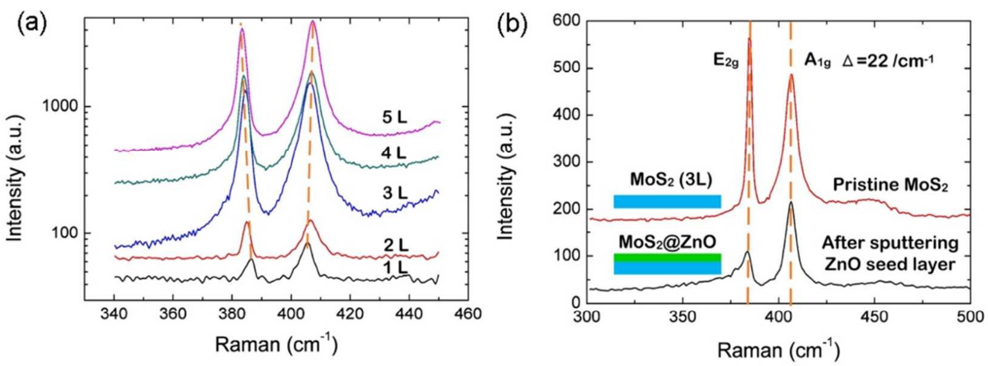

Figure S2. Raman spectrum for recognition the layer number of MoS_2. (a) Raman spectrum of MoS_2 fakes with different layer number. **(b)** Raman spectrum before (top) and after (bottom) sputtering a ZnO seed layer. The peak distance between E_{2g} and A_{1g} are all about 22 /cm for the pristine MoS_2 flake and the one decorated with ZnO seed layer, which indicates that the layer number of MoS_2 flake is possibly not affected by the sputtering in this project.

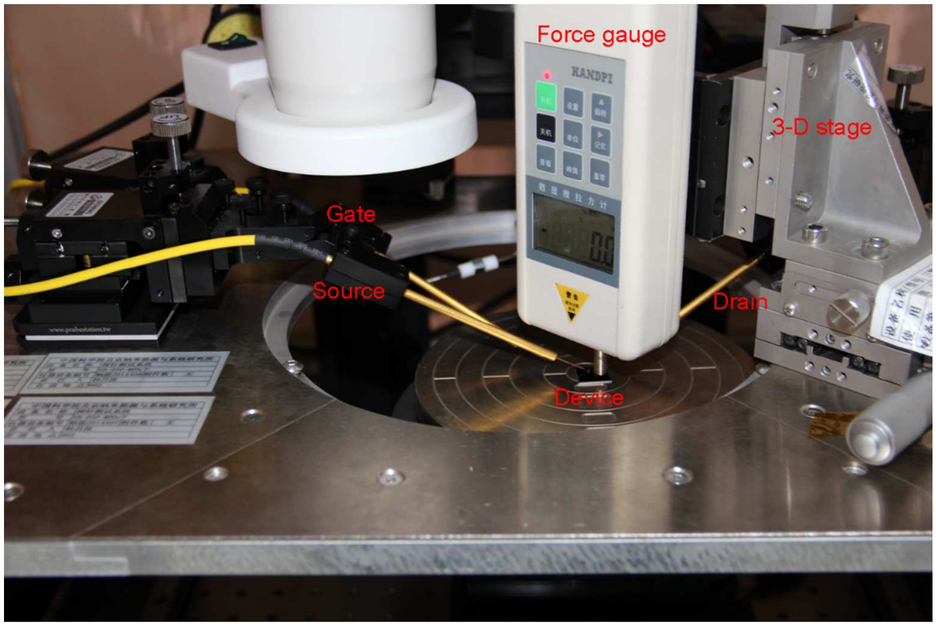

Figure S3. Optical graph of our testing platform. The drain, source and gate electrodes are connected to the Keithley 4200 semiconductor analyzer, respectively. For the measurement of repeatability as shown in Fig. 2 (Main text), the digital force gauge was mounted on a stepping motor.

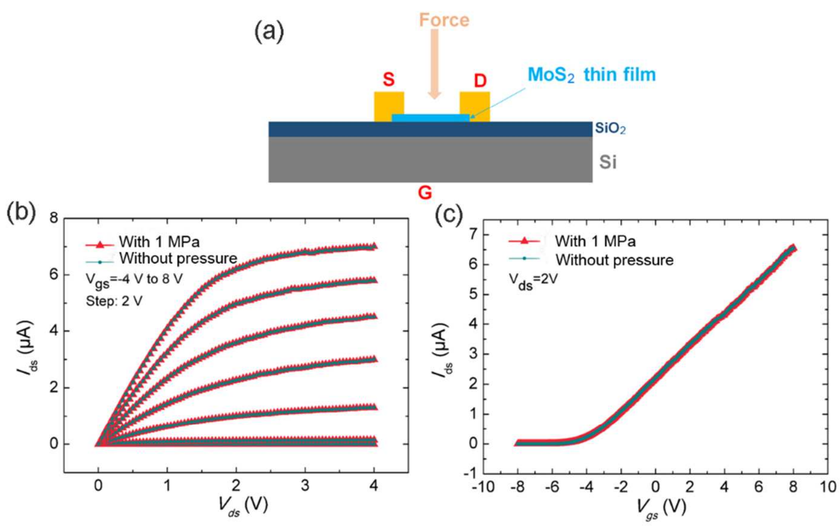

Figure S4 | Pressure's influence on the output curves (b) and transfer curve (c) of a MoS_2 transistor without any hybrid structure. Those three devices were tested and one of the typical characteristics was shown above. A robust output current saturation and high on/off ratio are obtained in the output curve and transfer curve respectively. More importantly, with an applied pressure of 1 MPa, there's no obvious change in drain current for all of the devices. Hence we conclude that the piezo-resistance effect of MoS_2 flakes can be ignored. What's more, it's observed that, compared with those MoS_2 transistors, the performance of MoS_2-ZnO hetero-structure as indicated in the main text is degraded by the solution process.

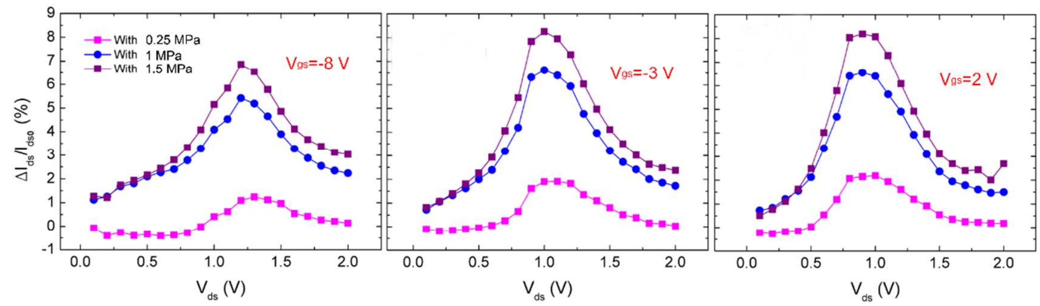

Figure S5. Drain current change under different applied pressures and different gate voltages acquired from Fig. 3f in the main text. The largest variation ranges, which could be modulated by the externally pressure, mainly center on the drain voltage of 0.8~1.3 V under different gate voltages and nearly 8% increased current variation is achieved at the pressure of 1.5 MPa and gate voltage of 2 V. We attribute this phenomenon of current change concentration to the result of competition between the increased electrons across the barrier height and the decreased piezoelectric polarization charges due to the screening effect.

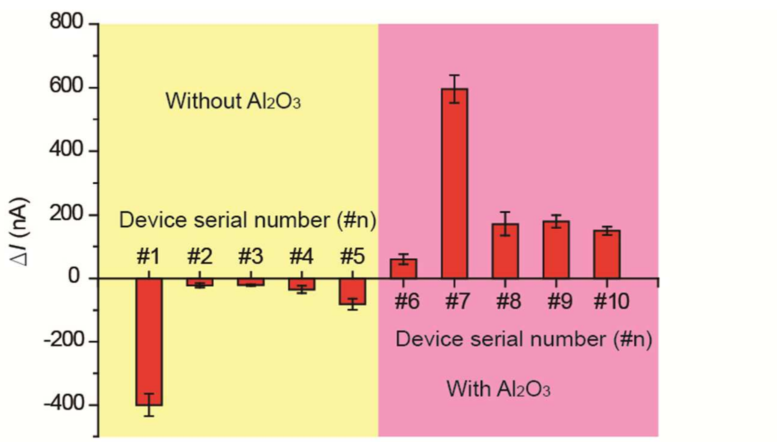

Figure S6. Histograms of change in drain current for two group devices at 2 MPa. For the first group devices (#1 ~ #5), ZnO NWs were directly synthesized on the MoS_2 nano-fakes as the structure of Dev. 1 in the main text while an insulator layer was deposited between MoS_2 and ZnO as the structure of Dev. 2 for the second group devices (#6 ~ #10). All of the first group devices show a negative current variation and the second group devices a positive current variation. The applied drain voltage is 0.5 V and the gate voltage 0 V.

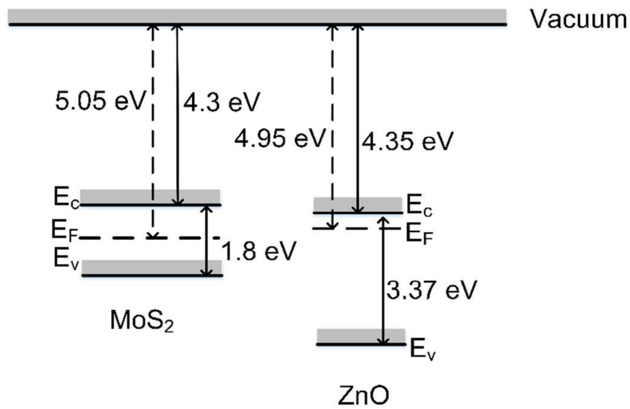

Figure S7. Electron affinity, work function and band gaps of MoS_2 and ZnO used in the energy band diagrams[2-5]. Three to five layers MoS_2 are chosen in this work, so the relevant band gap is considered to be 1.8 eV. A hetero-junction is formed at the interface of those two semiconducting materials. Due to the higher Femi-level in the ZnO side than that in the MoS_2, the electrons will deplete at the interface of ZnO and accumulate at the interface of MoS_2.

Reference

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