Monolithically Integrated Metal/Semiconductor Tunnel Junction Nanowire Light Emitting Diodes

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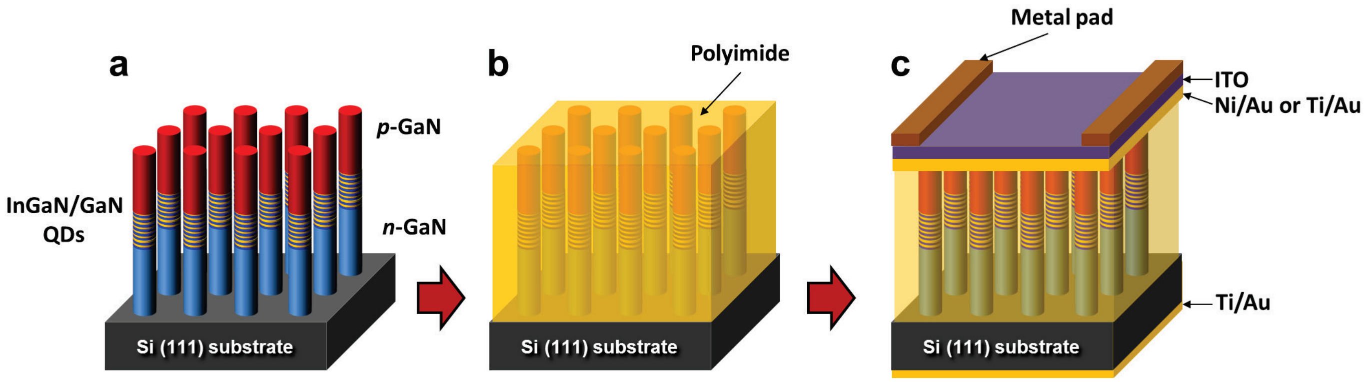
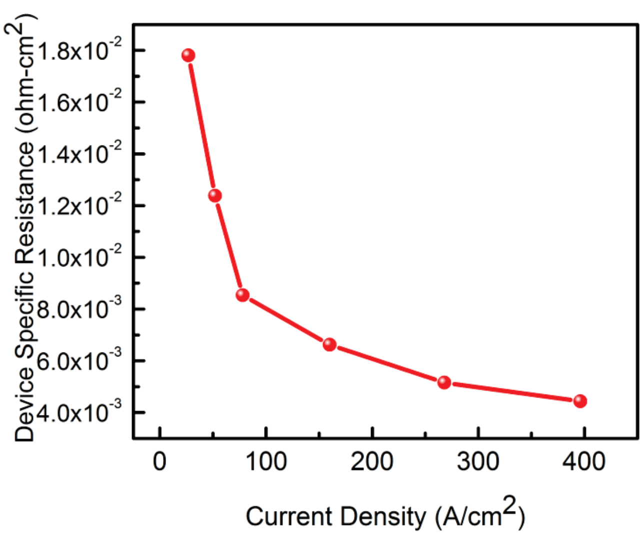


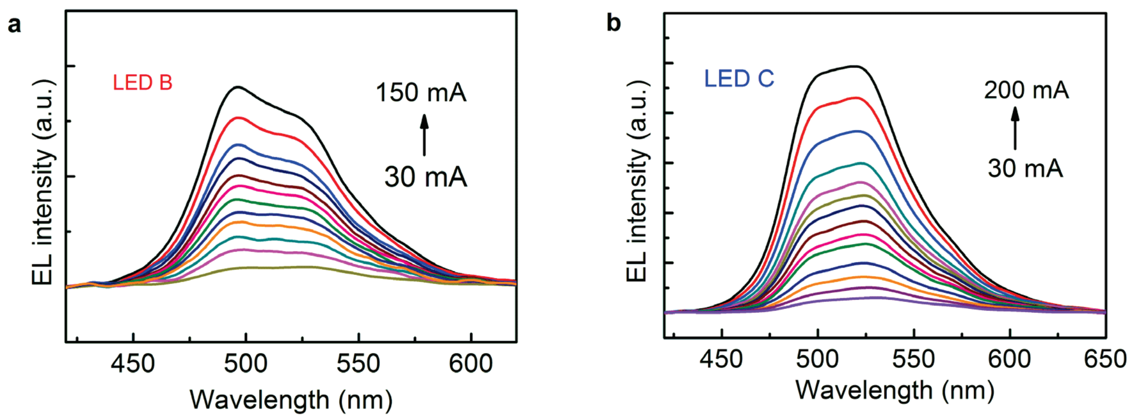
Supplementary Figure 1: Schematics of the fabrication process of nanowire LEDs **a**. as grown nanowires on Si substrate. **b**. Polyimide spin-coated to fill the gaps between the nanowires. **c.** Polyimide etching back, and contact metal and ITO deposition.



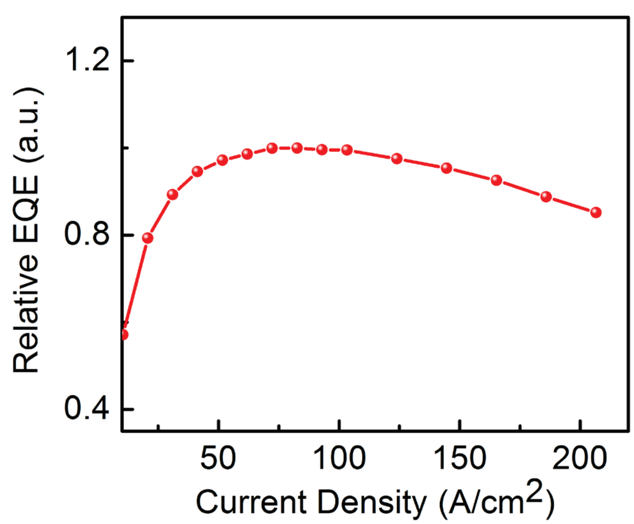
Supplementary Figure 2: Device specific resistance vs. current density plot for LED A.

Table S1. Summary of specific resistance values in previously reported tunnel junction devices.

Journal	Tunnel Junction (TJ)	TJ resistance (Ω.cm^2)	Device resistance(Ω .cm^2)	Structure	Method
APL, 105,141104, 2014	InGaN/GaN	5×10^{-4}	2×10^{-2}	***Planar***, TJ LED	PA-MBE
Nano Lett, 13, 2570-2575, 2013	GdN/GaN	1.3×10^{-3}	N/A	***Planar***, TJ p-n device	PA-MBE
Nano Lett, 13, 2570-2575, 2013	p^{++}-GaN/n^{++}-GaN	22.5×10^{-2}	N/A	***Planar*** TJ device	PA-MBE
IEEE EDL,36, 4, 2015	InGaN/GaN	6.05×10^{-3}	2.38×10^{-2}	***Planar*** TJ LED	MOCVD
IEEE JQE,51, 8, 2015	AlGaN/InGaN	1.95×10^{-3}	1.97×10^{-2}	***Planar*** TJ LED	MOCVD
APEX, 8, 082103, 2015	InGaN/GaN	5×10^{-4}	0.3×10^{-2}	***Planar***, cascaded TJ LED	PA-MBE
APL, 107,051107, 2015	p^{++}-GaN/n^{++}-GaN	N/A	3.7×10^{-4}	***Planar,*** TJ LED	Ammonia MBE
Nano Lett., 15,10,6696,2015	InGaN/GaN	N/A	3×10^{-2}	***Nanowire***, TJ LED	PA-MBE
This work	Al/GaN	$\sim10^{-3}$	0.4×10^{-2}	***Nanowire***, TJ LED	PA-MBE
APL, 99, 233504, 2011	InGaN/GaN	$\sim10^{-4}$	N/A	***Planar,*** TJ device	PA-MBE



Supplementary Figure 3: Electroluminescence (EL) spectra of LED B and LED C under pulsed biasing condition (10% duty cycle).



Supplementary Figure 4: Relative external quantum efficiency (EQE) of the Al-tunnel junction nanowire LEDs (LED A) measured under CW biasing condition.

Supplementary Note 1:

Impact of nanowire surface coverage, growth and processing on device series resistance:

In deriving the specific resistance, it is important to take into account the fill factor (surface coverage) of nanowires, which is estimated to be ~ 30%. It is seen the device specific resistivity is in the range of 4×10^{-3} Ω-cm^2 based on the I-V characteristics shown in Fig. 4. This specific resistivity includes not only the Al tunnel junction resistance, but also the metal/semiconductor contact resistance and resistance of the *p*-and *n*-GaN layers. It is further expected that the specific resistivity for the Al tunnel junction is significantly smaller than this value for the following two reasons. 1) During the MBE growth of GaN nanowires on Si, ~2-3 nm amorphous SiN_x was formed at the nanowire-Si substrate interface[1-3], which could lead to relatively high resistance of nanowire LEDs. 2) During the device fabrication process, a polymer resist layer was used to passivate and planarize the nanowires. Due to variations in the height of spontaneously formed nanowire arrays, some of the nanowire top surfaces are covered by some residual polymer, which leads to increased device resistance. These issues can be potentially addressed by developing highly uniform nanowire arrays using the technique of selective area growth. Taking these factors into account, we estimated that the specific resistivity for the Al tunnel junction is in the range of 10^{-3} Ω.cm^2, or smaller.

References:

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