SUPPLEMENTAL

# Origin of anomalous piezoresistive effects in VLS grown Si nanowires

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**Nanowire synthesis and tensile strain device (TSD) formation**

An SOI wafer with a highly p-doped (< 0.02 Ωcm) and (110)- oriented 3μm thick device layer is structured with conventional lithographical and reactive ion etching to build up free standing mesa structures with straight <111> orientated sidewall facets. The buried oxide is partly etched using buffered hydrofluoric acid (BHF). To prevent parasitic shunt resistance the device is covered with a 300 nm thick thermally grown $SiO_2$ layer. Again optical lithography and a further BHF etch step is performed to open contact pads at the rear section and a growth notch at the tip of the mesa structure. Au colloids with a diameter of 80 nm in aqueous solution are deposited at the tip facets using dielectrophoresis. VLS growth in a hot wall chemical vapor deposition system using 2% silane diluted in He atmosphere is performed to grow epitaxial <111> orientated Si nanowires perpendicular to the (111) oriented side facets of the mesa structures. These nanowires have an average diameter of 100 nm and electrically reliable and mechanical robust contacts.

After growth the residual gold at the nanowire is removed with an etching procedure consisting of a 20 sec BHF dip to remove the native oxide followed by a 5 min aqua-regia etch step to remove the gold at the nanowire surface followed by another BHF dip to remove the oxide layer formed in the former etchant.

To enable an electrical field modulation of the wire a gate stack consisting of a transparent dielectric layer as well as a transparent conductive layer is deposited at the wire. To investigate the influence of different dielectric materials $SiO_2$ and $Al_2O_3$ are used. Therefore the sample is dipped for 20 sec in a BHF solution and transferred immediately either into an ALD reactor-chamber to deposit a 30 nm thick $Al_2O_3$ layer at the wire or into a thermal oxidation furnace to perform dry thermal oxidation to create a 25 nm thick $SiO_2$ layer. To ensure an electrical stable gate dielectric also at high strain levels an additional 20 nm $Al_2O_3$ layer is deposited on top of the $SiO_2$ layer. To enable optical measurements 180nm ITO was deposited as transparent gate material. Finally Ti/Au contacts are formed at the ITO layer to enable wire bonding.

For straining experiments the fully featured TSD is aligned and glued with epoxy onto a steel plate with the NW axis parallel to the longitudinal axis of the plate. To apply uniaxial strain along the <111> growth direction the sample/ steel plate stack is mounted in a 3-point bending device.

**Strain determination**

All measurements were performed at room temperature. The strain at the wire was measured using a confocal μ-Raman setup (Alpha300, WITec) in back scattered geometry with a grating monochromator and CCD camera (DV401_BV, Andor). A frequency doubled Nd:Yag laser at an excitation frequency of 532 nm is used polarized along the NW axis. The exciting laser power was limited to avoid a shift in the Raman spectra related to nanowire heating. The laser is focused on the sample to a diffraction limited spot with a diameter of ~500 nm. The relation between applied uniaxial tensile strain and the respective shift in the Raman spectra is given by:

$$\Delta\Omega \cong - k * \varepsilon_{\parallel}$$

with $\Delta\Omega$ representing the shift in the peak position of the Raman spectra, k a proportionality factor and $\varepsilon_{\parallel}$ the strain in <111> growth direction of the nanowire. Calibration measurements comparing Raman peak shifts with physical length change of the NW reveal a proportionality factor k = 326 $cm^{-1}$.[1] Therefore the length and elongation of the Si NW under stress was determined in situ by SEM imaging, measuring the distance between the two ends of the NW. The epitaxial growth of the Si NWs perpendicular to the Si pads (i.e. to the direction of the electron beam) enables a precise measurement of the NW elongation with approximately 10nm precision without any "hidden" displacement along the electron beam direction. Thus, the maximal peak shift of about 8 $cm^{-1}$ corresponds to a maximal applied strain value of 2.4 %.

Comparative strain measurements before and after $Al_2O_3$ coating via ALD showed no significant change in the measured Raman signal.

**Back-gate measurements**

Silicon NWs are grown on a plain Si (111) wafer using the same growth parameters as for the TSD and transferred into ISO through ultrasonic treatment. The NWs are dispersed onto a Si substrate covered with 200nm thermally grown $SiO_2$ which serves as gate dielectric. A Raith e-Line electron beam lithography tool is used to contact a single nanowire in four point measurement geometry. For the back-gate transfer-characteristic measurements a current is applied to the outer two contacts while the voltage difference along the wire is measured at the inner two contacts to minimize measurement errors. The back-gate voltage is applied to the silicon bulk and is swept between -12V and +12V.

(1) Wagesreither, S.; Bertagnolli, E.; Kawase, S.; Isono, Y.; Lugstein, A. *Nanotechnology* **2014**, *25*, 455705.