Supporting Information for:

Synthetically Encoding 10-nm Morphology in Silicon Nanowires

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Supporting information includes:
NW Growth
Etching and Device Fabrication
Electron and Raman Microscopy
Finite-Element Simulations

NW growth

Si NWs were grown with a home-built, hot-wall CVD system using SiH_4 (Voltaix), PH_3 (Voltaix; diluted to 1000 ppm in H_2), and H_2 (Matheson TriGas 5N semiconductor grade) gases. The CVD system consists of a quartz tube furnace (Lindberg Blue M) with 1 inch diameter bore, fast-responding mass-flow controllers (MKS Instruments P4B), a pressure control system (MKS Instruments 250E), and vacuum system with base pressure of $1x10^{-4}$ Torr. The CVD system was computer-controlled using custom Labview software to enable rapid and reproducible modulation of the NW growth conditions and gas flow rates. Calibration runs indicated that changes in flow rate were achieved on time scales <1 s and that complete exchange of gas within the quartz tube was achieved on a time scale of ~5 s. Thus the resolution of ENGRAVE structures was primarily limited by the kinetics of the NW growth or etching process and not by the mechanics of the CVD system. For a typical NW growth run, citrate-stabilized ~100 nm Au catalysts (BBI International) were dispersed on 2 cm x 1 cm Si wafers (University Wafer; p-type Si with 600 nm thermal oxide) that had been functionalized with poly-L-lysine solution (Aldrich). These growth substrates were inserted into the center of the tube furnace, and the furnace temperature was ramped to 450 °C to nucleate NW growth for between 5 to 60 min using 2.00 sccm SiH_4 and 200.0 sccm H_2 at 40.0 Torr total reactor pressure. The reactor temperature was then cooled (1 °C/min) to 420 °C and ENGRAVE structures were encoded by introducing PH_3 gas with a tightly controlled flow profile, as discussed in the text.

Etching and device fabrication

To fabricate ENGRAVE structures, NWs were transferred from the growth substrates onto Si wafers coated with 100 nm thermal oxide and 200 nm Si nitride (Nova Electronic Materials). NWs, which were then lying flat on the substrate, were etched by immersing in concentrated buffered hydrofluoric acid (Transense BHF Improved) for 10 s, rinsing in water and isopropanol, etching in KOH solution (20.0 g KOH; 80.0 g water; 20 mL isopropanol as top surface layer) at 40 °C for variable times up to 90 s, and rinsing in water and isopropanol. To fabricate Si NWs with Noble metal structures, Si NWs were etched

as described above and then placed in an electron-beam evaporator (Thermionics VE-100) for deposition of 50 nm Au at normal incidence with a rate of ~1 Å/s at a pressure $<1 \times 10^{-7}$ Torr. Thermal oxidation of NWs was performed for 3 min in a quartz tube furnace with 100 Torr O_2 at 1000 °C. NW devices were fabricated by defining metal contacts to individual NWs using electron-beam lithography followed by electron-beam evaporation of 3 nm Ti and 150 nm Pd. Devices were measured under nitrogen environment using a home-built probe station equipped with W probe tips (Signatone) connected to a Keithley 2636A sourcemeter. Single voltage pulses were applied using a square wave pattern with nominal width of 100 μs, the minimum pulse width produced by our measurement system. Prior to operation as a resistive switch for non-volatile memory, an electroforming process consisting of multiple voltage sweeps to high bias was performed. A typical forming process contained two sweeps from 0-30 V, two sweeps from 0-25 V and two sweeps from 0-20 V. Following the final 0-20 V sweep, additional sweeps from 0-15 V would reproducibly yield the characteristic 'switching' *I-V* behavior shown Fig 5D.

Electron and Raman microscopy

SEM imaging was performed with an FEI Helios 600 Nanolab Dual Beam system with an imaging resolution <5 nm using a typical acceleration voltage of 5 kV and imaging current of 86 pA. Raman imaging was performed with a Renishaw inVia Raman microscope using a HeNe laser source at 633 nm and 50x objective. Spectra were collected by raster scanning the sample in steps of 100 nm using an averaging time of 1.0 s. Prior to Raman image collection, the Au-coated substrates were immersed in an aqueous solution of methylene blue (Aldrich), rinsed with water, and dried with flowing N_2. Three-dimensional plots of the Raman signal were generated by summing all counts within the 1580-1650 cm^{-1} spectral window.

Finite-element simulations

Optical and device simulations were performed using the Comsol Multiphysics commercial software package. Three-dimensional optical simulations were implemented using the total-field, scattered-field

method. The background field was evaluated with a plane wave normally-incident on the substrate using periodic boundary conditions on the four horizontal boundaries, a perfectly matched layer (PML) on the lower boundary, and the plane wave source on the upper boundary. The scattered field was then solved after adding the Si/Au plasmonic structure to the simulation domain and replacing all boundaries with PMLs. Images of the surface plasmon modes were generated by evaluating the scattered electric field intensity ($|E|^2$) in a horizontal plane 3 nm above the top surface of the NW. Finite-element device simulations were performed using a modification of our previously published model[50] and used cylindrical symmetry to represent the three-dimensional structure. The external voltage was applied to Ohmic contacts on the n-type regions, and the simulations included realistic doping profiles as well as drift-diffusion and recombination processes to reproduce the current-voltage characteristics of the devices.