Supporting information

Demonstration of enhanced switching variability and conductance quantization properties in a SiO_2 conducting bridge resistive memory with embedded 2D MoS_2 Material

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S1. MoS_2 SEM images

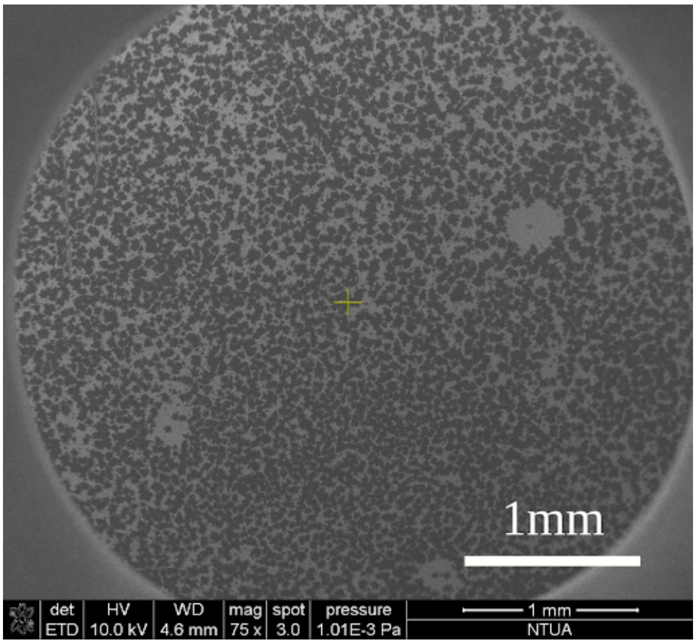
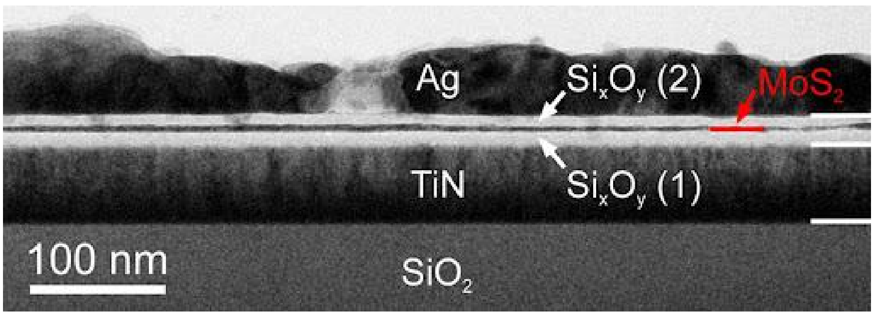


Figure S1. SEM image showing CVD grown MoS_2 with multiple layers.

S2. TEM Structural Analysis

a.



b.

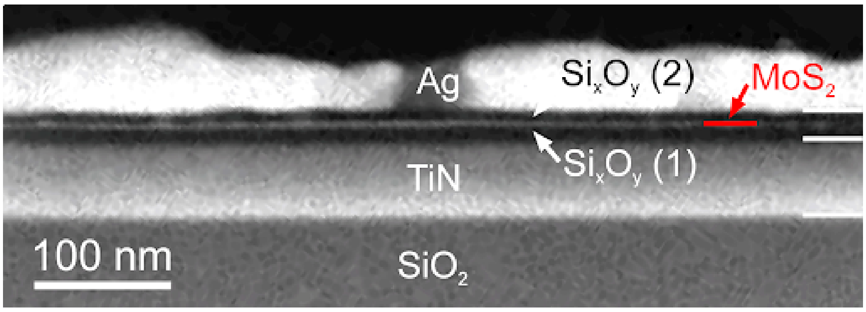
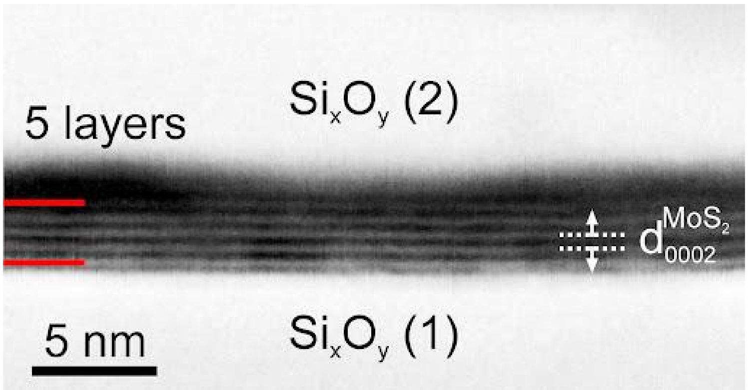


Figure S2. a. Cross sectional TEM (XTEM) micrograph obtained along the $[1\bar{1}0]_{Si}$ zone axis (ZA) of the Si wafer. Few-layer of MoS_2 was successfully grown on the amorphous SixOy (1) layer exhibiting good surface coverage. **b.** Z-contrast high-angle annular dark field (HAADF) STEM image from around the same area. The average thickness of each alternate layer is presented in table 1.

a.



b.

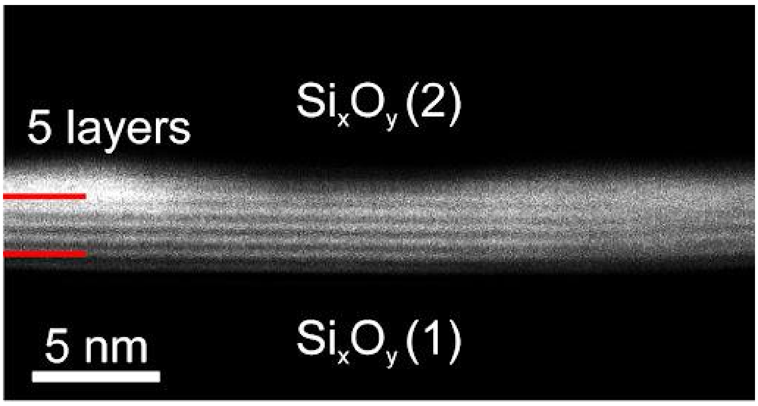


Figure S3. a. Annular bright field (ABF) and **b.** Z-constrast HAADF cross-sectional STEM images showing a MoS_2 film consisting of five (0002) layers, with an interplanar space of 0.65±0.5 nm, which is close to the nominal value of hexagonal MoS_2 (d_{0002}=0.62 nm).

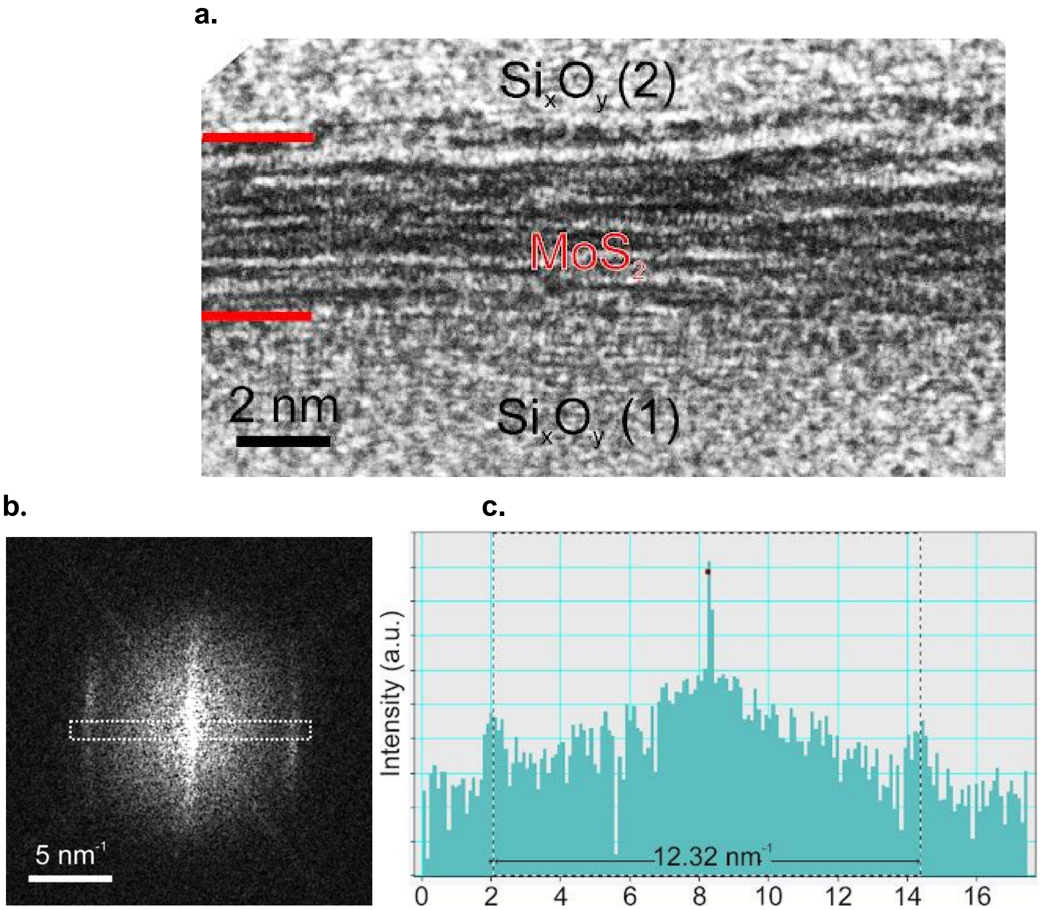


Figure S4. a. High magnification cross-sectional HRTEM image from the MoS_2 layer. The in-plane lattice spacings are not clearly resolved, due to their low spacing and the fact that MoS_2 is not well ordered, as it grown on top of an amorphous Si_xO_y layer and may exhibit tilted grains. **b.** Diffractogram obtained from the HRTEM image by Fourier transform and, **c.** corresponding intensity profile from the delineated region in b. The in-plane g-vector was measured at ~ 6.16 nm^{-1}, corresponding to 0.16 nm in direct space, which is consistent with the $d_{11\bar{2}0}$ interplanar spacing of MoS_2.

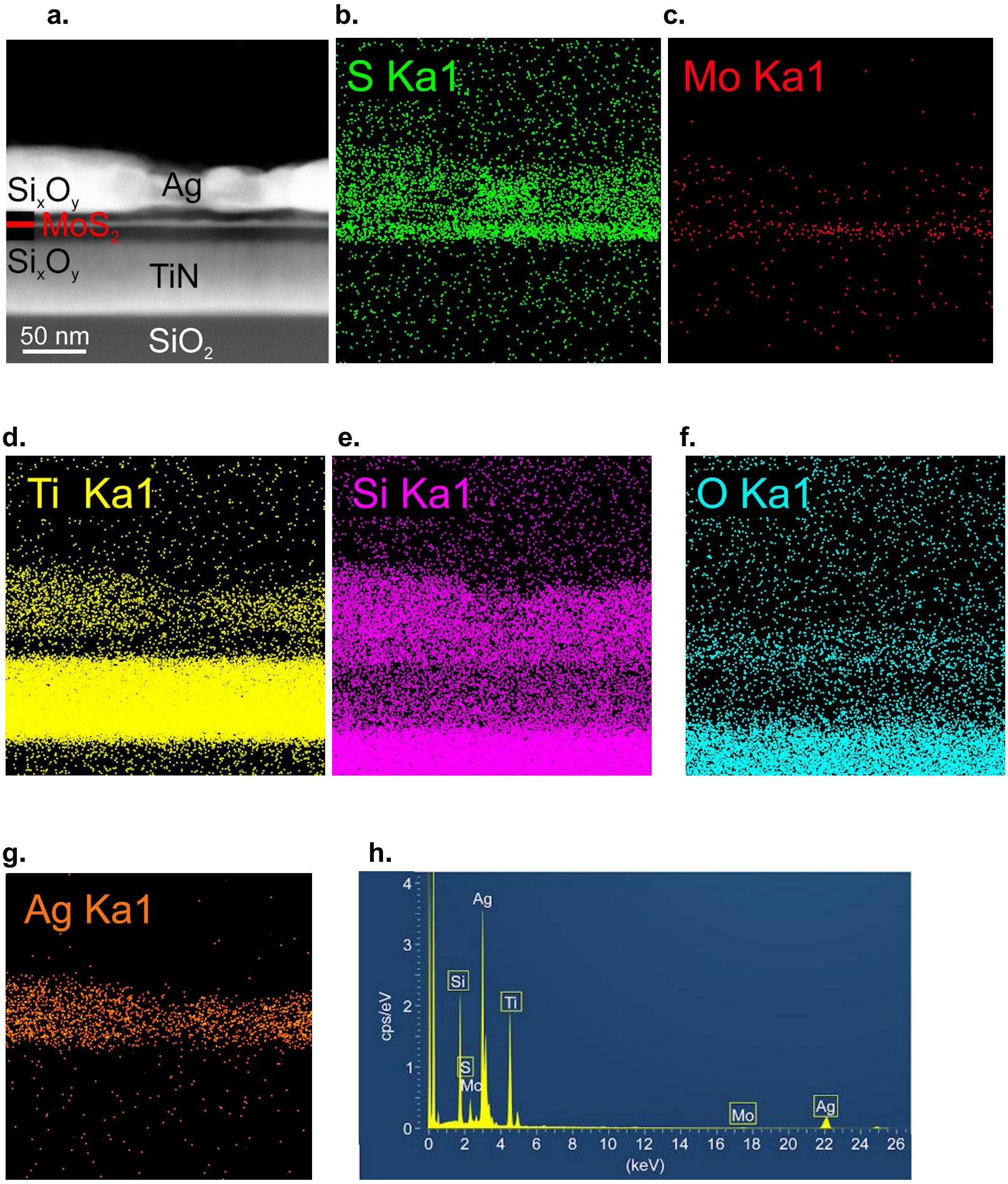


Figure S5. a. STEM image from the multilayer structure, and **b-g.** Elemental maps obtained by EDX. The appearance of Si, S, and Ti inside the Ag layer is attributed to background scattering as well as to the influence of the ion milling during TEM sample preparation. **h.** Overall EDX spectrum from this area. The lines used for the elemental maps are indicated.

S3. I-Vs

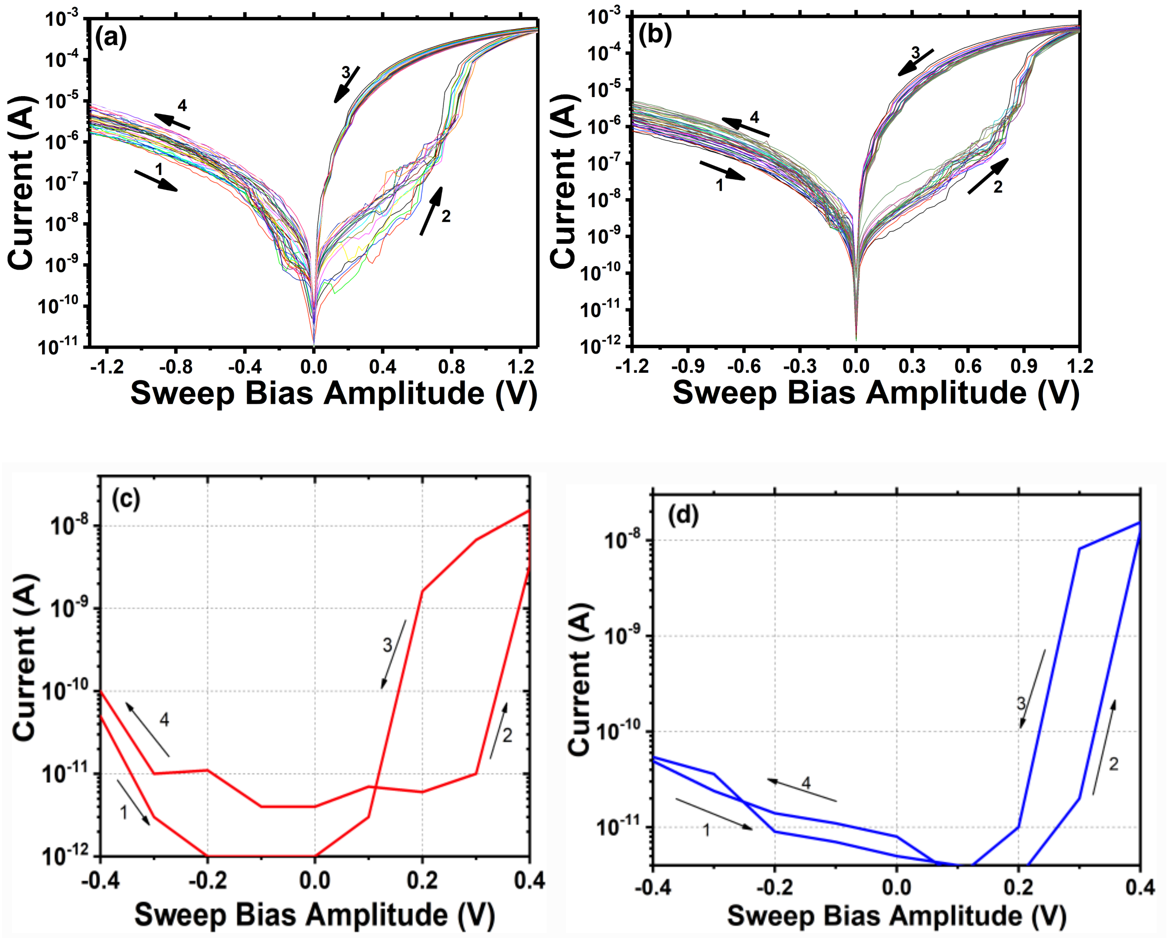


Figure S6. a) I-V cycles for the reference sample and b) for the MoS_2 embedded sample, c) I-V cycles for lower compliance currents for the reference sample and d) for the MoS_2 embedded sample indicating the threshold switching effect.

S4. Device Area and Temperature Dependence

Insights regarding the potential existence of CFs within our device's active core are presented below. More specifically, the total independence of the LRS distribution from the total device area (Figure S7a) provides strong pieces of evidence towards the formation of percolating CFs.

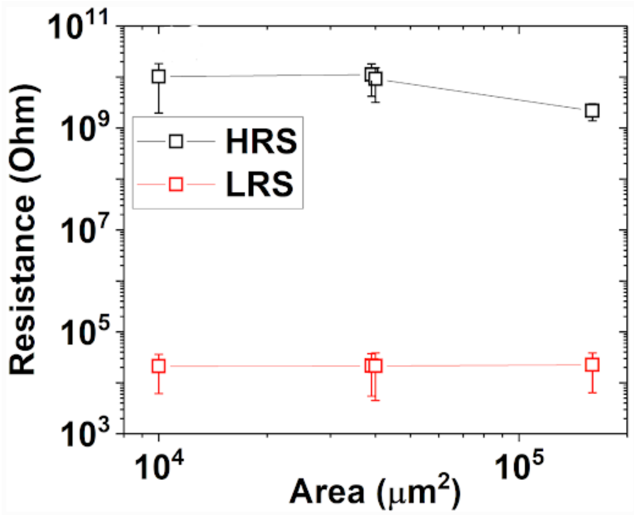


Figure S7. Distribution of both HRS and LRS as a function of the total device area.

S5. Conduction Mechanism

A further examination of the conduction mechanism was done in order to gain insight of how the thin films of CVD grown MoS_2 affect the behavior of the memory device. For this reason, distributions of current and voltage during the SET process were plotted in logarithmic scale. This is an attribute of the Space-Charge-Limited-Current (SCLC) mechanism whose function is based on nonlinear features of the IV characteristics. In our case, figures and represent the forward part of the IVs, for reference and MoS_2 embedded stacks respectively. We observed three different segments of the distribution, two linear that are represented by slope-a and slope-c and the nonlinear increase region (slope-b). The first region refers to V<0.5V, the nonlinear region expands from 0.5V to 1V with the third occur at V>1V. Theory states that the first region with slope-a is represented by the proportionality of current and voltage ($I \propto V$) and reflecting ohmic behavior while the third region with slope-c implements the Child's law ($I \propto V^2$). [1]

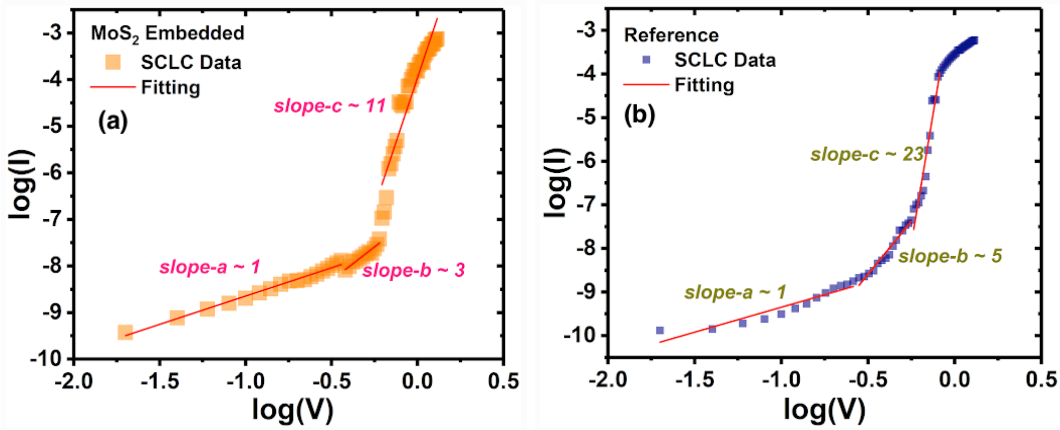


Figure S8. I-Vs representing SCLC mechanism for MoS_2 embedded (a) and reference samples (b) respectively.

S6. CDF device-to-device measurements

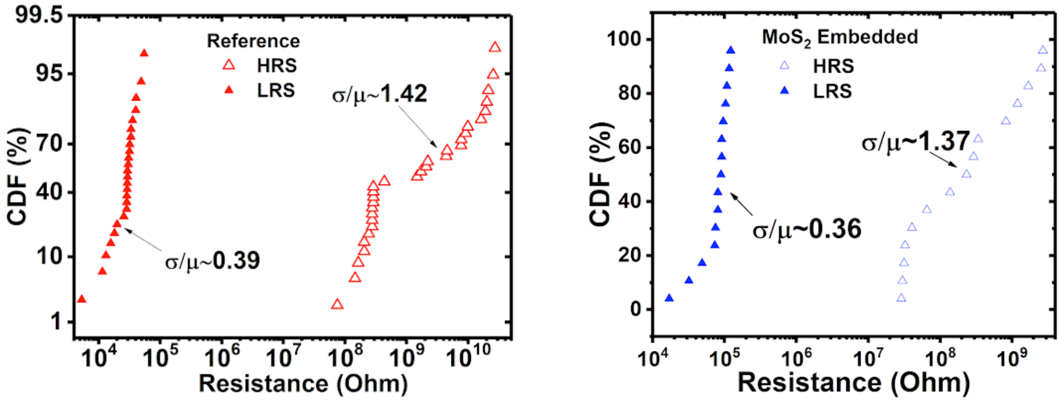


Figure S9. Device-to-device cumulative distribution functions.

S7. Device-to-device endurance and retention measurements for MoS_2 embedded samples

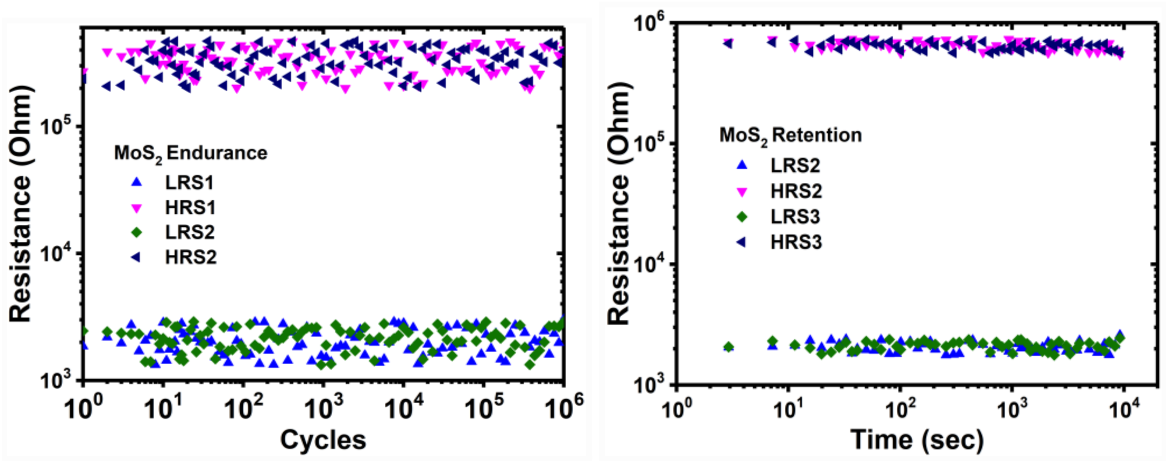


Figure S10. Device-to-device endurance and retention for MoS_2 embedded samples.

S8. SiO_2 various thicknesses and CBRAM performance

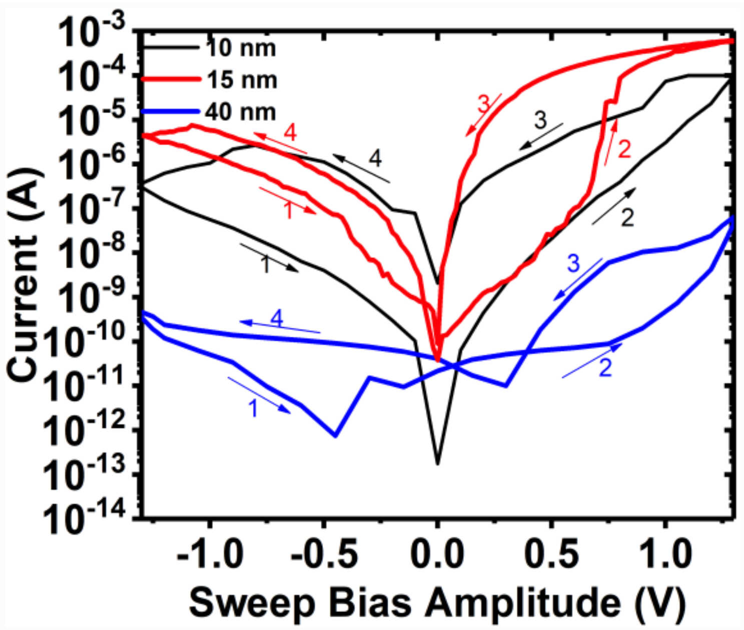


Figure S11. I-V characteristics for various SiO_2 thicknesses (10 nm, 15 nm and 40 nm).

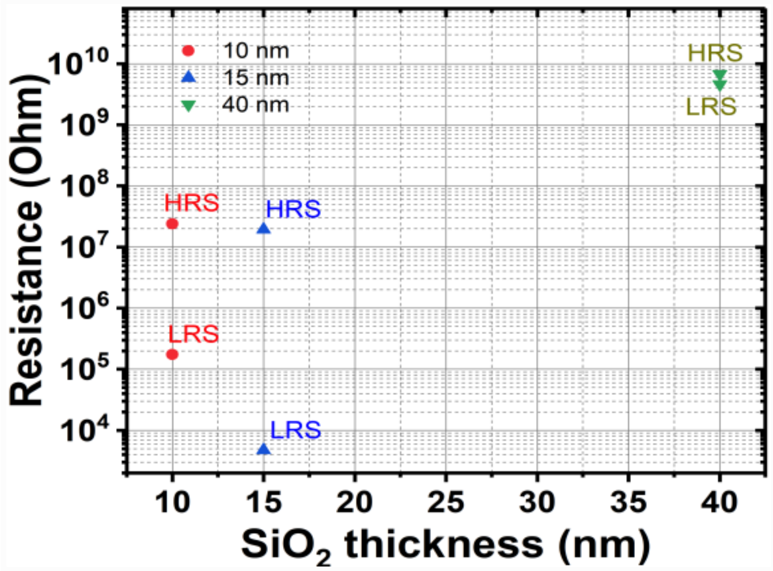


Figure S12. HRS and LRS for the various SiO_2 thicknesses.

References

1. Voronkovskii VA, Aliev VS, Gerasimovaet AK, Islamov DR. Conduction mechanisms of TaN/HfOx/Ni memristors. *Mater. Res. Express*. 2019, **6**, 076411.