Supplementary Materials for "Topology-optimized ultra-compact all-optical logic devices on silicon photonic platforms"

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S1. The effective permittivity of the Si layer

Under the approximation of effective medium theory[1, 2], the effective permittivity of silicon corresponding to the Si layer is taken by the mode analysis in the finite element method. In the 2D calculation model, periodic boundary conditions are used in left and right boundaries. 3μm-thickness air and SiO_2 areas are built at the top and bottom of the Si layer. By the calculation, effective permittivities of Si in different thicknesses are plotted in Fig. S1(a). The steady-state intensity distributions for five representative cases are shown in Fig. S1(b), whose thicknesses are from 200nm to 240nm, respectively. We use the value being 8.04, corresponding to 220nm-thickness, in the TO process.

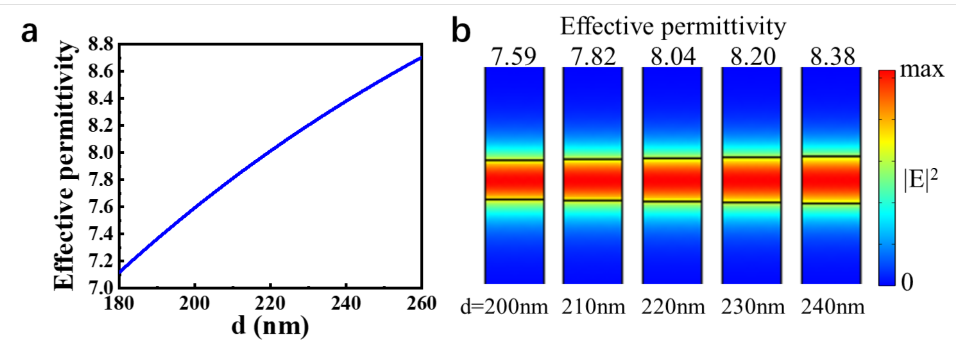

Fig. S1. (a) The effective permittivity of the Si layer with various thicknesses d on the SiO_2 substrate. (b) The steady-state intensity distribution of the electric field with d=200nm, 210nm, 220nm, 230nm, and 240nm.

S2. Artificial modification method and its effect on device properties

In this section, we discuss artificial modifications and their effect on the device's properties.

The TO design pattern by 1000 iterations is shown in Fig. S2(a). The design has a good performance at the communication band, i.e. the nearly equal output intensity of OR and XOR ports. However, some details of the structure are too narrow to be fabricated experimentally. Thus, we provide specific modifications, as shown in Fig. S2(b). The green part is removed, and the red part is added to widen the narrow area up to 80nm. After the modifications, the final design is given in Fig. S2(c).

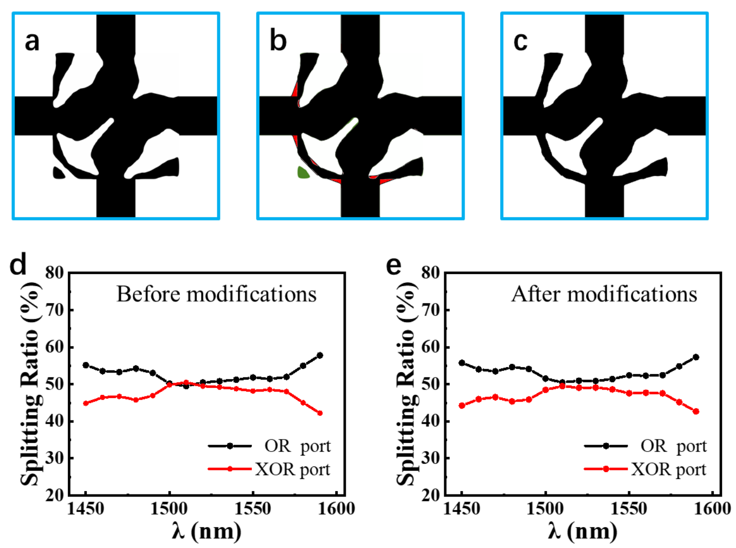

Fig. S2. The schematic diagram of artificial modifications of the final design. (a) The TO design after 1000 iterations. (b) The artificial modifications. The green part is removed, and the red part is added to widen the narrow area up to 80nm. (c) The final design. The splitting ratios of the XOR and OR gates (d) before modifications, and (e) after modifications.

Now, we compare the performances between the original design and the modified design. When the incident light at Input A is turn-on, splitting ratios of XOR and OR ports are plotted in Figs. S2(d) and S2(e). There is almost no difference between them. That is to say, artificial modifications do not change the performance of the device.

S3. Adjustments of empirical constants

In the TO design process, we have to set empirical constants γ_1 and γ_2 carefully, so that the 3D model can meet the requirement of the logic device.

First, we select a numerical value of γ_1, and another constant γ_2 is set as γ_1+0.1, for example, γ_1=0.4 and γ_2=0.5. Then, we execute the TO procedure in the 2D model and get the design pattern of the device, as shown in the inset of Fig. S2. The 3D structure is directly built by using the 2D pattern. By the simulation in 3D, we get the splitting ratio of XOR and OR ports, 36:64. It is not good to realize the logic gate. So, we adjust the constant, from 0.4 to 0.8, and expect to find a 3D ratio of 50:50. As shown in Fig. S3, the ideal ratio appears if the empirical constant γ_1 is set as 0.6 or 0.7. Thus, we decide to set the empirical constants as γ_1=0.6 and γ_2=0.7.

Additionally, we also find an interesting phenomenon in above adjustments. The TO procedures are executed independently every time. But the patterns we get are similar, except for the length of the trench in the center of the design pattern. The longer trench, the higher power in the XOR port.

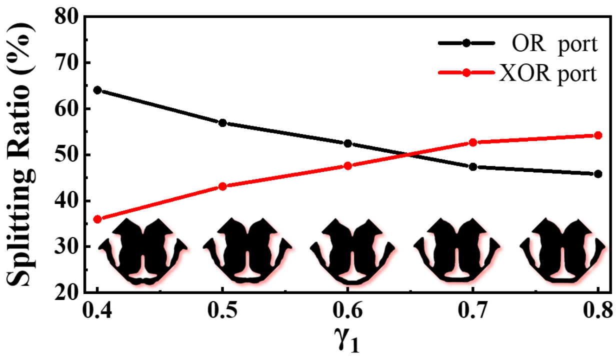

Fig. S3. Splitting ratios of the 3D model with empirical constants γ_1, from 0.4 to 0.8. The insets are optimized patterns in different empirical constants γ_1.

S4. The total transmittance with the length of the side of the design square.

In our work, we try to design the logic unit by the TO method in the square with different sizes, from 1μm to 1.5μm. It is found that the total transmittance is too low if the size is too small. In Fig. S4, we plot the total transmittance along with the side length of the squares. For our TO algorithm, the transmittance is significantly low when the length is less the 1.2μm. There is almost no difference from 1.3μm to 1.5μm. So, we choose the length 1.3μm as the footprint of our device.

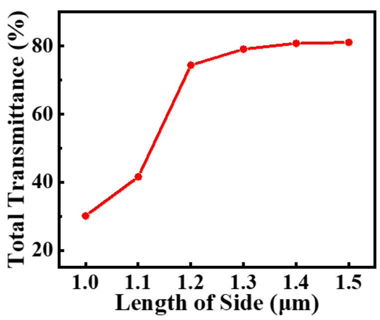

Fig. S4. The total transmittance of different lengths of the side of the square.

S5. The insertion loss of the XOR and OR gates.

Here we provide the measured result for the insertion loss (IL) of XOR and OR gates. The IL is calculated as follow:

$$IL = 10\lg(T_{device} / T_{waveguide}), \tag{S1}$$

where T_{device} represents the transmission of the device, and $T_{waveguide}$ is the transmission of the straight waveguide. In fact, the IL of XOR and OR gates can be obtained by deducting the losses of 1D grating and waveguides from the overall loss. The calculated results are shown in Fig. S5. A low loss (-0.96dB) for the device can be seen at λ=1550nm. In the whole communication band, the losses are lower than -3dB. Our design shows a good performance with a high transmission.

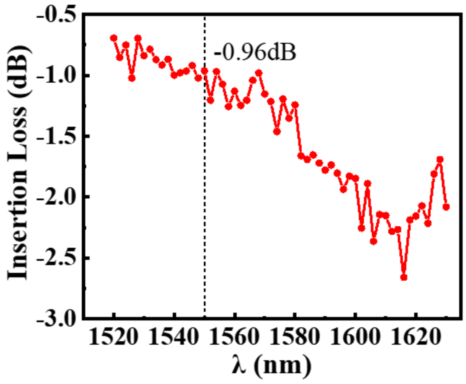

Fig. S5. The insertion loss of XOR and OR gates.

S6. The phase and amplitude of bias lights.

In Fig. 3(a) of the main text, the connection waveguide of the logic units has a 300nm length. For various wavelengths, optical distances are different. We need to adjust the phase of the BLs to realize the ideal destructive interference at output ports. By the simulation, we get the phase difference of signals between the BL_1 and the Input A, as shown in Fig. S6(a). The black points are the phase difference of simulation results. By the fitting, the function of the phase difference is

$$\Delta\varphi = 0.0054\lambda - 7.86624. \tag{S2}$$

The red line is the fitting curve. In the simulation, we also consider the coefficients multiplied by the amplitudes of signals at BLs. Their values are determined by the loss of the device. The simulation coefficients at two input channels, η_{BL_1} and η_{BL_2}, are shown in Fig. S6(b).

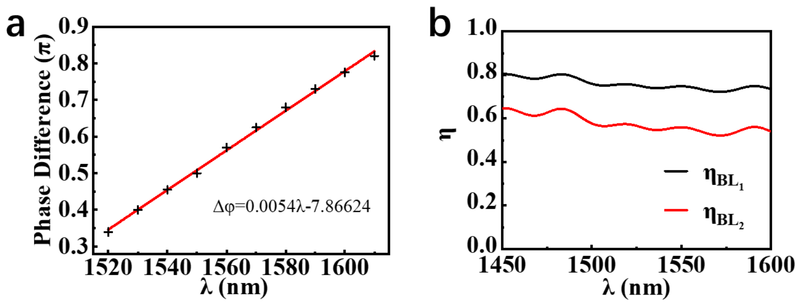

Fig. S6. (a) The phase difference between BL_1 and Input A; BL_1 and BL_2. (b) The coefficients of signals at BL_1 and BL_2 to compensate for the transmission loss.

S7. The experimental set-up and the measurement method for the logic device.

The experimental set-up is shown in Fig. S7. Our logic chip has four input ports, named as Input A, Input B, BL_1, and BL_2. The continuous wave laser is used to pump the single mode fiber (SMF) at the communication band (1520nm-1630nm). A quarter-wave plate (QWP) and a half wave plate (HWP) are used to make sure the linear polarization of the pumping laser. Before entering the chip, the incident wave is split into four paths with different intensities in free spaces, where an HWP combined with a polarization beam splitter (PBS) could split the laser beam into two paths with the controlled ratio of intensities. In this case, three PBSs can split the laser beam into four paths (marked as ①, ②, ③, and ④), which are coupled into four SMFs by couplers (black semicircles in Fig. S6). Then, four input lights are guided by SMFs and coupled to the logic chip through the fiber array and 1D gratings.

In experiments, we find that phases of laser beams in four independent SMFs are unstable. It is noted that many factors could affect the phase, including the temperature, the eigenvibration of the fibers, and so on. We find that the phase difference for any pair of SMFs has changed from 0 to 2π after 20-30 seconds, which is enough to finish the measurement of XOR and OR gates with only two incident signals. But for the cascaded logic gates, more input lights are needed and the stabilized phase differences are extremely hard to be realized. Thus, an alternative method should be used to test the logic chip.

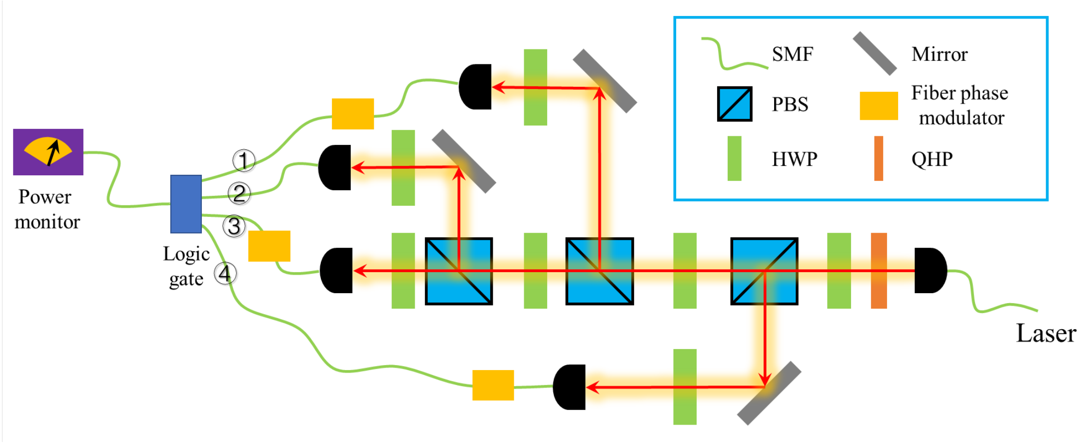

Fig. S7. Experimental set-up of measurement for the logic gate chips.

We add three fiber phase modulators to periodically change the phases of the light in fibers, where the modulation frequencies of three phase modulators are selected from 1Hz to 2kHz, and each modulation frequency is much larger or smaller than others. Moreover, these three frequencies are much larger than that of the spontaneous phase-changed in fibers. In this case, we can think that the phases of signals in fibers are nearly stable in a short interval of time (about 1s). Next, we illustrate the measurement principle in detail.

Firstly, we express the output field from XOR and OR ports as:

$$E_1 = 0.5\sqrt{2}a_A e^{i\pi/2} + 0.5\sqrt{2}a_B e^{i\phi_1(t)}, \tag{S3}$$

$$I_1 = |E_1|^2 = 0.5a_A^2 + 0.5a_B^2 + a_A a_B \sin(\phi_1(t)), \tag{S4}$$

where E_1 (I_1) is the output field (intensity) at the XOR or OR port. a_A and a_B are amplitudes of incident waves at Input A and B, where we have $a_A = a_B$. As mentioned in the main text, an additional phase ($\pi/2$) should be added to the incident signal coming from Input A. $\phi_1(t)$ represents the modulation phase of the signal injected into the Input B. It is noted that $\phi_1(t)$ can be taken as a periodic function along with the time t (like sin, square wave, or sawtooth function). The frequency of $\phi_1(t)$ is set as 10Hz. The difference between the maximum and minimum of $\phi_1(t)$ should equal to 2π, so that the maximum value ($0.5a_A^2 + 0.5a_B^2 + a_A a_B$ corresponds to the output signal of OR_11) and minimum value ($0.5a_A^2 + 0.5a_B^2 + a_A a_B$ corresponds to the output signal of XOR_11) can be obtained when the modulated phase equals to $\phi_1(t) = \pi / 2$ and $\phi_1(t) = 3\pi / 2$, respectively. In the experiment, a high-speed optical power monitor is used to record the curve of the output intensity, and the measured maximum and minimum values of output signals correspond to the logic state of OR_11 and XOR_11. Additionally, as for other logic states (XOR_10, XOR_01, OR_10, OR_01), only one input signal should be used, making the influence of the spontaneous phase fluctuation could be ignored. Hence, these logic states could be easily detected.

And then, we consider cascaded gates (XNOR, NAND, and NOR), where three input ports (A, B, and BL_1) should be used. Except for the phase modulation added on the signal injected into Input B (the same to XOR and OR gates), another phase modulation on the signal injected into the BL_1 should also be applied. In this case, the output field (E_2) and intensity (I_2) from the middle channel could be expressed as:

$$E_2 = 0.5\sqrt{2}E_1 + 0.5\sqrt{2}a_{BL_1}e^{i\phi_2(t)}, \tag{S5}$$

$$\begin{aligned} I_2 &= |E_2|^2 \\ &= 0.25a_A^2 + 0.25a_B^2 + 0.5a_{BL_1}^2 + 0.25a_Aa_B\sin(\phi_1(t)) \\ &\quad + 0.25\sqrt{2}a_Aa_{BL_1}\sin(\phi_2(t)) + 0.25\sqrt{2}a_Ba_{BL_1}\cos(\phi_2(t) - \phi_1(t)), \end{aligned} \tag{S6}$$

where a_{BL_1} is the amplitude of the bias light at BL_1. $\phi_2(t)$ represents the modulation phase of the signal injected into BL_1. Especially, the modulation frequency of $\phi_2(t)$ is set as 1kHz, which is 100 times larger than that of $\phi_1(t)$.

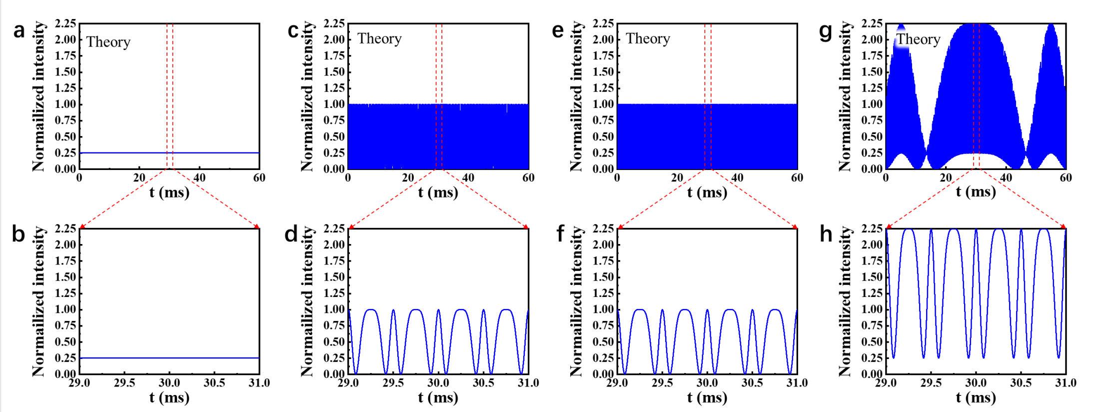

Fig. S8. Theoretical results of the measurement method for the XNOR gate. (a)-(b) Input A and B are both turn-off. (c)-(d) Input A is turn-on but Input B is turn-off. (e)-(f) Input B is turn-on but Input A is turn-off. (g)-(h) Input A and B are both turn-on. (b), (d), (f), and (h) are enlarged views of key parts for (a), (c), (e), and (g), respectively.

We firstly consider the XNOR gate. When Inputs A and B are both turn-off and only the BL_1 is turn-on, the output intensity is a constant, i.e. $I_2 = 0.5a_{BL_1}^2$ as shown in Figs. S8(a) and S8(b). When one of Inputs A and B is turn-on, the output intensity is:

$$I_2 = 0.25a_A^2 + 0.5a_{BL_1}^2 + 0.25\sqrt{2}a_A a_{BL_1}\sin(\phi_2(t)),$$

$$\text{or } I_2 = 0.25a_B^2 + 0.5a_{BL_1}^2 + 0.25\sqrt{2}a_B a_{BL_1}\sin(\phi_2(t) - \phi_1(t)),$$

as shown in Figs. S8(c)-S8(f). To realize the logic function, the destructive interference is needed in these two cases. So, we take the minimum of the intensity as the logic signal XNOR_01 (XNOR_10). It is worthy to note that this minimum of the XNOR gate is zero theoretically.

When Inputs A and B are both turned on, the output intensity is expressed as Eq. (S6). In this case, the signal from Input A constructively interferes with that from Input B, and then, the interference signal of Inputs A and B destructively interferes with the signal from BL_1. Finally, the output signal arrives at the XNOR port. It is known that the maximum of the intensity curve can be taken when constructive interference appears among these three signals. When the phase of $\phi_2(t)$ changes π, the phase of $\phi_1(t)$ remains unchanged, owing to the much larger modulated frequency of $\phi_2(t)$. That is to say, the expected signal of XNOR_11 can be taken as the local minimum close to the maximum of the curve. As shown in Figs. S8(g) and S8(h), the maximum of the curve is taken at t=30ms. The logic signal intensity for XNOR_11 is obtained at t=29.9ms, and its numerical value is 0.25, which is equal to that of XNOR_00 in Fig. S8(a).

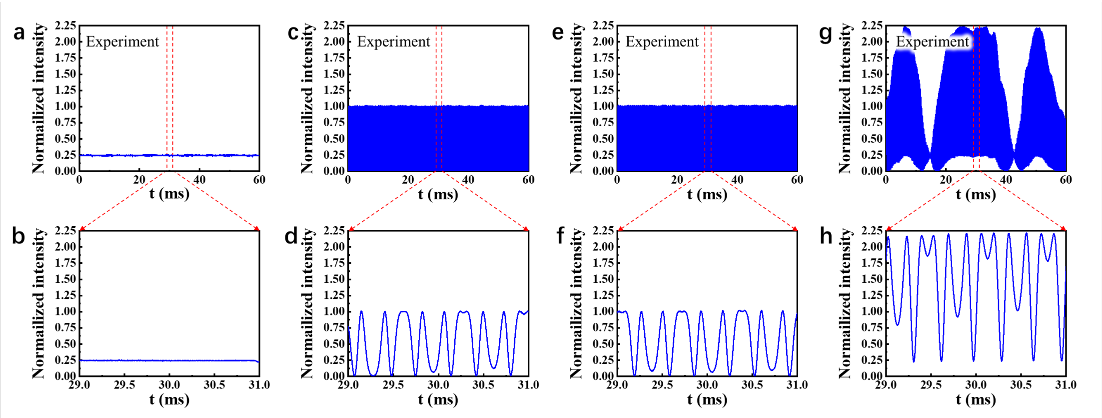

Fig. S9. Experimental results of the measurement method for the XNOR gate. (a)-(b) Input A and B are both turn-off. (c)-(d) Input A is turn-on but Input B is turn-off. (e)-(f) Input B is turn-on but Input A is turn-off. (g)-(h) Input A and B are both turn-on. (b), (d), (f), and (h) are enlarged views of key parts for (a), (c), (e), and (g), respectively.

In Figs. S9(a), S9(c), S9(e), and S9(g), we show experimental intensity curves corresponding to four logic cases as described above. And Figs. S9(b), S9(d), S9(f), and S9(h) display the enlarged views of curves. It can be seen measured results are in good agreement with theoretical results. We take output signals for the XNOR gate at various wavelengths (from 1520nm to 1605nm), and then we calculate and plot ERs in Fig. 4 of the main text.

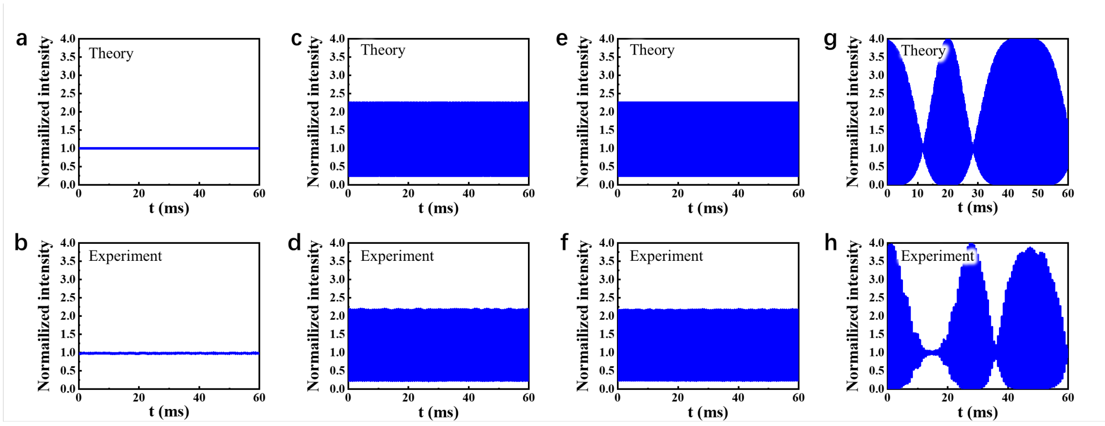

Fig. S10. Theoretical and experimental results of the measurement method for the NAND gate. (a)-(b) Input A and B are both turn-off. (c)-(d) Input A is turn-on but Input B is turn-off. (e)-(f) Input B is turn-on but Input A is turn-off. (g)-(h) Input A and B are both turn-on. (a), (c), (e), and (g) are theoretical results, (b), (d), (f), and (h) are experimental results, respectively.

As for the NAND gate, Eqs. S5 and S6 can also be applied except for the amplitude of the bias light at BL_1 being changed to $\sqrt{2}$. We can get output intensities of logic signals in the same way.

Theoretical and experimental intensity curves are shown in Fig. S10. Four logic states correspond to Figs. S10(a) and S10(b), Figs. S10(c) and S10(d), Figs. S10(e) and S10(f), Figs. S10(g) and S10(h), respectively. It is worthy to note that the NAND_11 case shows the output intensity is zero, which corresponds to the logic function of the NAND gate.

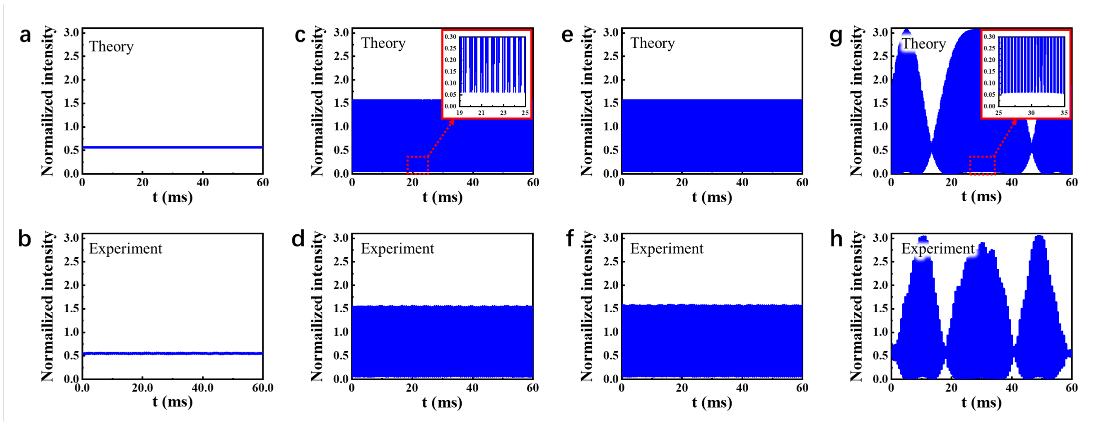

Fig. S11. Theoretical and experimental results of the measurement method for the NOR gate. (a)-(b) Input A and B are both turn-off. (c)-(d) Input A is turn-on but Input B is turn-off. (e)-(f) Input B is turn-on but Input A is turn-off. (g)-(h) Input A and B are both turn-on. (a), (c), (e), and (g) are theoretical results, (b), (d), (f), and (h) are experimental results, respectively.

In Fig. S11, we plot theoretical and experimental results for the NOR gate. The measurement method in such a case is identical with the cases for XNOR and NAND gates, except for the amplitude of the bias light at BL_1 being changed to $0.75\sqrt{2}$. The output intensity being 0.5625 (logic signal 1) can be obtained when Inputs A and B are both turn-off, as shown in Figs. S11(a) and S11(b). In the other three cases (Figs. S11(c)-S11(h)), the logic output intensity can be calculated and measured as 0.0625 (1/9 of 0.5625). The experiment measurement corresponds well to the theoretical results.

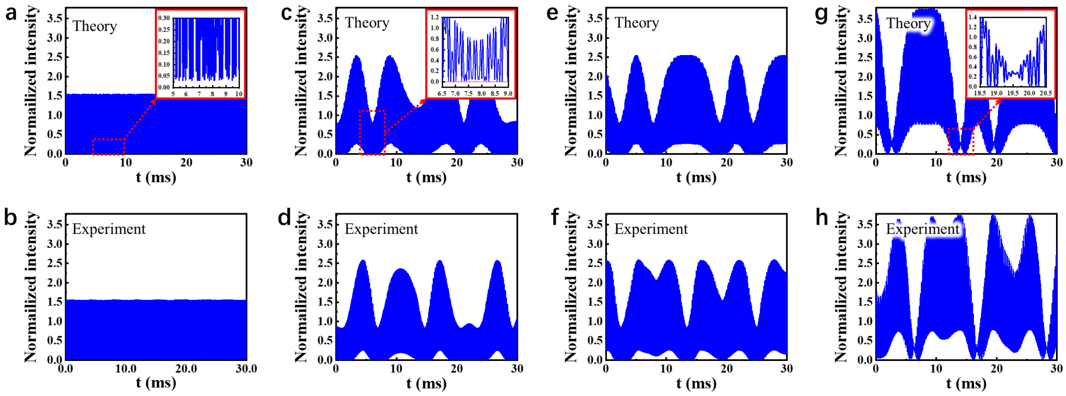

Fig. S12. Theoretical and experimental results of the measurement method for the AND gate. (a)-(b) Input A and B are both turn-off. (c)-(d) Input A is turn-on but Input B is turn-off. (e)-(f) Input B is turn-on but Input A is turn-off. (g)-(h) Input A and B are both turn-on. (a), (c), (e), and (g) are theoretical results, (b), (d), (f), and (h) are experimental results, respectively.

In the last case for the AND gate, additional formulas are needed as follows:

$$E_3 = 0.5\sqrt{2}E_2 + 0.5\sqrt{2}a_{BL_2}e^{i\phi_3(t)}, \tag{S7}$$

$$\begin{aligned} I_3 = |E_3|^2 = {} & 0.125a_A^2 + 0.125a_B^2 + 0.25a_{BL_1}^2 + 0.5a_{BL_2}^2 \\ & + 0.125a_A a_B \sin(\phi_1(t)) + 0.125\sqrt{2}a_A a_{BL_1} \sin(\phi_2(t)) + 0.25a_A a_{BL_2} \sin(\phi_3(t)) \\ & + 0.125\sqrt{2}a_B a_{BL_1} \cos(\phi_2(t) - \phi_1(t)) + 0.25a_B a_{BL_2} \cos(\phi_3(t) - \phi_1(t)) \\ & + 0.25\sqrt{2}a_{BL_1} a_{BL_2} \cos(\phi_3(t) - \phi_2(t)), \end{aligned} \tag{S8}$$

where E_3 (I_3) represents the field (intensity) of the output signal at the AND port, a_{BL_2} is the amplitude of the bias light at BL_2. $\phi_3(t)$ represents the modulation phase of the signal injected into BL_2. We set the frequency of $\phi_3(t)$ as 2kHz, and that of $\phi_1(t)$ ($\phi_2(t)$) is changed to 1Hz (30Hz).

When Inputs A and B are both turn-off, the BL_1 and BL_2 are turn-on. The output intensity I_3 can be expressed as: $0.25a_{BL_1}^2 + 0.5a_{BL_2}^2 + 0.25\sqrt{2}a_{BL_1}a_{BL_2}\cos(\phi_3(t) - \phi_2(t))$. At the AND port, the output waves from BL_1 and BL_2 need to destructively interfere with each other for realizing the logic function of the AND gate. Thus, we take the signal intensity from the minimum of the curve of Fig. S12(a). Here, the normalized output intensity for the logic signal 0 is 0.03.

When one of Inputs A and B is turn-on and another is turn-off, the output intensity is:

$$I_3 = 0.125a_A^2 + 0.25a_{BL_1}^2 + 0.5a_{BL_2}^2 + 0.125\sqrt{2}a_A a_{BL_1}\sin(\phi_2(t)) + 0.25a_A a_{BL_2}\sin(\phi_3(t))\text{, or}$$

$$I_3 = 0.125a_B^2 + 0.25a_{BL_1}^2 + 0.5a_{BL_2}^2 + 0.125\sqrt{2}a_B a_{BL_1}\cos(\phi_2(t)-\phi_1(t)) + 0.25a_B a_{BL_2}\cos(\phi_3(t)-\phi_1(t)).$$

In this case, the signal from Input A(B) destructively interferes with that from BL_1, and then, the interference signal of Input A and BL_1 destructively interferes with the signal from BL_2. Finally, the output signal arrives at the AND port. Thus, we can take the signal intensity of logic states (AND_01 and AND_10) as the local value of the bottom envelope of the curve close to the minimum of the top envelope. In Figs. S12(c) and S12(e), the logic signal 0 can be obtained, whose value is 0.03.

When both Inputs A and B are turn-on (AND_11), the output intensity is expressed as Eq. (S8). In this case, the signal from Input A constructively interferes with that from Input B, and then, the interference signal of Inputs A and B destructively interferes with the signal from BL_1. Next, the interference signal of Inputs A, B, and BL_1 destructively interferes with the signal from BL_2. Finally, the output signal arrives at the AND port. Thus, the output intensity of the logic signal (AND_11) can be also taken as the local value of the bottom envelope of the curve close to the minimum of the top envelope (the cross point of the top and bottom envelopes), as shown in Fig. S12(g). The signal intensity is about 0.27. The intensity ratio of logic signals 1 and 0 is 9:1 (ER=9.54dB). Such experimental results can be seen in Figs. S12(b), S12(d), S12(e), and S12(h). They are in a good agreement with theoretical results.

In all, according to the above measurement method, we can obtain all logic signals from logic gates in the communication band. All measured results are shown in Figs. 2 and 4 of the main text.

S8. The scheme of the optical phase lock loops (OPLLs).

Here, we propose a scheme to stabilize the phase difference between logic input signals and the bias lights. The optical phase lock loops (OPLLs)[3-5] are such a way to offset the phase fluctuations. As shown in Fig. S13, we use three fiber tunable couplers to split the laser into four paths. The strengths of the input light in every fiber can be flexibly adjusted, so the amplitude ratio of input signals for all logic gates is satisfied.

The phase of logic input A is chosen as the phase standard. The phases of the other three input signals are adjusted by a feedback method in the OPLLs. On the SOI chip, input signal A is split into four paths, and input signals B, BL_1 and BL_2 are split into two paths. They interfere in pairs at

Y branches, and then the interference signals are exported and injected into the OPLLs. The interference optical output signals are converted to electrical signals. After the signal processing in the OPLLs, the corresponding output electrical signals are injected into the fiber phase modulators. So, the phases of inputs B, BL_1 and BL_2 can be fixed. By such a feedback adjustment, the phase differences of input signals can be stable. Thus, all logic gates we designed can be used for a long time.

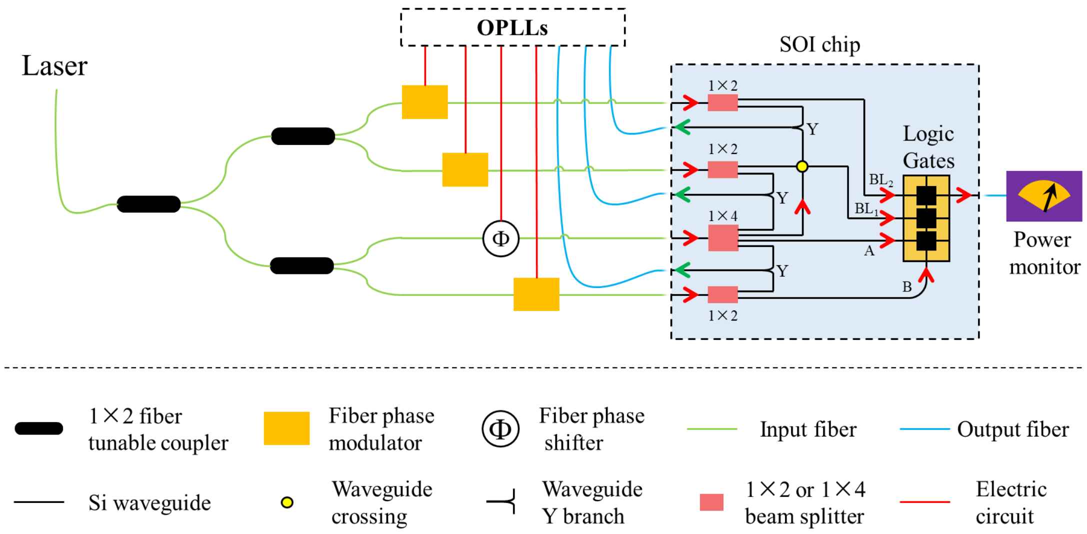

Fig. S13. The schematic diagram of the logic gate measurement by using the optical phase lock loops (OPLLs).

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