Supporting Information for

Achieving low-voltage, high-mobility IGZO transistor through ALD-derived bi-layer channel and hafnia-based gate dielectric stack

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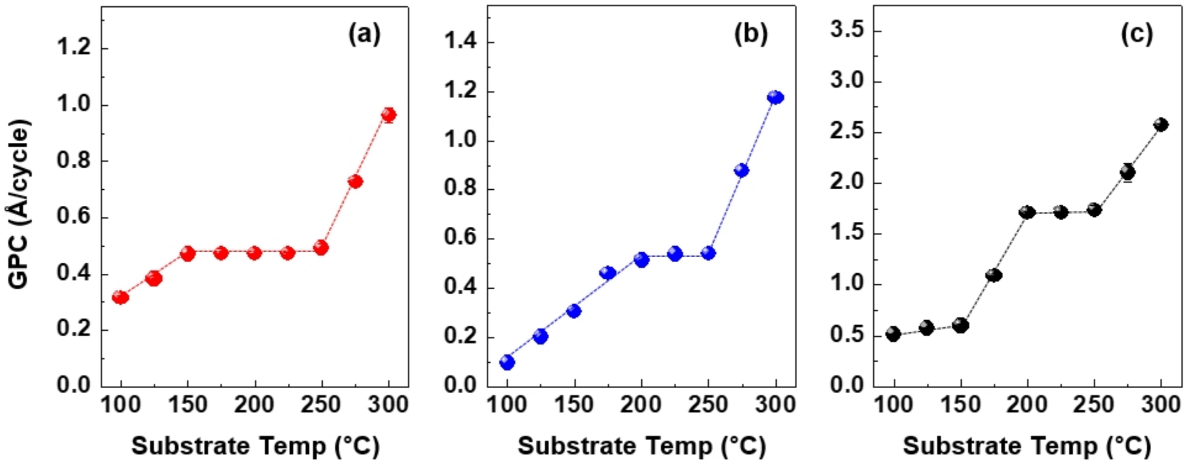

Figure S1. The growh rate per cycle (GPC) of (a) In_2O_3, (b) Ga_2O_3, and (c) ZnO as a function of substrate temperature.

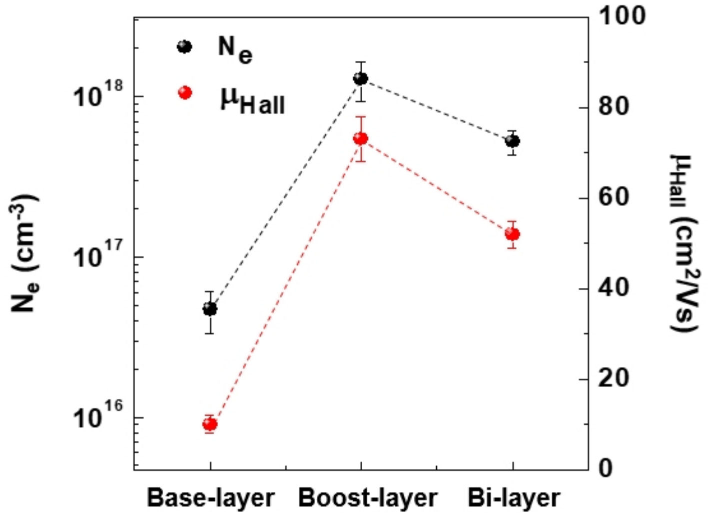

Figure S2. Carrier density (N_e) and Hall mobility (μ_{Hall}) of the ALD-derived base layer, boost layer and bilayer IGZO thin films at T_A = 500 °C on the glass substrate.

Table S1. N_e and μ_{Hall} of the ALD-derived base layer, boost layer and bilayer IGZO thin films at T_A = 500 °C on a glass substrate.

Material	N_e [10^{17}/cm^3]	μ_{Hall} [cm^2/(V s)]
$In_{0.52}Ga_{0.29}Zn_{0.19}O$ (13 nm), Base layer	0.47 ± 0.14	10 ± 2
$In_{0.82}Ga_{0.08}Zn_{0.10}O$ (13 nm), Boost layer	12.81 ± 3.49	73 ± 5
$In_{0.82}Ga_{0.08}Zn_{0.10}O$ (3 nm)/$In_{0.52}Ga_{0.29}Zn_{0.19}O$ (10 nm), Bilayer	5.24 ± 0.91	52 ± 3

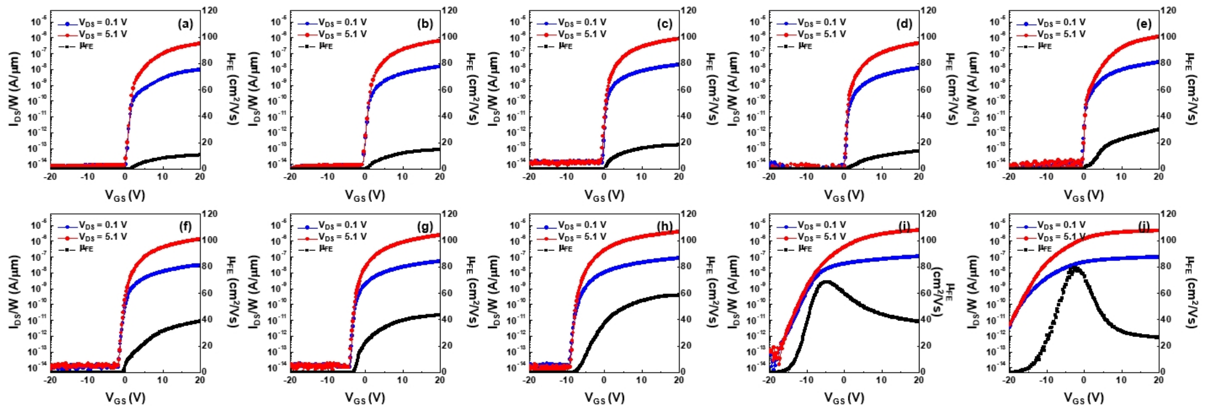

Figure S3. Representative transfer characteristics of ALD-derived IGZO bottom-gate structure TFT with 10 different cation compositions; (a) $In_{0.42}Ga_{0.48}Zn_{0.10}O$, (b) $In_{0.47}Ga_{0.40}Zn_{0.13}O$, (c) $In_{0.52}Ga_{0.29}Zn_{0.19}O$, (d) $In_{0.28}Ga_{0.30}Zn_{0.42}O$, (e) $In_{0.32}Ga_{0.21}Zn_{0.47}O$, (f) $In_{0.42}Ga_{0.48}Zn_{0.10}O$, (g) $In_{0.42}Ga_{0.15}Zn_{0.43}O$, (h) $In_{0.54}Ga_{0.12}Zn_{0.34}O$, (i) $In_{0.67}Ga_{0.10}Zn_{0.22}O$, and (j) $In_{0.82}Ga_{0.08}Zn_{0.10}O$. The devices were fabricated on the SiO_2/Si substrate where the thermal SiO_2 and p^+-Si substrate act as the gate insulator and electrode, respectively.

Table S2. Summary of electrical parameters: μ_{FE}, SS, V_{TH}, and $I_{ON/OFF}$ of the ALD-derived IGZO bottom-gate structure TFTs with 10 different cation compositions.

Channel	Gate Insulator	Cation Composition [In:Ga:Zn, at%]	μ_{FE} [cm^2/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	Corresponding I-V curve in Fig. S2
IGZO	100 nm SiO_2	42:48:10	10.6	0.37	1.58	~ 5.4	(a)
		47:40:13	14.5	0.40	1.05	~ 7.2	(b)
		52:29:19	18.2	0.43	0.57	~ 8.3	(c)
		28:30:42	13.7	0.34	1.35	~ 6.8	(d)
		32:21:47	29.8	0.42	0.92	~ 13.3	(e)
		38:18:44	38.5	0.52	-0.24	~ 17.7	(f)
		42:15:43	43.5	0.60	-2.69	~ 19.5	(g)
		54:12:34	58.6	0.71	-7.32	~ 31.2	(h)
		67:10:22	68.7	1.72	-11.68	~ 3.8	(i)
		82:8:10	79.4	2.63	-16.44	~ 0.01	(j)

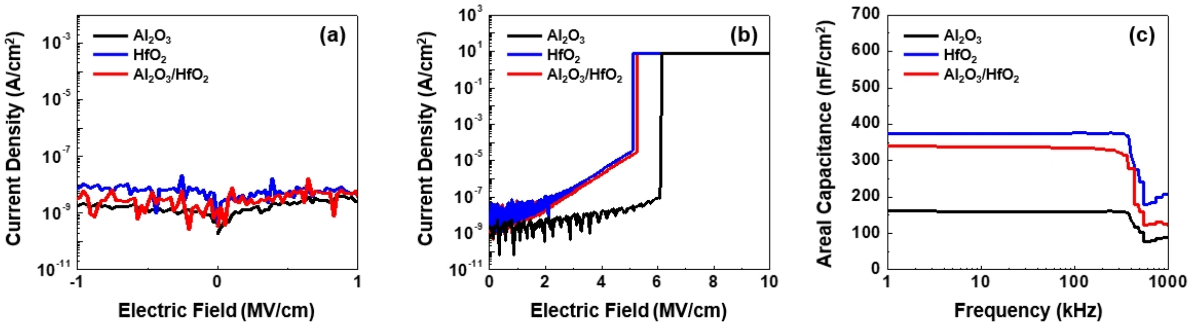

Figure S4. Electrical characteristics of the ALD-derived high-κ dielectric film with an Al_2O_3 (50 nm), HfO_2 (50 nm) and Al_2O_3 (4 nm)/HfO_2 (50 nm) stack: (a) leakage current density (J_g), (b) breakdown field (E_{br}), and (c) frequency-dependent areal capacitance.

The leakage current density (J_g), critical breakdown field (E_{br}) and dielectric constant (κ) of the MIM capacitors with different ALD-derived high-κ dielectric films were measured to evaluate their suitability as a gate insulator for IGZO TFTs. The fabricated MIM capacitors were subjected to PDA at 400°C in a vacuum ambient. **Figure S4a** shows the variations of the leakage current density (J_g) as a function of the applied electric field (E), which was thickness-normalized for better comparison. The capacitor with an Al_2O_3 film had a J_g value of 2.37×10^{-9} A/cm^2 at 1 MV/cm. The J_g value slightly increased to 5.55×10^{-9} A/cm^2 for the capacitor with the HfO_2 film. This phenomenon can be attributed to the existence of the grain boundary defects in HfO_2 as a leakage current path (**Figure S10**). Since the IGZO/HfO_2 interface is known to be inferior to the IGZO/SiO_2 and IGZO/Al_2O_3, the 4-nm-thick Al_2O_3 film was inserted as the interface stabilizer. The capacitor with an Al_2O_3/HfO_2 dielectric stack film had a J_g value of 3.59×10^{-9} A/cm^2, which is an intermediate value between the J_g value of Al_2O_3 and HfO_2 film, indicating that the inserted Al_2O_3 thin film can suppress the leakage current. The E_{br} value, which is defined as the electric field yielding a rapid increase up to the compliance limit, is also shown in **Figure S4b**. The E_{br} value for the different ALD-derived high-κ dielectric films shows the same trend as the J_g value. **Figure S4c** shows the variations in the areal capacitance value as a function of applied frequency for the MIM capacitors with different ALD-derived high-κ dielectric films. The areal capacitance values of the MIM capacitors with the Al_2O_3, HfO_2, and Al_2O_3/HfO_2 dielectric stack films were 175.1, 375.8, and 334.9 nF/cm^2 at 100 kHz, respectively. From these values, the κ values were calculated to be 9, 21, and 20, respectively. It is evident that the Al_2O_3/HfO_2 dielectric stack film with the inserted 4-nm-thick Al_2O_3 thin layer had better J_g and E_{br} values compared to the HfO_2 only capacitor, whereas κ values of 20 were obtained that are comparable to that of the HfO_2 only capacitor.

The J_g, E_{br}, and κ values for different ALD-derived high-κ dielectric films are summarized in **Table S3**.

Table S3. Summary of electrical parameters: leakage current density (J_g), critical breakdown field (E_{br}), areal capacitance (C_{OX}), and κ values of the ALD-derived high-κ dielectric films.

Material	Thickness [nm]	J_g [A/cm^2] (@ 1 MV/cm)	E_{br} [MV/cm]	C_{OX} [nF/cm^2] (@ 100 kHz)	κ (@ 100 kHz)
Al_2O_3	50	2.37×10^{-9}	6.1	159.31	~ 9
HfO_2	50	5.55×10^{-9}	5.1	375.80	~ 21
Al_2O_3/HfO_2	54 (Al_2O_3 = 4, HfO_2 = 50)	3.59×10^{-9}	5.3	334.91	~ 20

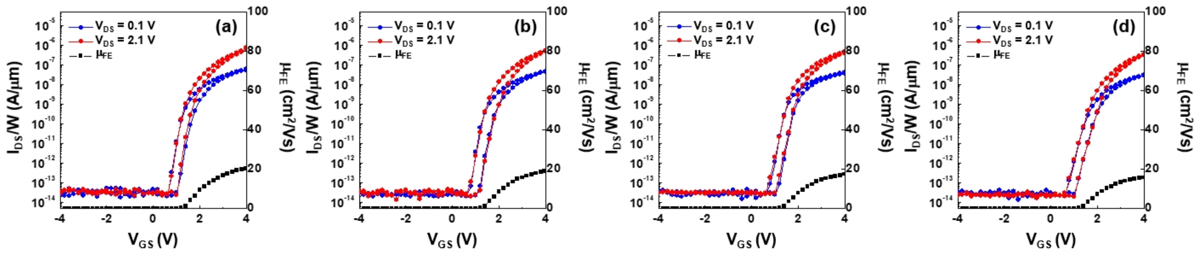

Figure S5. Representative transfer characteristics of the base layer IGZO TFTs with different thicknesses of HfO_2 as a gate insulator; (a) 60, (b) 70, (c) 80, and (d) 90 nm.

Table S4. Summary of electrical parameters: μ_{FE}, SS, V_{TH}, $I_{ON/OFF}$, and $N_{T.max}$ of the base layer IGZO TFTs with different thickness of HfO_2 as a gate insulator.

Channel	Gate Insulator.	C_{OX} [nF/cm^2]	μ_{FE} [cm^2/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.52}Ga_{0.29}Zn_{0.19}O$ (Base layer)	60 nm HfO_2	313	20.5 ± 0.38	0.15 ± 0.01	1.27 ± 0.25	~ 2.2	3.96×10^{18}
	70 nm HfO_2	269	18.9 ± 0.45	0.17 ± 0.02	1.38 ± 0.31	~ 1.5	3.97×10^{18}
	80 nm HfO_2	234	17.4 ± 0.56	0.20 ± 0.02	1.47 ± 0.29	~ 1.4	3.96×10^{18}
	90 nm HfO_2	208	15.6 ± 0.31	0.24 ± 0.01	1.61 ± 0.21	~ 1.2	4.00×10^{18}

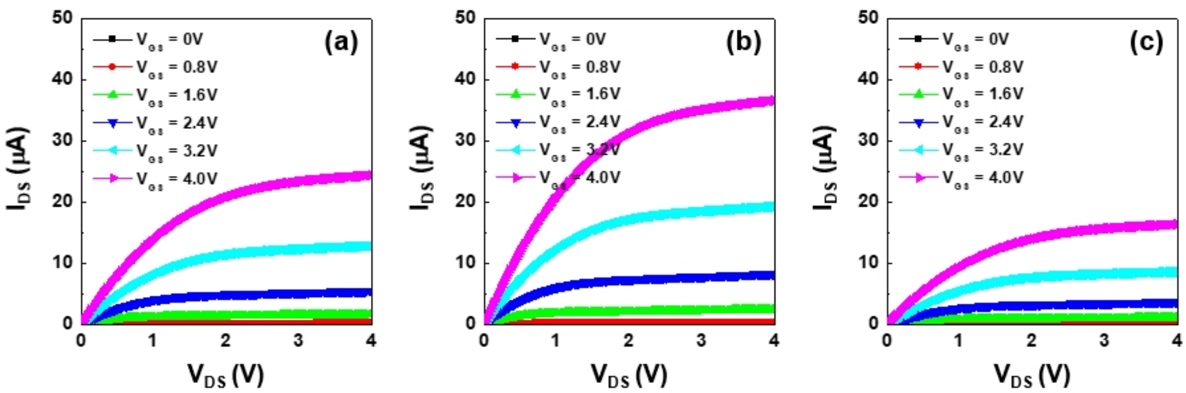

Figure S6. Corresponding output characteristics of the base layer IGZO TFT with different gate insulators of (a) HfO_2 (100 nm), (b) HfO_2 (50 nm), and (c) Al_2O_3 (50 nm).

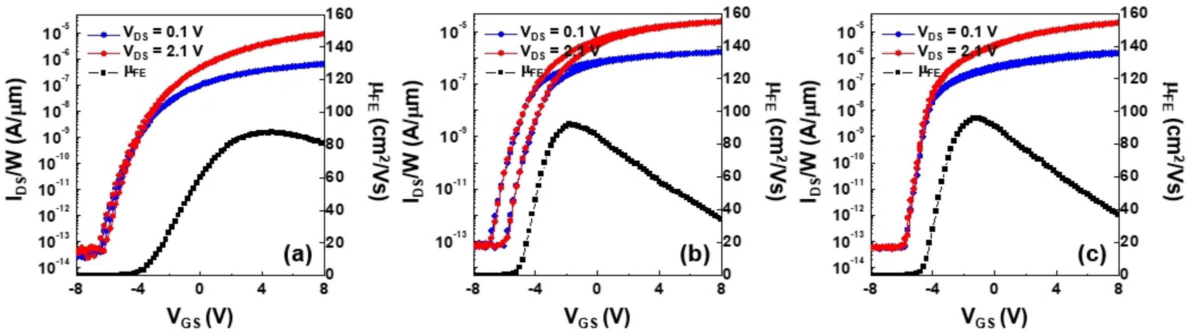

Figure S7. Representative transfer characteristics of the boost layer IGZO TFTs with different gate insulators of (a) Al_2O_3 (50 nm), (b) HfO_2 (50 nm), and (c) Al_2O_3 (4 nm)/ HfO_2 (50 nm).

Table S5. Summary of electrical parameters: μ_{FE}, SS, V_{TH}, $I_{ON/OFF}$, and $N_{T.max}$ for the boost layer IGZO TFTs with different gate insulators of (a) Al_2O_3 (50-nm), (b) HfO_2 (50-nm), and (c) Al_2O_3 (4-nm)/ HfO_2 (50-nm).

Channel	Gate Insulator	C_{OX} [nF/cm^2]	μ_{FE} [cm^2/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.82}Ga_{0.08}Zn_{0.10}O$ (Boost layer)	50 nm Al_2O_3	159	87.8 ± 0.73	0.63 ± 0.02	-4.36 ± 0.22	~ 17.8	8.08 × 10^{18}
	50 nm HfO_2	376	92.3 ± 0.73	0.36 ± 0.03	-5.58 ± 0.28	~ 35.0	10.9 × 10^{18}
	54 nm Al_2O_3/HfO_2	335	95.7 ± 0.66	0.30 ± 0.02	-4.84 ± 0.14	~ 37.4	8.10 × 10^{18}

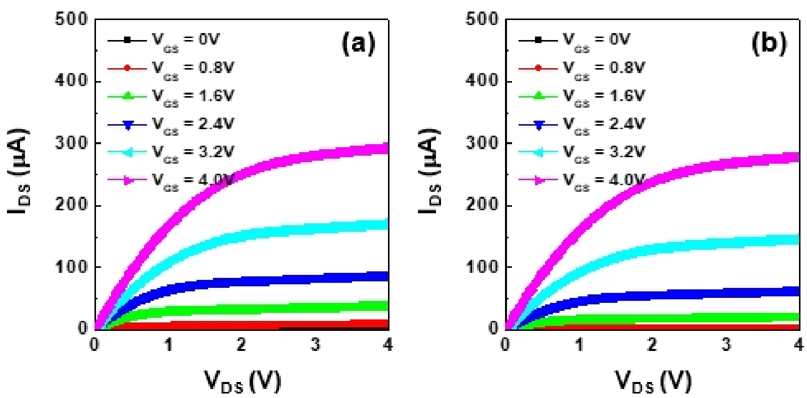

Figure S8. Corresponding output characteristics of the bilayer IGZO TFTs with different gate insulators of (a) HfO_2 (50 nm) and (b) Al_2O_3 (4 nm)/ HfO_2 (50 nm).

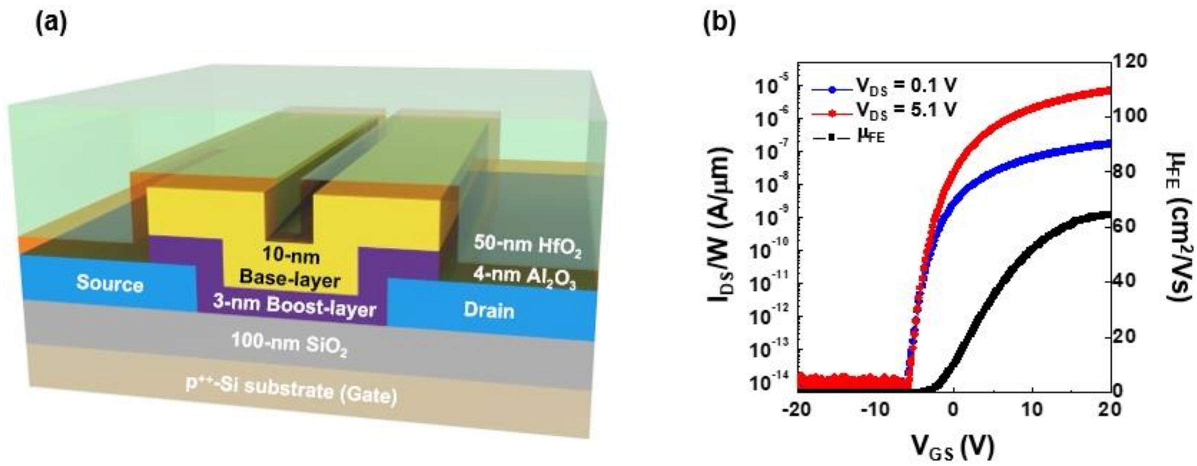

Figure S9. (a) Schematic diagram of the bottom gate structure bilayer IGZO TFT with gate insulator of SiO_2 (100 nm) and (b) corresponding transfer characteristic. The device went through PDA at 500°C for 1h in air ambient.

Table S6. Summary of electrical parameters: μ_{FE}, SS, and V_{TH}, and $I_{ON/OFF}$ of the bilayer IGZO TFT with gate insulator of SiO_2 (100 nm) through PDA at 500°C for 1h in air ambient.

Channel	Gate Insulator	C_{OX} [nF/cm^2]	μ_{FE} [cm^2/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.60}Ga_{0.21}Zn_{0.19}O$ (Bilayer)	100 nm SiO_2	34.5	64.6 ± 1.21	0.79 ± 0.01	-3.80 ± 1.02	~ 22.1	2.21 × 10^{18}

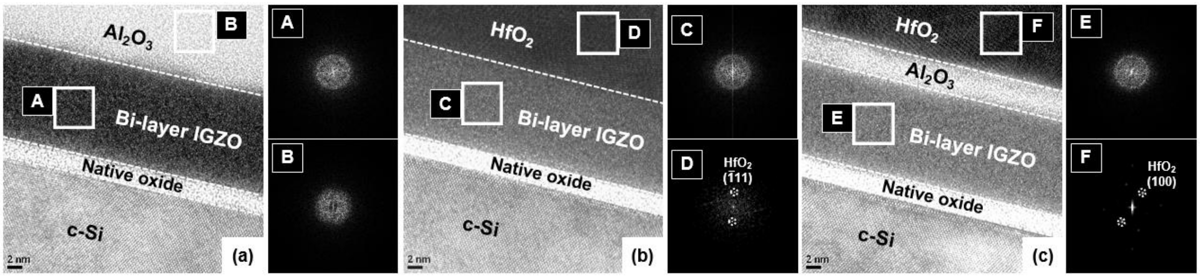

Figure S10. Cross-sectional HRTEM images of (a) Al_2O_3/bilayer IGZO, (b) HfO_2/bilayer IGZO and (c) HfO_2/Al_2O_3/bilayer IGZO. Fast Fourier transform (FFT) patterns of the selected area in IGZO film are inserted in the given TEM images.

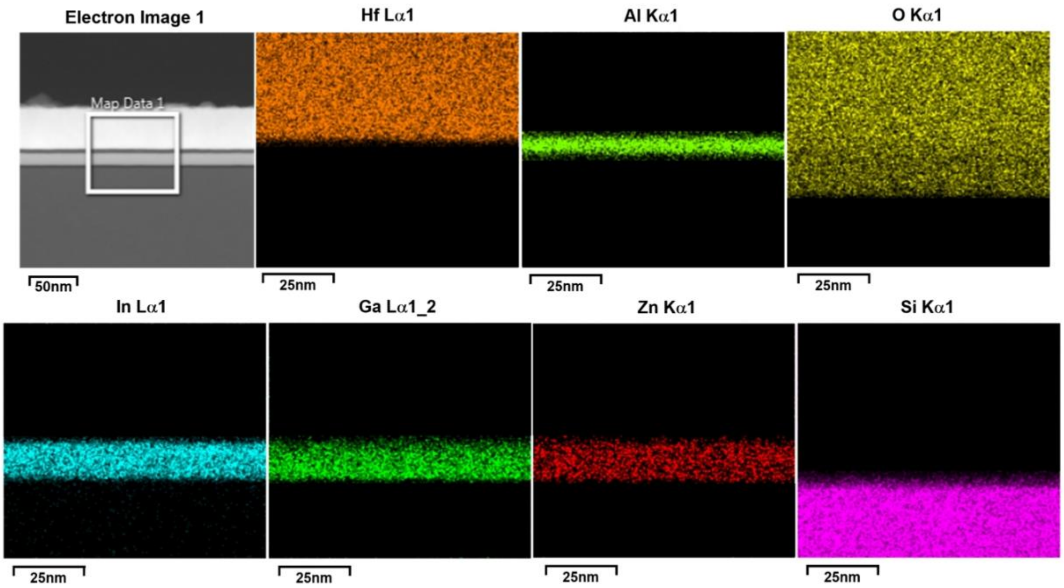

Figure S11. Elemental distributions of the HfO_2/Al_2O_3/bilayer IGZO stack by energy dispersive spectroscopy (EDS) mapping.

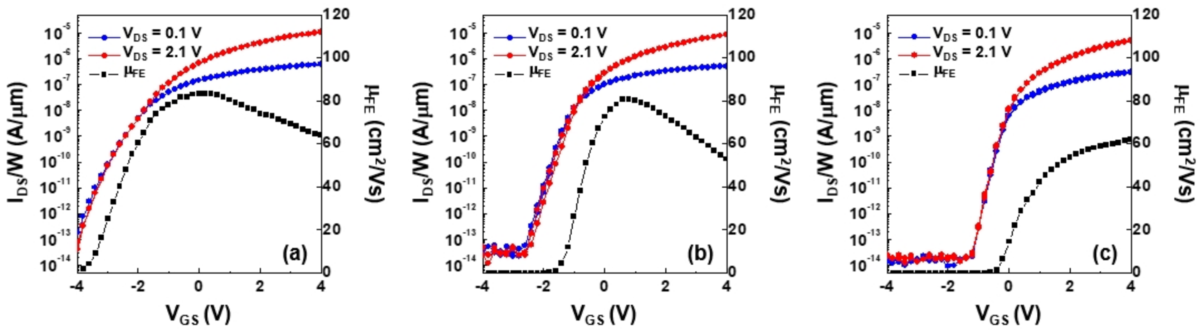

Figure S12. Representative transfer characteristics of the bilayer IGZO TFT with gate insulator of Al_2O_3 (4 nm)/ HfO_2 (50 nm) stack varying PDA conditions; PDA at (a) 300°C, (b) 400°C for 1h in air, and (c) 400°C for 1h in O_2 ambient.

Table S7. Summary of electrical parameters: μ_{FE}, SS, V_{TH}, and $I_{ON/OFF}$, and $N_{T,max}$ of the bilayer IGZO TFTs with gate insulator of Al_2O_3 (4 nm)/HfO_2 (50 nm) with varying PDA conditions.

Channel	Gate Insulator	PDA Condition	μ_{FE} [cm²/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.60}Ga_{0.21}Zn_{0.19}O$ (Bilayer)	54 nm Al_2O_3/HfO_2	300°C 1h in air	83.5 ± 1.03	0.46 ± 0.02	-2.64 ± 0.67	~ 26.6	12.4 × 10^{18}
		400°C 1h in air	80.8 ± 0.86	0.30 ± 0.02	-1.49 ± 0.42	~ 24.8	8.10 × 10^{18}
		400°C 1h in O_2	61.9 ± 1.25	0.20 ± 0.01	-0.38 ± 0.14	~ 21.7	5.40 × 10^{18}

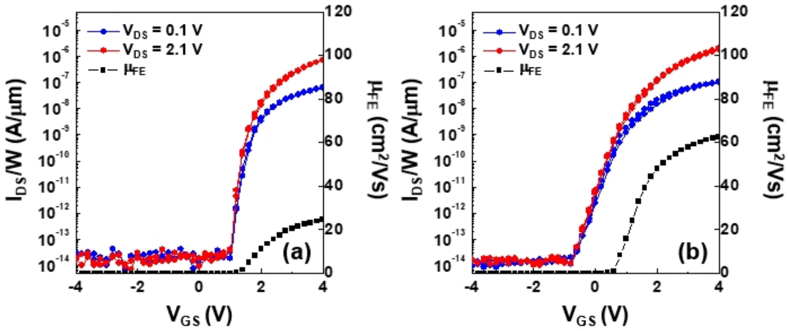

Figure S13. Representative transfer characteristics of the (a) base layer IGZO TFTs with the Al_2O_3 (4 nm)/HfO_2 (50 nm) gate insulator and (b) bilayer IGZO TFTs with a Al_2O_3 (50 nm) gate insulator.

Table S8. Summary of electrical parameters: μ_{FE}, SS, V_{TH}, $I_{ON/OFF}$, and $N_{T.max}$ of the base layer IGZO TFTs with the Al_2O_3 (4 nm)/HfO_2 (50 nm) and bilayer IGZO TFTs with Al_2O_3 (50 nm) gate insulator.

Channel	Gate Insulator	C_{OX} [nF/cm^2]	μ_{FE} [cm^2/(V s)]	SS [V/decade]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.52}Ga_{0.29}Zn_{0.19}O$ (Base layer)	54 nm Al_2O_3/HfO_2	335	24.5 ± 0.58	0.10 ± 0.01	1.52 ± 0.27	~ 3.8	2.70 × 10^{18}
$In_{0.60}Ga_{0.21}Zn_{0.19}O$ (Bilayer)	50 nm Al_2O_3	159	62.7 ± 0.81	0.27 ± 0.02	0.74 ± 0.13	~ 11.3	3.46 × 10^{18}

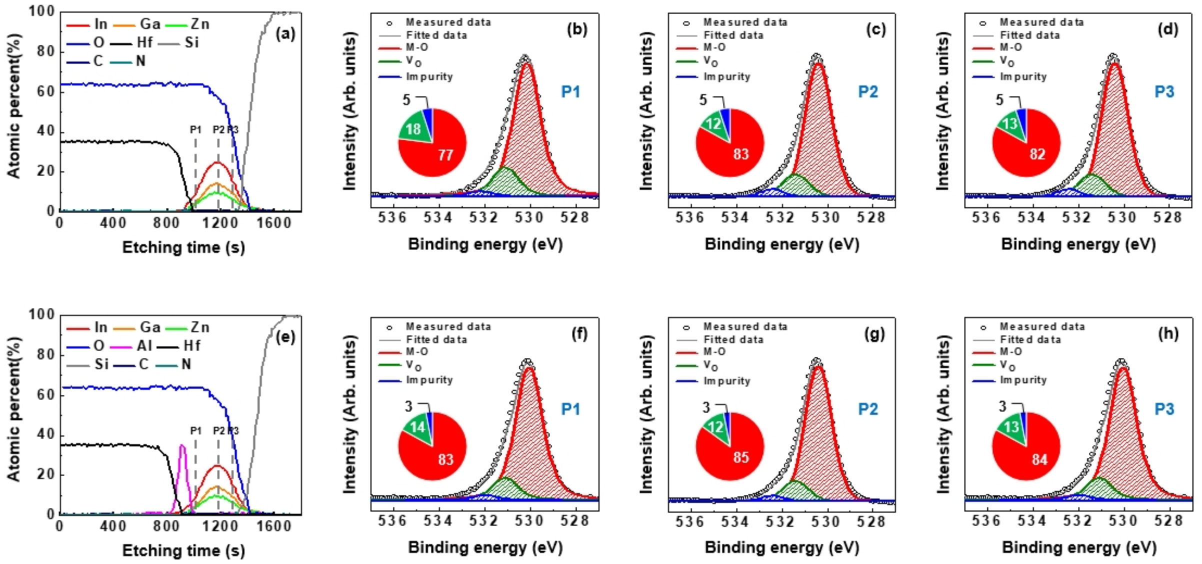

Figure S14. XPS depth profile of the base layer IGZO film with different high-κ dielectric stacks and O *1s* spectra: (a) XPS depth profile of the HfO_2/base layer IGZO stack. O *1s* spectra taken from (b) P1, (c) P2, and (d) P3 position for the HfO_2/base layer IGZO stack. (e) XPS depth profile of the HfO_2/Al_2O_3/base layer IGZO stack. O *1s* spectra from (f) P1, (g) P2, and (h) P3 positions for the HfO_2/Al_2O_3/base layer IGZO stack.

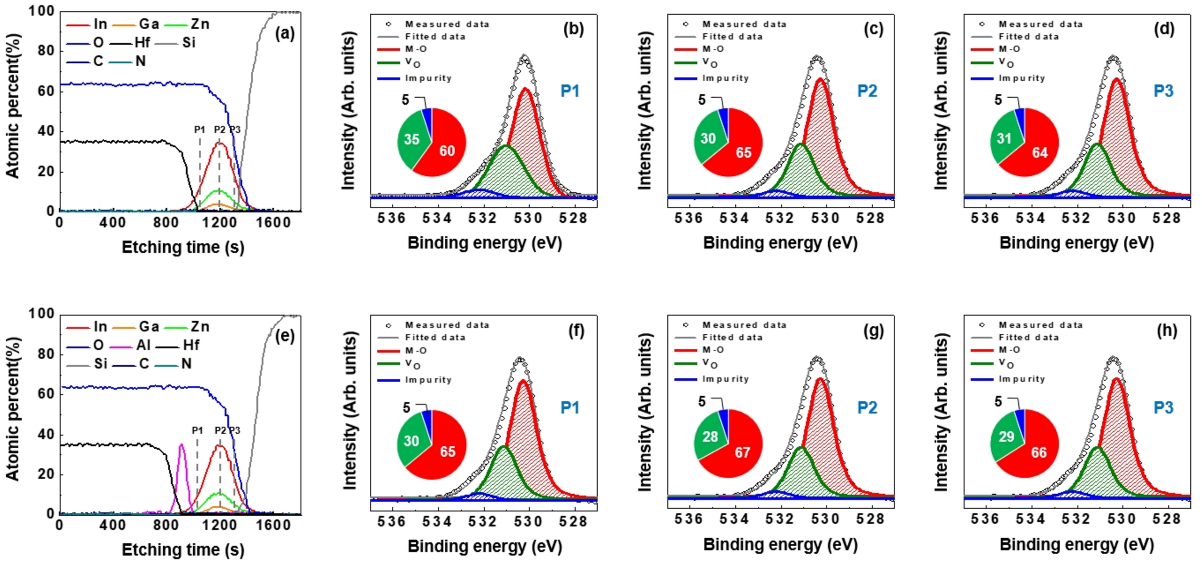

Figure S15. XPS depth profile of the boost layer IGZO film with different high-κ dielectric stacks and O *1s* spectra: (a) XPS depth profile of the HfO_2/boost layer IGZO stack. O *1s* spectra taken from (b) P1, (c) P2, and (d) P3 position for the HfO_2/boost layer IGZO stack. (e) XPS depth profile of the HfO_2/Al_2O_3/boost layer IGZO stack. O *1s* spectra from (f) P1, (g) P2, and (h) P3 position for the HfO_2/Al_2O_3/boost layer IGZO stack.

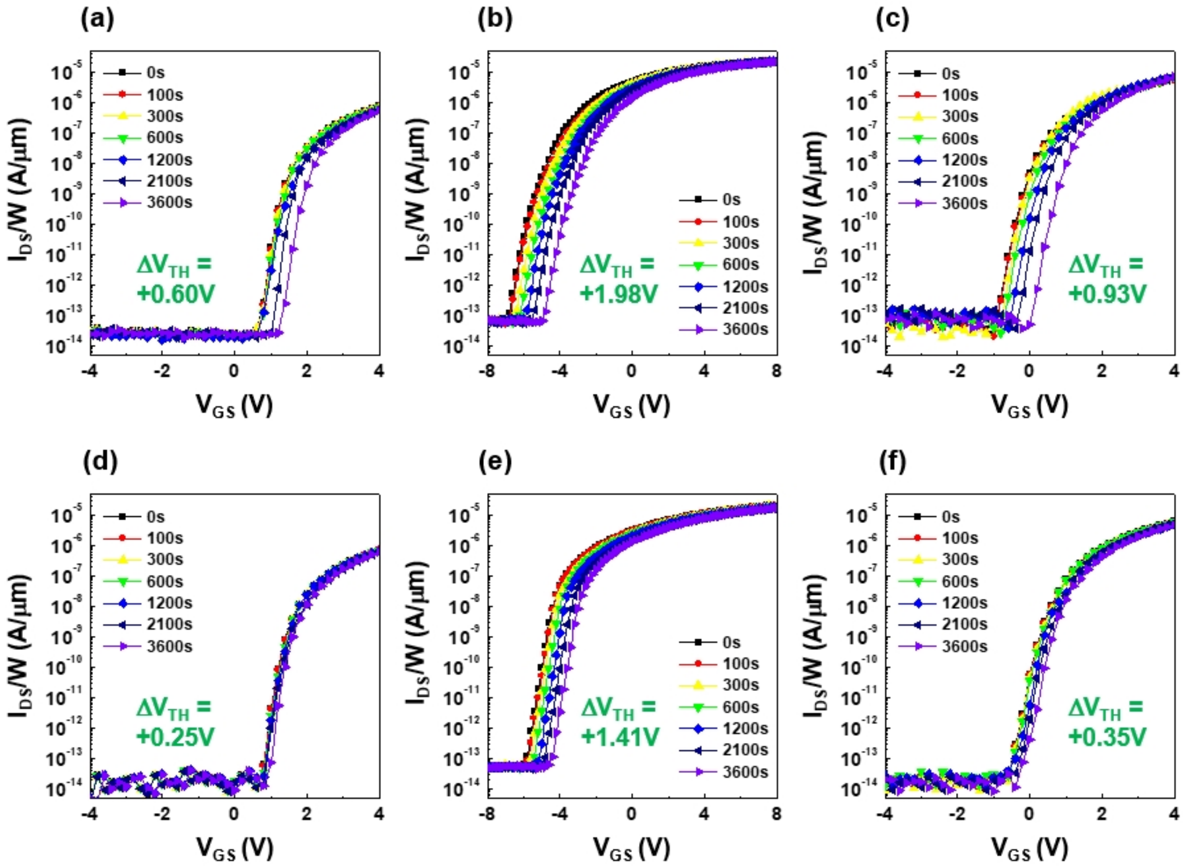

Figure S16. Evolution of time-dependent transfer characteristics of ALD-derived IGZO TFTs with various gate insulator; (a,d) base layer IGZO TFTs with (a) HfO_2 and (d) Al_2O_3/HfO_2, (b,e) boost layer IGZO TFTs with (b) HfO_2 and (e) Al_2O_3/HfO_2, (c,f) bilayer IGZO TFTs with (c) HfO_2 and (f) Al_2O_3/HfO_2. The stress conditions are $V_{GS} = V_{TH} + 10V$ at 60°C.

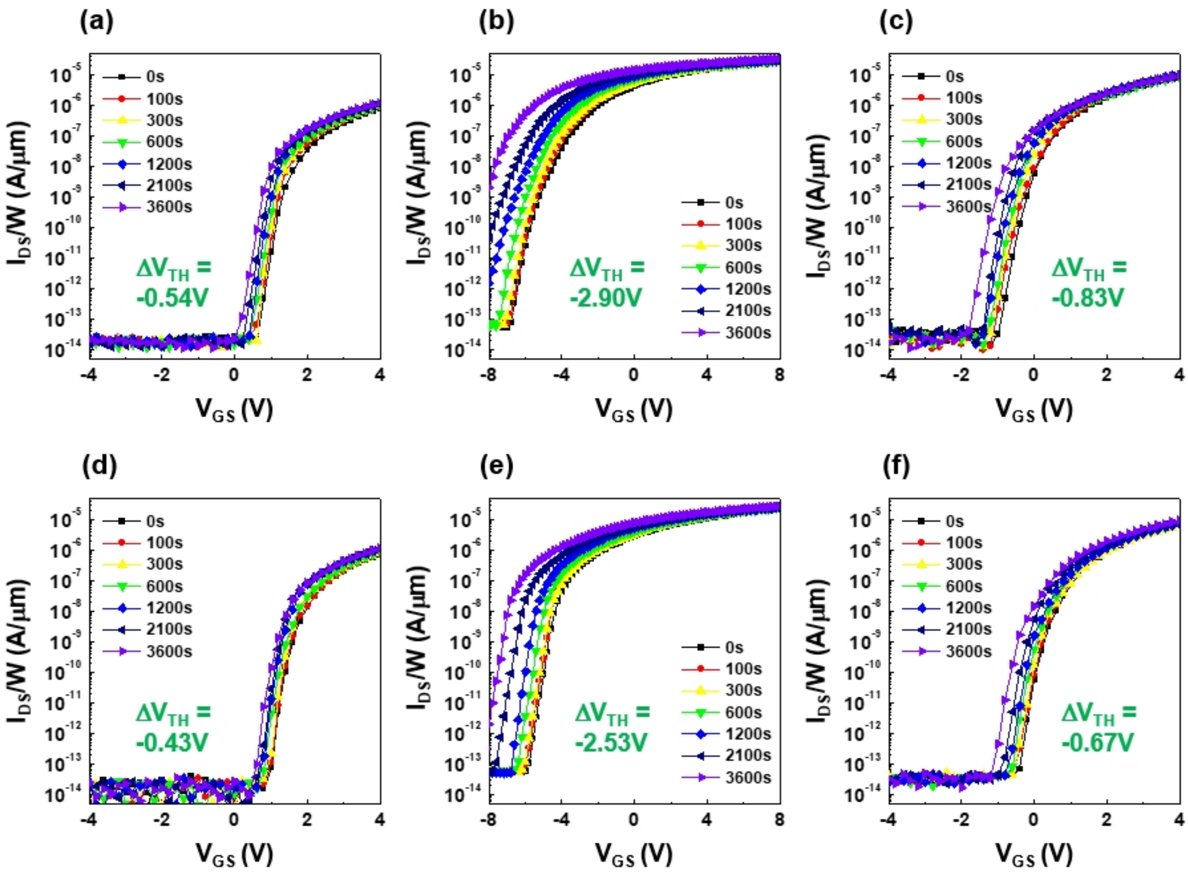

Figure S17. Evolution of time-dependent transfer characteristics of ALD-derived IGZO TFTs with various gate insulator; (a,d) base layer IGZO TFTs with (a) HfO_2 and (d) Al_2O_3/HfO_2, (b,e) boost layer IGZO TFTs with (b) HfO_2 and (e) Al_2O_3/HfO_2, (c,f) bilayer IGZO TFTs with (c) HfO_2 and (f) Al_2O_3/HfO_2. The stress conditions are $V_{GS} = V_{TH}$-10V and a light intensity of 0.066mW/cm^2 (light source with a wavelength of ~533 nm with full-width at half maximum of approximately ±10 nm).

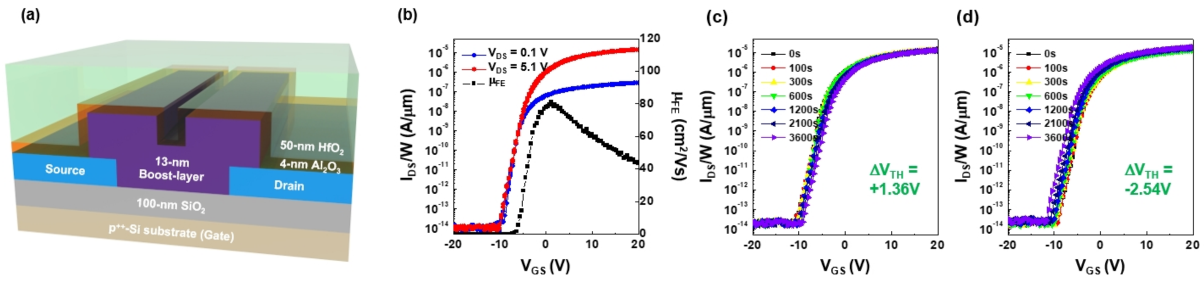

Figure S18. (a) Schematic diagram of the bottom gate structure boost layer IGZO TFT with SiO_2 (100 nm) gate insulator and (b) corresponding transfer characteristics. (c,d) Evolution of time-dependent transfer characteristics of bottom gate structure boost layer IGZO TFT with SiO_2 (100 nm) gate insulator under (c) PBTS and (b) NBIS conditions for 3,600 sec.

Table S9. Summary of electrical parameters: μ_{FE}, SS, and V_{TH}, and $I_{ON/OFF}$ of the boost layer IGZO TFT with SiO_2 (100 nm) gate insulator through PDA at 500°C for 1h in air ambient.

Channel	Gate Insulator	C_{OX} [nF/cm^2]	μ_{FE} [cm^2/(V s)]	SS [V/dec]	V_{TH} [V]	$I_{ON/OFF}$ [× 10^7]	$N_{T,max}$ [cm^{-3}ev^{-1}]
$In_{0.82}Ga_{0.08}Zn_{0.10}O$ (Boost layer)	100 nm SiO_2	34.5	81.3 ± 4.04	0.97 ± 0.02	-6.08 ± 2.16	~ 29.4	2.70 × 10^{18}

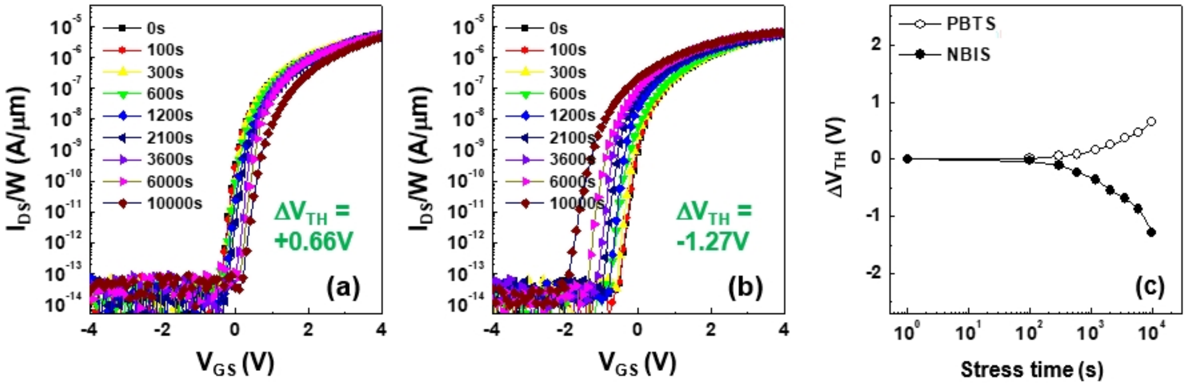

Figure S19. Variations in the transfer characteristics for the bilayer IGZO TFT with gate insulator of Al_2O_3 (4 nm)/HfO_2 (50 nm) stack under (a) PBTS and (b) NBIS conditions for 10,000 sec. (c) Corresponding V_{TH} shift as a function of the stress time.

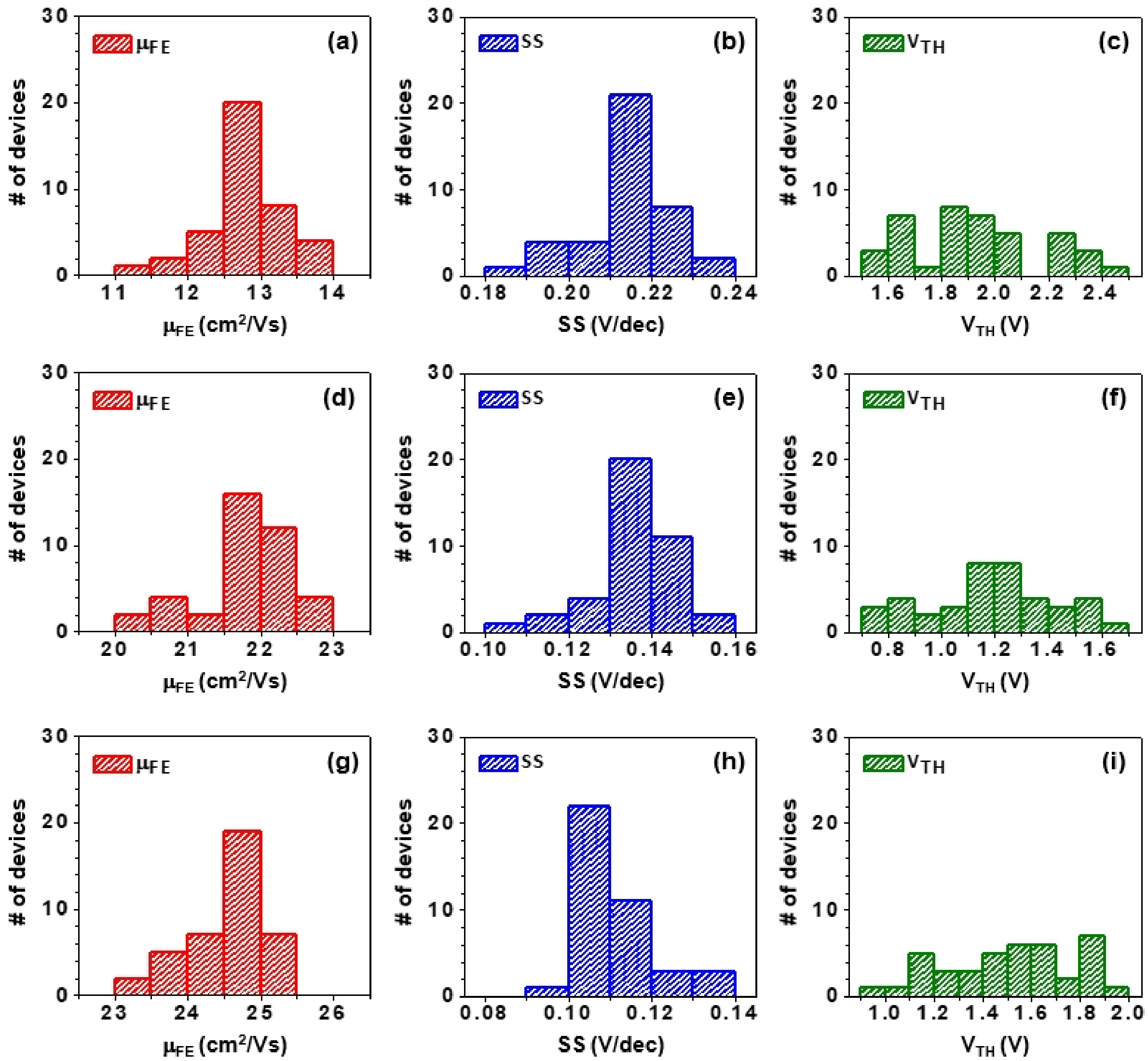

Figure S20. Distribution of (a, d, g) μ_{FE}, (b, e, h) SS, and (c, f, i) V_{TH} for the base layer IGZO TFTs with (a-c) Al_2O_3, (e-f) HfO_2, and (g-i) Al_2O_3/HfO_2 gate insulator. These data were for 40 different transistors.

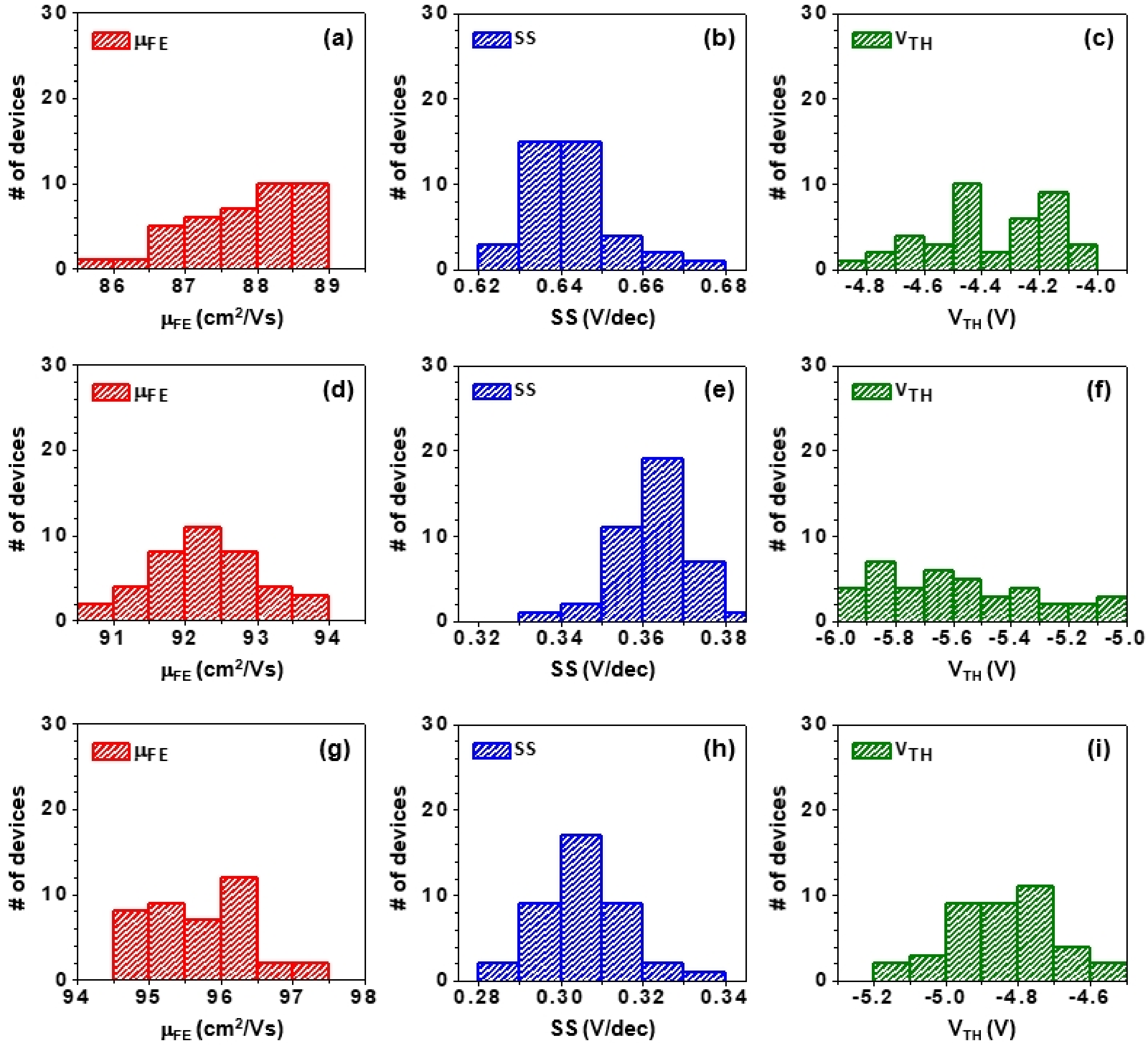

Figure S21. Distribution of (a, d, g) μ_{FE}, (b, e, h) *SS*, and (c, f, i) V_{TH} for the boost layer IGZO TFTs with (a-c) Al_2O_3, (e-f) HfO_2, and (g-i) Al_2O_3/HfO_2 gate insulator. These data were for 40 different transistors.

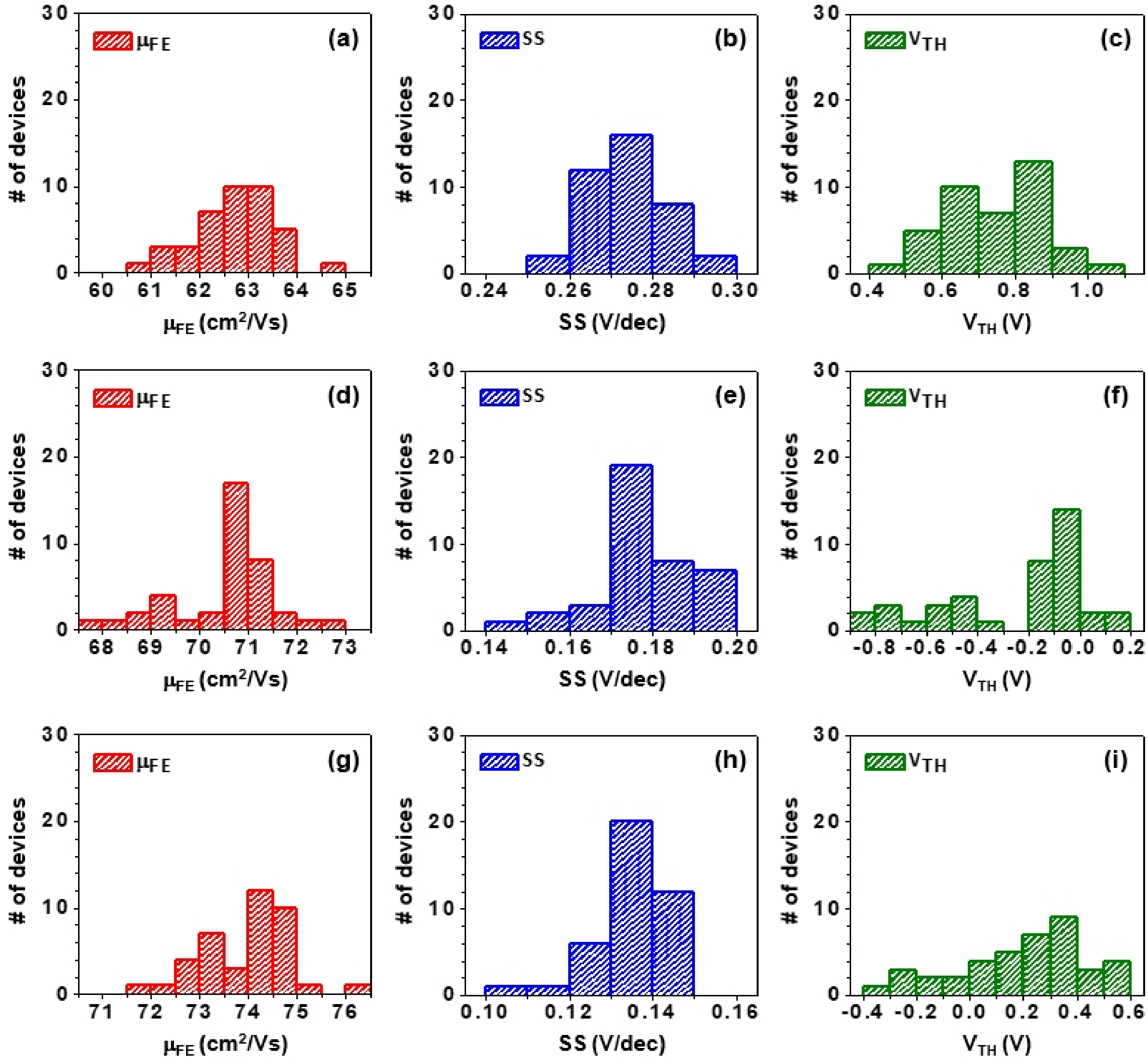

Figure S22. Distribution of (a, d, g) μ_{FE}, (b, e, h) *SS*, and (c, f, i) V_{TH} for the bilayer IGZO TFTs with (a-c) Al_2O_3, (e-f) HfO_2, and (g-i) Al_2O_3/HfO_2 gate insulator. These data were for 40 different transistors.