Supporting Information
Tellurium Nanowire Gate–All–Around MOSFETs for Sub–5 nm Applications

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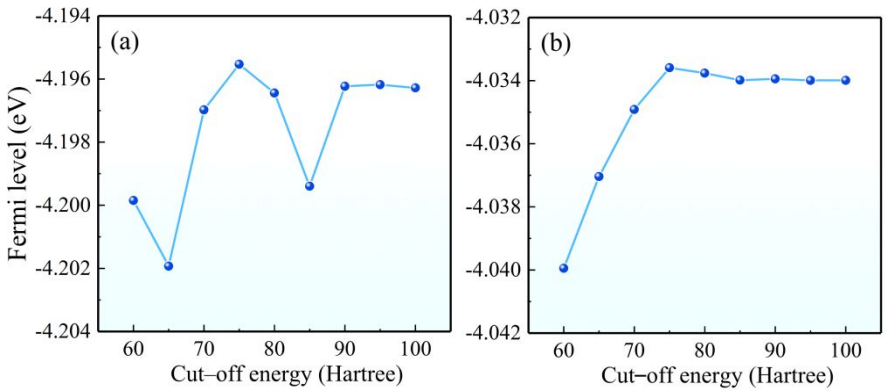

Figure S1. The convergence test of cutoff energy for (a) 1Te GAA MOSFETs and (b) 3Te GAA MOSFETs.

In terms of device transport, the Fermi level (ε_F) is an exponential term in the formula (1) to calculate the drain current. Hence, the accuracy of ε_F is very important for the drain current, so ε_F error less than 0.001 eV is used as convergence criteria of 1Te and 3Te gate–all–around (GAA) MOSFETs in Figure S1. Based on the results in Figure S1, the grid mesh cutoff energy for the Te GAA MOSFETs is set to 75 Hartree.[1]

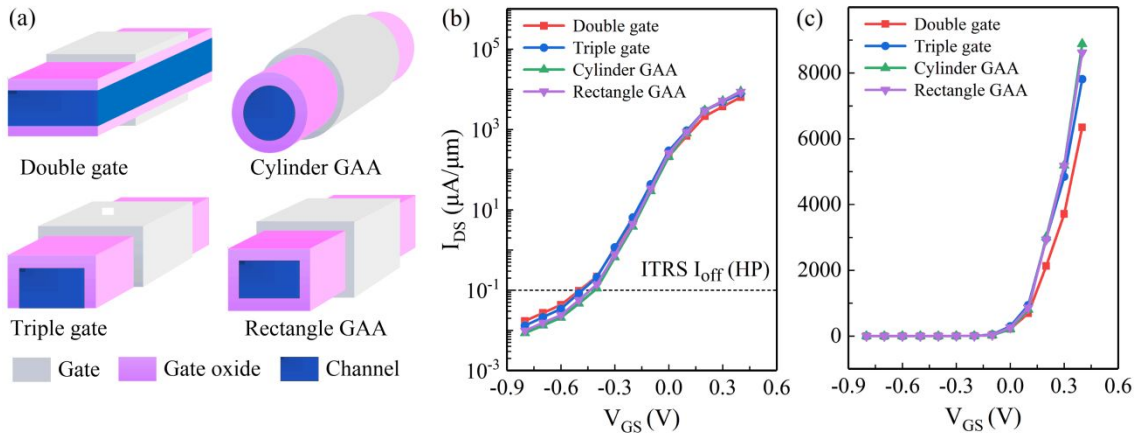

Figure S2. (a) Schematic structures of the 5 nm 1Te MOSFETs with different gate configurations, including double gate, triple gate, cylinder GAA and rectangle GAA. (b) semi–log and (c) linear transfer *I–V* curves.

Table S1. I_{on} and SS of 1Te MOSFETs with different configurations, obtained from the *I–V* curves in Figure S2.

MOSFETs configuration	I_{on} (μA/μm)	SS (μA/μm)
Double gate	1152	142
Triple gate	1914	137
Cylinder GAA	3215	122
Rectangle GAA	3374	125

In Figure 2, 1Te μ_h exhibits the largest variation with the changing of Fermi energy which is in consistent with the largest scattering rate fluctuation in Figure S3. On the contrary, other μ of Te NWs feature small variations corresponding to relative small

scattering rate fluctuations. Therefore, the μ in Figure 2 varies inversely with scattering rates in Figure S3.

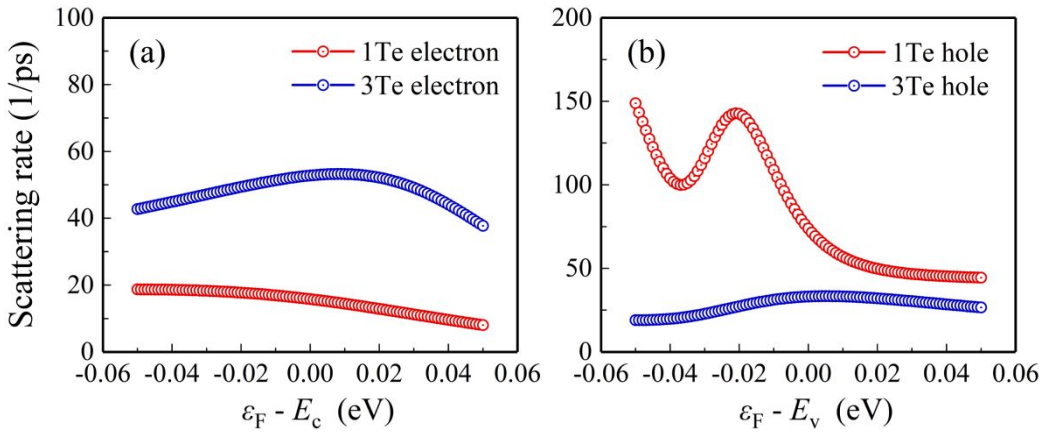

Figure S3. Te NWs scattering rates as a function of Fermi energy for (a) electron and (b) hole obtained by the electron-phonon coupling calculation. The temperature is at 300 K. The E_c and E_v represent the conduction band minimum and valance band maximum energies, respectively.

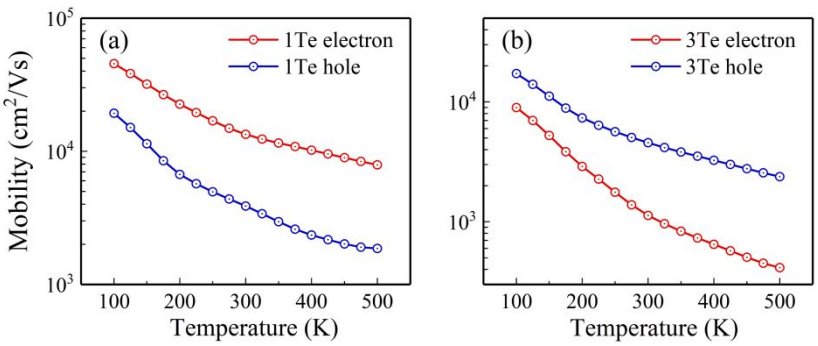

Figure S4. Te NWs carrier mobility as a function of temperature for (a) 1Te NW and (b) 3Te NW obtained by the electron-phonon coupling calculation.

The transfer *I–V* curves of 5 nm L_g 1Te double gate, triple gate, cylinder GAA and rectangle GAA MOSFETs are compared in the Figure S2. The detailed data of I_{on} and SS extracted from different configuration MOSFETs are shown in Table S1. It can be seen clearly that the performance of GAA MOSFETs is superior to the multi–gate

MOSFETs. The I_{on} and SS in Table S1 of rectangle GAA and cylinder GAA MOSFETs are very close, and in this paper we only focus on the performance of rectangle GAA Te MOSFETs.

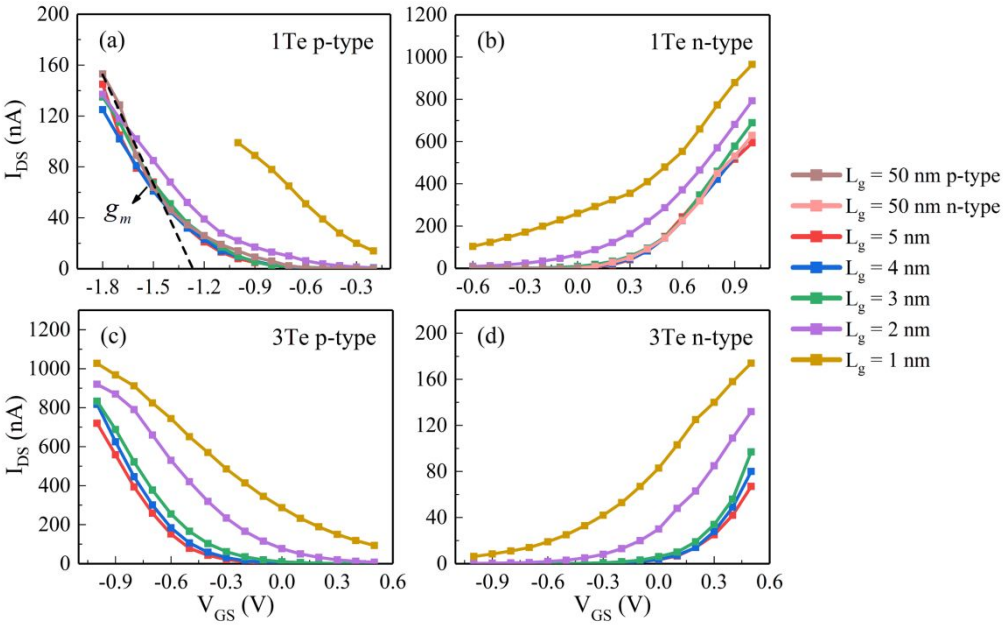

Figure S5. The transfer *I–V* curves of (a,b) 1Te and (c,d) 3Te GAA MOSFETs with p–type and n–type doping. The black dash line is an example to define the g_m. The legend in the right part represents the gate length and doping type.

Table S2. Gate capacitance and transconductance of 1Te and 3Te GAA MOSFETs with p–type and n–type doping.

	L_g (nm)	1	2	3	4	5	50
1Te n–type	C_g (F)	3.7×10^{-13}	2.6×10^{-13}	2.1×10^{-13}	1.7×10^{-13}	1.5×10^{-13}	6.0×10^{-13}
	g_m (S)	3.2×10^{-7}	5.1×10^{-7}	8.9×10^{-7}	9.9×10^{-7}	9.6×10^{-7}	1.0×10^{-6}
1Te p–type	C_g (F)	2.8×10^{-13}	3.2×10^{-13}	2.6×10^{-13}	2.7×10^{-13}	2.2×10^{-13}	1.7×10^{-13}
	g_m (S)	2.2×10^{-7}	1.3×10^{-7}	1.4×10^{-7}	2.3×10^{-7}	2.5×10^{-7}	4.0×10^{-7}
3Te p–type	C_g (F)	6.8×10^{-13}	4.6×10^{-13}	3.5×10^{-13}	3.3×10^{-13}	3.0×10^{-13}	–
	g_m (S)	8.5×10^{-6}	1.3×10^{-6}	1.6×10^{-6}	1.9×10^{-6}	1.6×10^{-6}	–
3Te n–	C_g (F)	2.6×10^{-13}	4.5×10^{-13}	3.7×10^{-13}	3.2×10^{-13}	3.0×10^{-13}	–

type	g_m (S)	1.9×10^{-7}	2.0×10^{-7}	3.1×10^{-7}	5.0×10^{-7}	3.4×10^{-7}	–

The transfer *I–V* curves of 1Te and 3Te GAA MOSFETs with 0.01V V_{dd} are shown in Figure S5 and the detailed data of gate capacitance (C_g) and transconductance (g_m) are shown in Table S2. The change of C_g and g_m remains at an order of magnitude, so the carrier mobility μ mainly depends on the device gate length.

Table S3. ITRS HP and LP requirements. The first line represents the geometry parameters. The third and fifth lines represent ITRS goals for HP and LP devices, respectively

Device parameters	L_g (nm)	EOT (nm)	V_{dd} (V)	–	–
ITRS HP/LP 2028	5.1	0.41	0.64	–	–
HP goals	I_{off} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
ITRS HP 2028	0.1	9×10^3	0.60	0.423	0.240
Lp goals	I_{off} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
ITRS LP 2028	5×10^{-5}	5.9×10^6	0.69	1.493	0.280

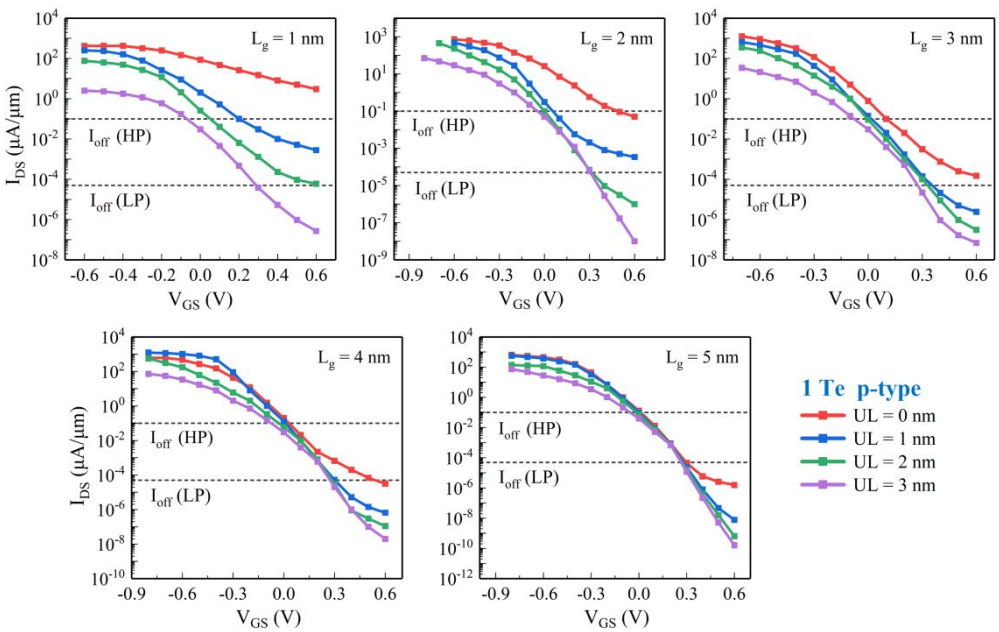

Figure S6. The transfer *I–V* curves of p–type 1Te GAA MOSFETs. The dash lines are the HP and LP threshold I_{off} set to 0.1 μA/μm and 5×10^{-5} μA/μm, respectively, according to the ITRS standards.

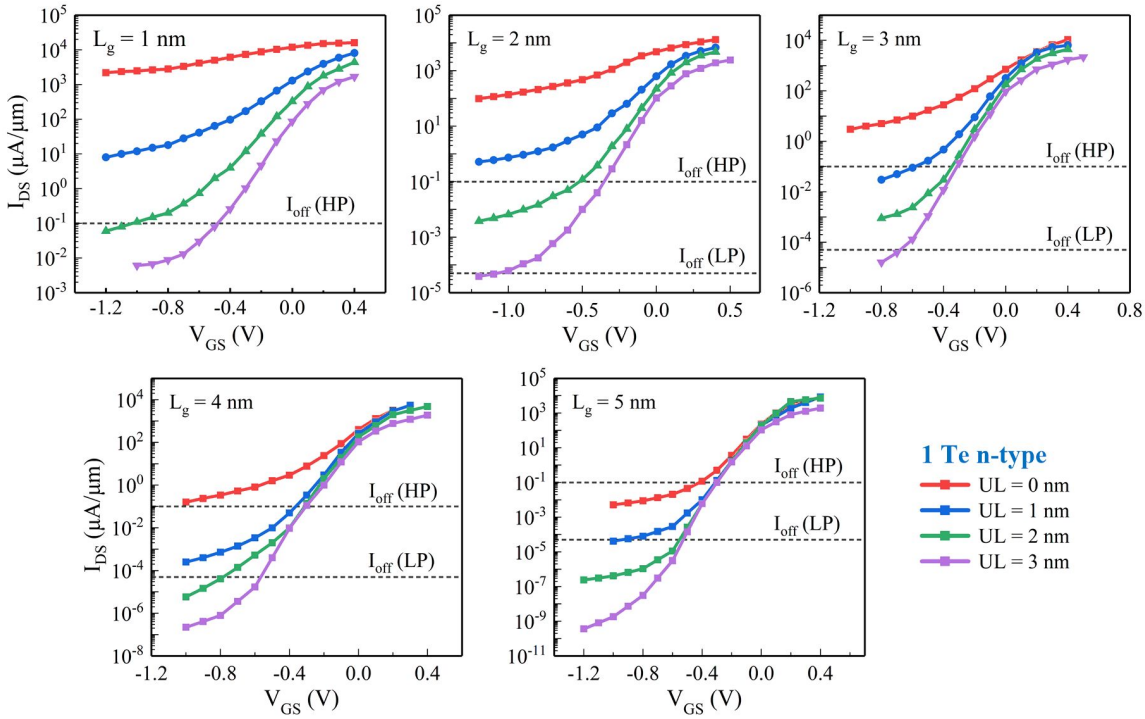

Figure S7. The transfer *I–V* curves of n–type 1Te GAA MOSFETs. The dash lines are the HP and LP threshold I_{off} set to 0.1 μA/μm and 5×10^{-5} μA/μm, respectively, according to the ITRS standards.

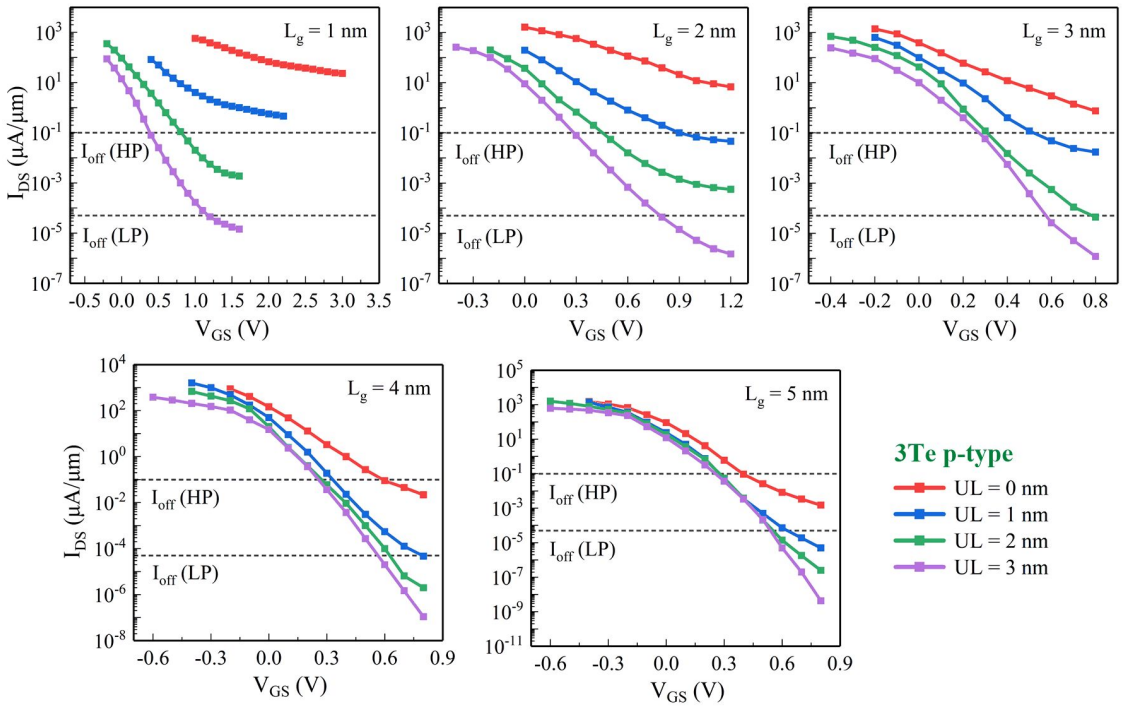

Figure S8. The transfer *I–V* curves of p–type 3Te GAA MOSFETs. The dash lines are the HP and LP threshold I_{off} set to 0.1 μA/μm and 5×10^{-5} μA/μm, respectively, according to the ITRS standards.

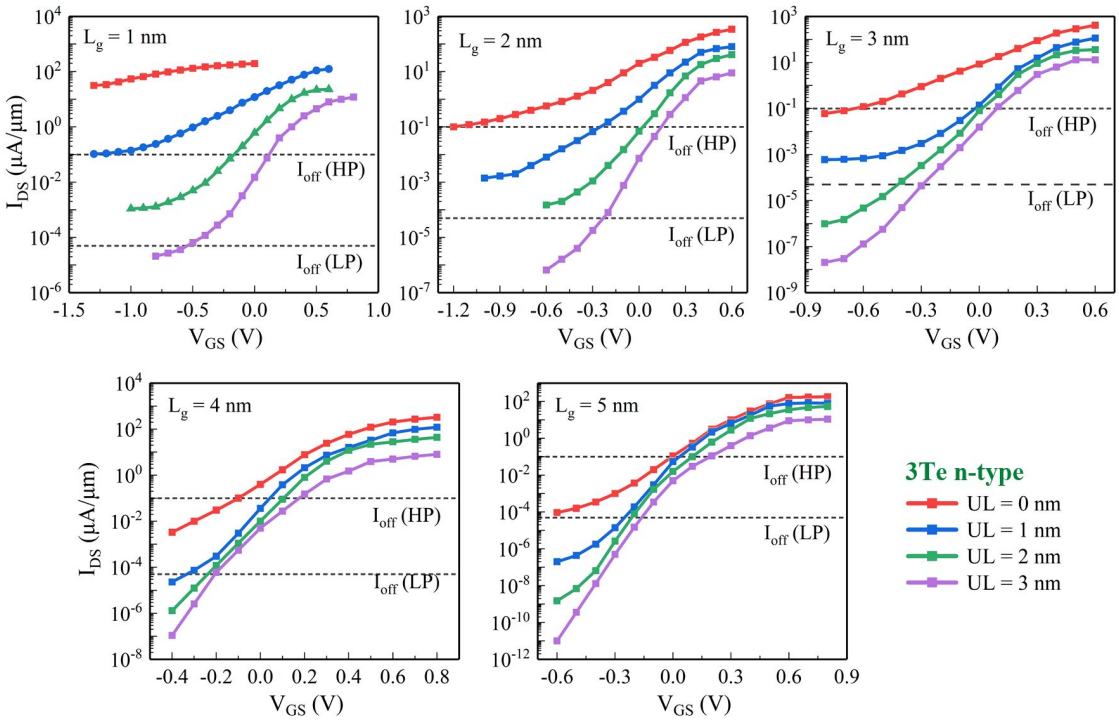

Figure S9. The transfer *I–V* curves of n–type 3Te GAA MOSFETs. The dash lines are the HP and LP threshold I_{off} set to 0.1 μA/μm and 5×10^{-5} μA/μm, respectively, according to the ITRS standards.

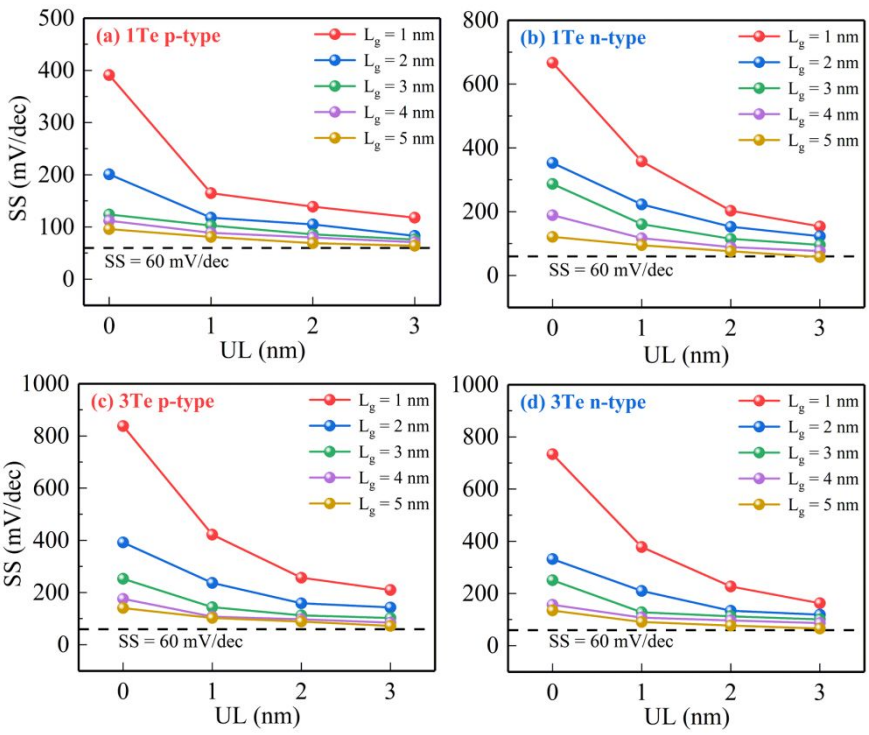

Figure S10. The SS of Te FETs as a function of UL. The dash lines in (a-d) represent the thermionic limit (60 mV/dec) of SS.

Table S4. Benchmark of p-type 1Te FETs performance compared with HP and LP ITRS goals.

L_g (nm)	UL (nm)	I_{on} (HP) (μA/μm)	I_{on} (LP) (μA/μm)	SS (mV/dec)	τ (HP) (ps)	PDP (HP) (fJ/μm)	τ (LP) (ps)	PDP (LP) (fJ/μm)
5	0	495	95	96	0.489	0.11	1.358	0.098
	1	431	103	81	0.451	0.085	0.721	0.065
	2	118	27	69	1.448	0.671	2.261	0.046
	3	49	9	64	3.134	0.063	6.094	0.041
4	0	478	–	112	0.371	0.103	–	–
	1	442	80	89	0.320	0.058	0.840	0.057
	2	303	22	80	0.445	0.052	2.043	0.031
	3	67	4	71	1.860	0.047	10.383	0.026
3	0	447	–	124	0.253	0.083	–	–
	1	432	51	103	0.227	0.045	0.936	0.043
	2	287	17	86	0.328	0.036	1.679	0.02
	3	36	3	76	2.457	0.031	8.934	0.016
2	0	246	–	201	0.273	0.068	–	–
	1	386	–	118	0.133	0.039	–	–
	2	140	5	105	0.486	0.023	3.530	0.017
	3	45	2	83	0.898	0.018	5.776	0.011
1	0	–	–	391	–	–	–	–
	1	230	–	165	0.112	0.012	–	–
	2	123	1	139	0.188	0.01	23.184	0.008
	3	2.6	0.3	118	7.926	0.009	68.693	0.006
ITRS goals	–	900	295	–	0.423	0.240	1.493	0.280

Table S5. Benchmark of n-type 1Te FETs performance compared with HP and LP ITRS goals.

L_g (nm)	UL (nm)	I_{on} (HP) (μA/μm)	I_{on} (LP) (μA/μm)	SS (mV/dec)	τ (HP) (ps)	PDP (HP) (fJ/μm)	τ (LP) (ps)	PDP (LP) (fJ/μm)
5	0	3215	–	121	0.079	0.122	–	–
	1	6479	–	95	0.036	0.098	–	–
	2	3701	762	76	0.055	0.088	0.139	0.065
	3	1643	248	60	0.111	0.082	0.384	0.058
4	0	–	–	189	–	–	–	–
	1	6401	–	117	0.016	0.074	–	–
	2	3014	10	89	0.042	0.071	12.659	0.048
	3	1443	346	77	0.036	0.050	0.174	0.035
3	0	–	–	257	–	–	–	–
	1	619	–	161	0.179	0.053	–	–

	2	2847	–	115	0.028	0.042		
	3	1253	20	96	0.059	0.034	3.696	0.014
2	0	–	–	353	–	–	–	–
	1	–	–	223	–	–	–	–
	2	958	–	153	0.059	0.032	–	–
	3	1208	–	123	0.032	0.022	–	–
1	0	–	–	667	–	–	–	–
	1	–	–	358	–	–	–	–
	2	6	–	203	4.034	0.018	–	–
	3	546	–	154	0.042	0.013	–	–
ITRS goals	–	900	295	–	0.423	0.240	1.493	0.280

Table S6. Benchmark of p-type 3Te FETs performance compared with HP and LP ITRS goals.

L_g (nm)	UL (nm)	I_{on} (HP) (μA/μm)	I_{on} (LP) (μA/μm)	SS (mV/dec)	τ (HP) (ps)	PDP (HP) (fJ/μm)	τ (LP) (ps)	PDP (LP) (fJ/μm)
5	0	1024	–	141	0.295	0.124	–	–
	1	1073	67	103	0.133	0.108	3.535	0.097
	2	784	58	89	0.163	0.093	4.084	0.073
	3	456	39	72	0.233	0.081	6.073	0.069
4	0	242	–	176	0.847	0.098	–	–
	1	903	–	108	0.150	0.073	–	–
	2	683	13	98	0.105	0.065	8.360	0.065
	3	211	38	85	0.313	0.061	2.630	0.056
3	0	–	–	253	–	–	–	–
	1	528	–	144	0.301	0.063	–	–
	2	567	2	113	0.175	0.054	49.613	0.041
	3	276	10	103	0.264	0.049	7.290	0.036
2	0	–	–	392	–	–	–	–
	1	21	–	237	5.111	0.037	–	–
	2	200	–	159	0.385	0.028	–	–
	3	217	2	143	0.184	0.023	30.081	0.02
1	0	–	–	838	–	–	–	–
	1	–	–	422	–	–	–	–
	2	17	–	257	1.718	0.019	–	–
	3	130	–	210	0.137	0.016	–	–
ITRS goals	–	900	295	–	0.423	0.240	1.493	0.280

Table S7. Benchmark of n-type 3Te FETs performance compared with HP and LP ITRS goals.

L_g (nm)	UL (nm)	I_{on} (HP) (μA/μm)	I_{on} (LP) (μA/μm)	SS (mV/dec)	τ (HP) (ps)	PDP (HP) (fJ/μm)	τ (LP) (ps)	PDP (LP) (fJ/μm)
5	0	237	–	135	1.722	0.162	–	–
	1	65	17	91	4.342	0.147	16.602	0.103
	2	35	11	77	7.643	0.133	24.320	0.091
	3	13	4	66	19.545	0.116	63.520	0.085
4	0	144	–-	157	1.52	0.135	–	–
	1	73	7	108	2.727	0.107	28.434	0.087
	2	40	15	97	4.608	0.088	12.288	0.072
	3	11	5	87	16.233	0.081	35.712	0.06
3	0	12	–	251	14.453	0.097	–	–
	1	101	–	128	1.451	0.085	–	–
	2	35	5	113	3.310	0.065	23.168	0.058
	3	19	2	101	5.726	0.058	54.400	0.042
2	0	5	–	332	20.608	0.054	–	–
	1	48	–	210	1.827	0.043	–	–
	2	27	1	134	2.702	0.039	72.960	0.035
	3	14	0.3	119	4.526	0.032	211.200	0.029
1	0	–	–	734	–	–	–	–
	1	3	–	378	16.427	0.031	–	–
	2	21	–-	227	1.615	0.025	–	–
	3	12	0.1	163	2.187	0.022	262.400	0.021
ITRS goals	–	900	295	–	0.423	0.240	1.493	0.280

Table S8. I_{on} and SS of 1Te FETs with and without SOC.

Doping type	SOC	I_{on} (HP) (μA/μm)	SS (mV/dec)
p–type	without SOC	924	141
	with SOC	978	163
n–type	without SOC	181	135
	with SOC	165	140

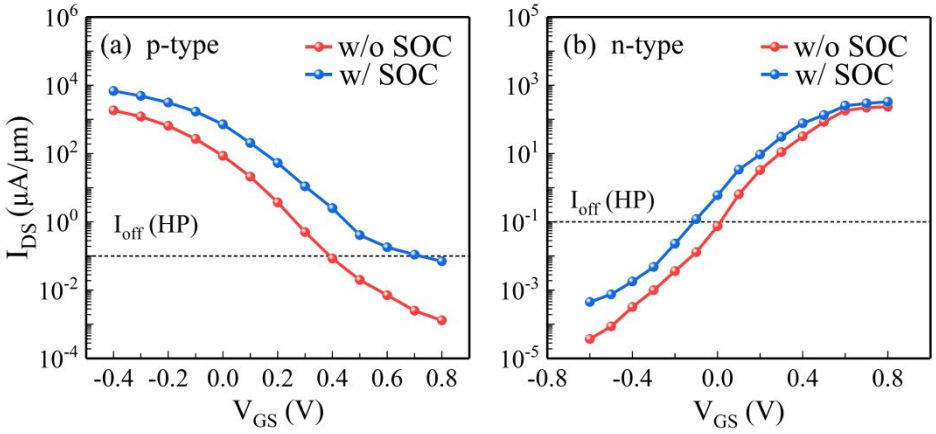

Figure S11. Transfer *I–V* curves of (a) p–type and (b) n–type 3Te MOSFETs with and without SOC effect. The dash lines are the high performance threshold I_{on} set to 0.1 μA/μm according to the ITRS standards.

Reference

1. Yin, Y. *et al.* Anisotropic Transport Property of Antimonene MOSFETs. *ACS Appl. Mater. Interfaces* **12**, 22378-22386, (2020).