Supporting Information

Doping-Free All $PtSe_2$ Transistor via Thickness-Modulated Phase Transition

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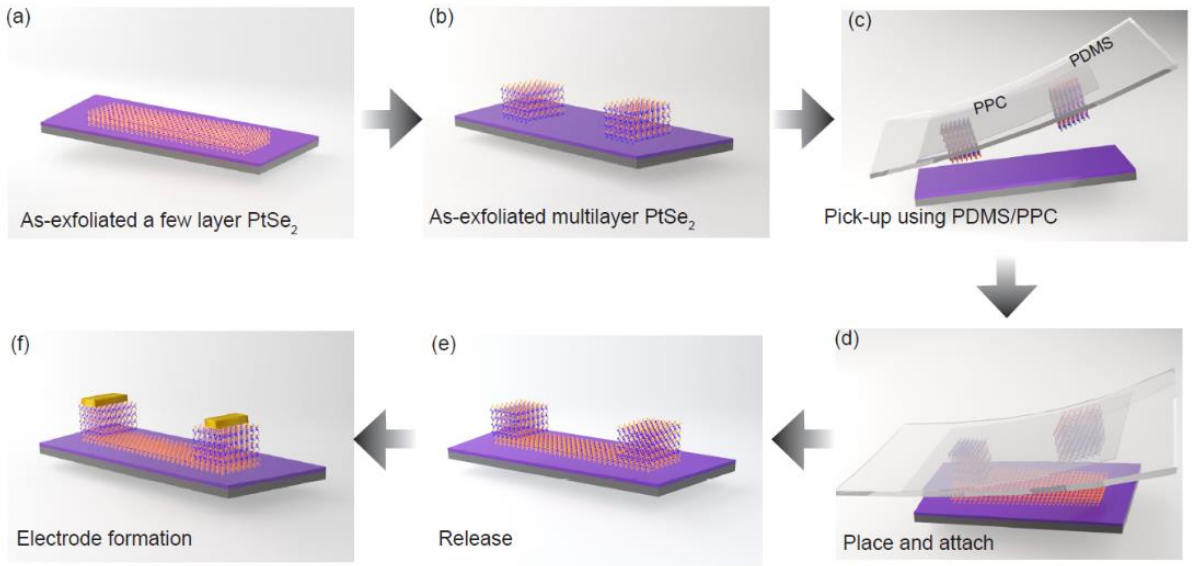

Figure S1. Fabrication process of $PtSe_2$ FETs using $PtSe_2$ vdW integration. (a-f) Detailed description of the dry transfer. (a, b) The ultrathin few layer semiconducting $PtSe_2$ and the thick multilayer $PtSe_2$ with the intrinsic metallic property were mechanically exfoliated from bulk $PtSe_2$ crystals on SiO_2/Si substrate. (c) Pick up: To pick-up the multiplayer $PtSe_2$ flake, the exfoliated multilayer $PtSe_2$ flake on SiO_2/Si substrate was placed under a microscope on a hot stage. A PDMS/PPC polymer block was attached on a slide-glass and held in a micro manipulator and placed above the sample with polymer facing toward the $PtSe_2$ target. Then, the polymer was brought in close contact with the $PtSe_2$ flake by lowering the manipulator height until the polymer completely covers the flake. Next, the glass slide was retracted slowly, which picked up the $PtSe_2$ flake from the SiO_2 on the surface PPC. (d) Placing: The SiO_2/Si substrate with the exfoliated semiconducting $PtSe_2$ flake was then placed on a hot stage. The previously picked-up multilayer $PtSe_2$ flake was aligned over the target few layer semiconducting $PtSe_2$ flake and precisely controlled to the position over the chosen flake before contacting together. At this point the temperature was elevated to 90 ^oC and PDMS/PPC proceeded slowly to contact fully. (e) Release:

Subsequently, the glass slide holding the polymer block was slowly moved upward using the micromanipulator. In this manner, the multiplayer $PtSe_2$ flake on PCC was released and attached onto the semiconducting $PtSe_2$ flake. (f) Contact fabrication: Metallic multilayer $PtSe_2$ was finally connected with the conventional Ti/Au metal for the characterization in a back-gated FETs geometry.

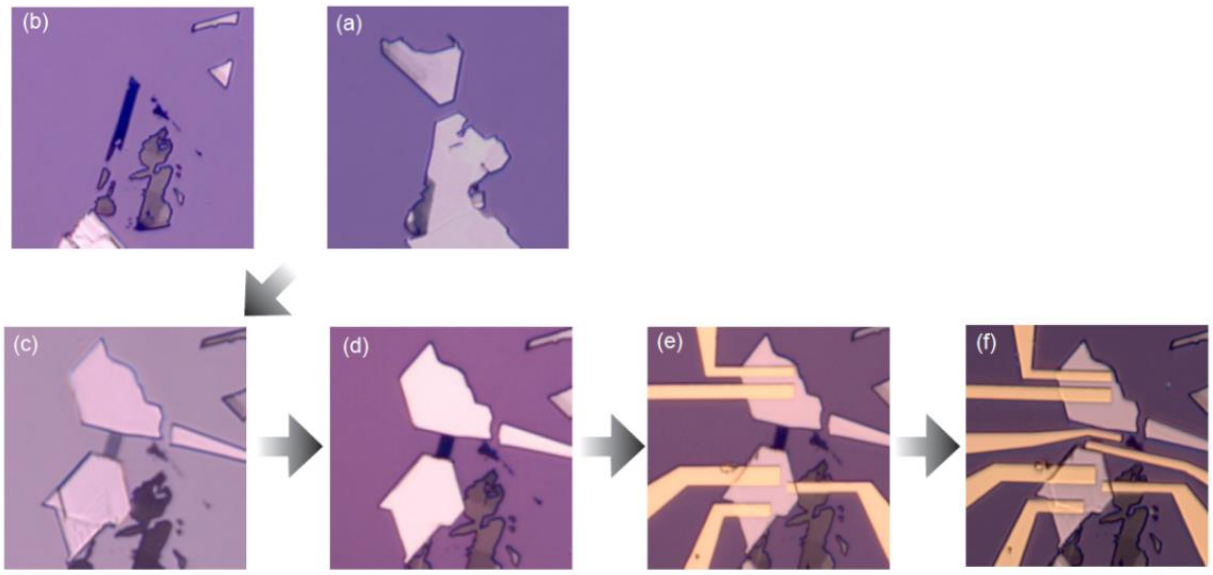

Figure S2. OM images in sequence showing the fabrication of few layer $PtSe_2$ FETs with $PtSe_2$ vdW contact. (a, b) Exfoliated multilayer and few layer $PtSe_2$ on SiO_2/Si substrate. (c) Pick-up and place: Two previously exfoliated multilayer $PtSe_2$ flakes (shown in Figure a) were picked up using PPC at a same time and dropped down on top of the ultrathin semiconducting $PtSe_2$ flake (shown in Figure b). (d) Release: The dropped-down $PtSe_2$ flake was adhered by the strong vdW interaction and PPC was removed from the stack. (e, f) Fabricated $PtSe_2$ vdW contact and Ti/Au contact FETs on the same $PtSe_2$ flake, respectively.

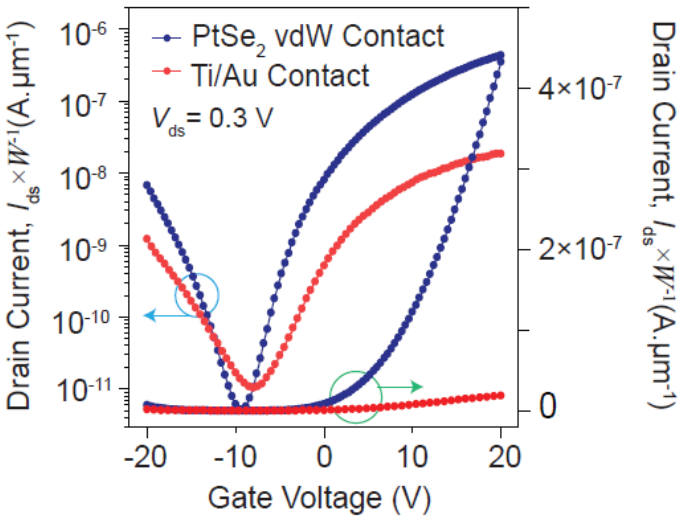

Figure S3. Room-temperature semi-logarithmic and linear transfer curve (I_{ds}-V_{gs}) comparing few layer $PtSe_2$ FETs with $PtSe_2$ vdW contact and Ti/Au contact. The current is normalized by width (W). From the width normalized transfer characteristics, the ON current levels could be compared more fairly.

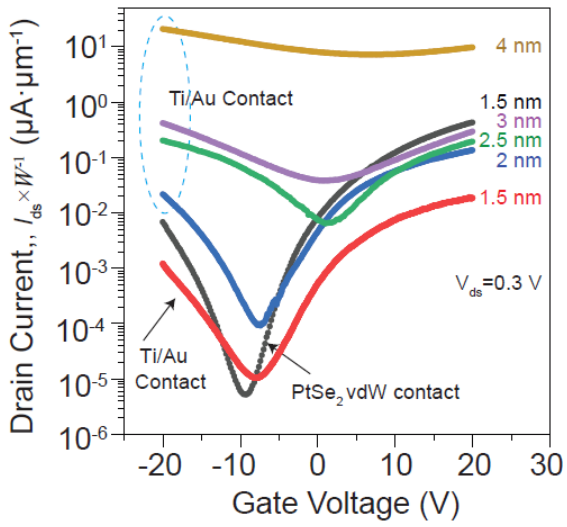

Figure S4. Thickness-modulated transport property of $PtSe_2$ FETs. A progressive transition of electrical transport properties of $PtSe_2$ FETs with the various thicknesses of $PtSe_2$ flakes is summarized here. We observed more than six orders increase in the OFF current from ~10^{-5} to ~10 μA as the thickness varies from ~1.5 to ~4 nm. The n-type conduction property in the thinnest sample was transformed into more symmetrical ambipolar behavior as the thickness increases until there is an appreciable band gap in the $PtSe_2$ flake. Remarkably, the $PtSe_2$ devices maintained their typical ambipolar behavior up to ~3 nm, but the insufficient increase in the maximum ON current lowered the current tunability by the gate voltage as the thickness increases. The transfer characteristics finally became independent on the gate voltage in the 4 nm thick $PtSe_2$ FETs, which is consistent with the decrease in band gap size, indicating the semiconducting to metallic phase transition in $PtSe_2$. Interestingly, the representative $PtSe_2$ vdW contact FETs with the 1.5 nm channel thickness exhibited superior ON current than the ~3 nm thick $PtSe_2$ FETs with conventional Ti/Au contact.

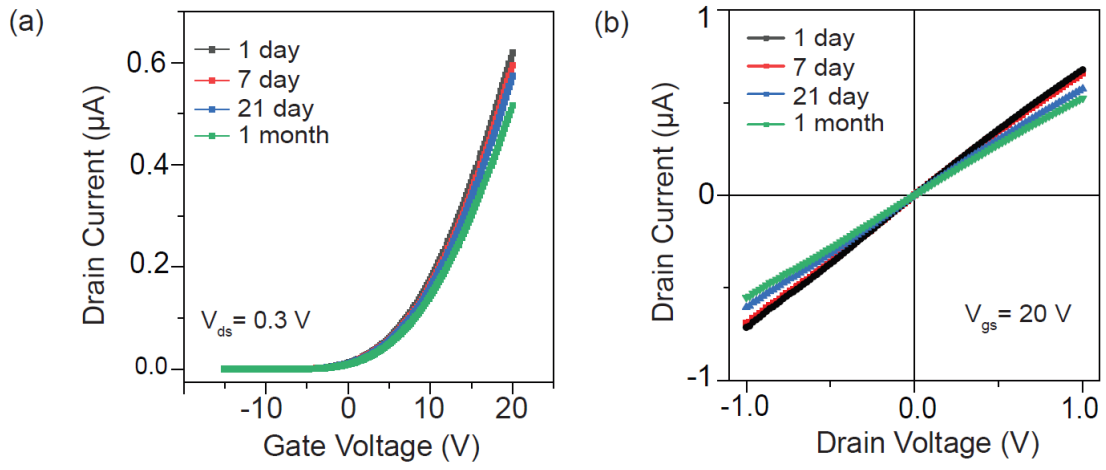

Figure S5. Stability of $PtSe_2$ vdW contact FETs. (a, b) Typical transfer and output characteristics of few layer $PtSe_2$ FETs with $PtSe_2$ vdW contact. Our representative device exhibited a stable device performance over month with minimal degradation in the ON current (~0.6 to ~0.5 μA) in the ambient condition. This limited degree of variation in the device performance was possibly due to the degradation in dielectric environments which is independent of 2D materials. It is well known that the metallic phase-engineered TMDs such as 1T-MoS_2 and 1T'-WTe_2 can be severely oxidized by the chemical adsorption of O_2 after the air exposure, resulting in the insufficient ambient stability. Doping induced aging effect and environmental degradation are the two main reason for instability [1]. Our phase transition mediated $PtSe_2$ vdW contact eliminates the chance of aging related to chemical doping and the intrinsic stability of $PtSe_2$ resulted to demonstrate long-term stability to air for months only with a minor change in the transfer characteristics which is promising for the potential use of new 2D device architecture.

Contact Resistance Calculation Using the Y-Function Method

YFM is an effective technique for the low-field mobility (μ_0) extraction utilizing the I_{ds}-V_{gs} and g_m-V_{gs} characteristics at low V_{ds} in the linear region [2]. This method has been extensively adopted in the research of organic thin-film transistors (TFTs) and recently applied in the analysis of MoS_2 based FETs as it can be also used to estimate the contact resistance and the threshold voltage. I_{ds} and g_m in the linear region are expressed by the following well known equations:

$$I_{ds} = \frac{W}{L} C_{ox} \mu_{eff} (V_{gs} - V_{th}) V_{ds}$$

$$I_{ds} = \frac{W}{L} C_{ox} \frac{\mu_0}{1+\theta(V_{gs}-V_{th})} (V_{gs} - V_{th}) V_{ds} \quad \text{(S1)}$$

$$g_m = \frac{W}{L} C_{ox} \frac{\mu_0}{[1+\theta(V_{gs}-V_{th})]^2} V_{ds} \quad \text{(S2)}$$

where W and L are the effective channel width and length, C_{ox} is the gate oxide capacitance, μ_0 is the low-field mobility, θ is the mobility attenuation coefficient, and V_{th} is the threshold voltage. The influence of the mobility attenuation with V_{gs} can be eliminated by combining the equation S1 and S2 to achieve a simplified function defined as Y-function:

$$Y = \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{\mu_0 C_{ox} V_{ds} \frac{W}{L}} (V_{gs} - V_{th}) \quad \text{(S3)}$$

The extracted threshold voltage values assist to determine the mobility reduction factor related to the contact resistance, surface roughness, and phonon scattering which can be expressed by:

$$\theta = \left[\frac{I_{ds}}{\left(g_m (V_{gs}-V_{th})\right)} - 1 \right] / (V_{gs} - V_{th}) \quad \text{(S4)}$$

In strong inversion, this function is expected to be a constant equal to the value of the mobility reduction coefficient. The mobility attenuation factor θ described in equation S1, S2 and S4 is θ =

$\theta_{ch}+\theta_c = \theta_{ch}+R_c\mu_0 C_{ox}W/L$, where θ_{ch} is the mobility attenuation factor from the channel related to the surface roughness and phonon scattering and θ_c is the mobility attenuation factor due to contact. In absence of $\theta_{ch,,}$ the upper limit of R_c can be extracted eventually from the expression, $R_c = \frac{\theta}{\mu_0 C_{ox}}\frac{L}{W}$.

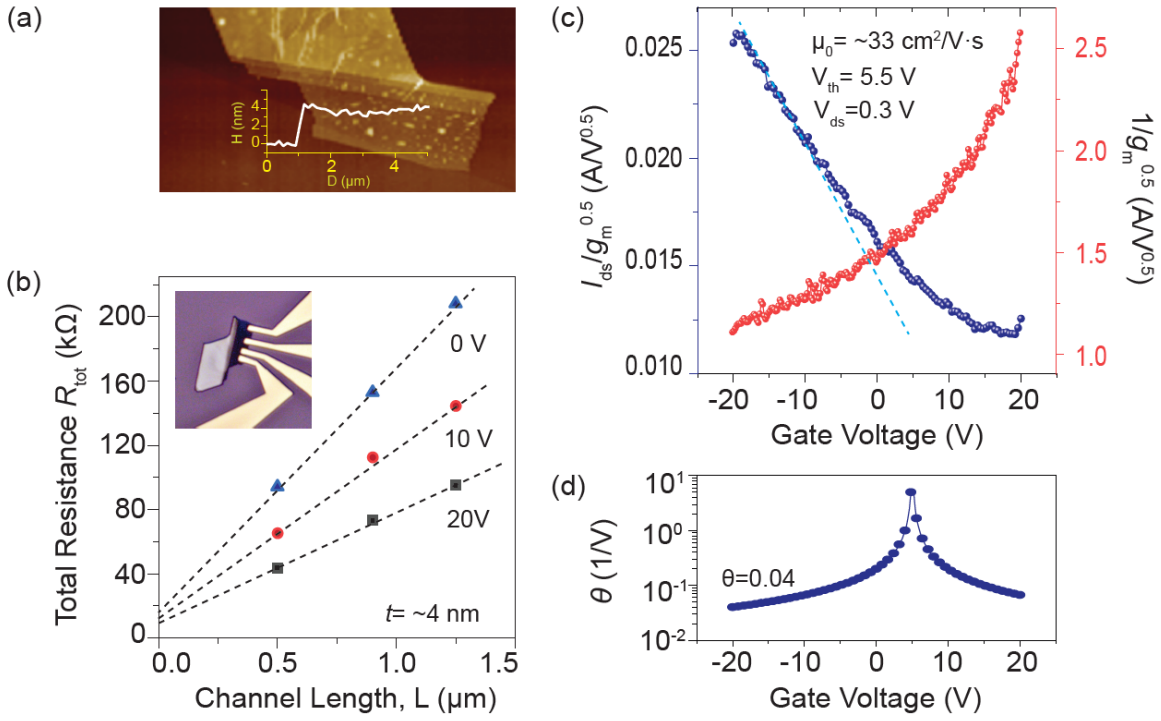

Figure S6. Comparison of the contact resistance (R_c) in a 4 nm thick $PtSe_2$ FETs by TLM and YFM. (a) AFM image of a 4 nm thick $PtSe_2$ flake with the corresponding height profile in the inset. (b) Total device resistance (R_{tot}) *vs.* channel length (L) measured by TLM, for different V_{gs}. Linear extrapolation of R_{tot} *vs.* L in the vertical y-axis intercept provides the estimation of R_c of ~6 kΩ·μm for a 4 nm thick $PtSe_2$ FETs with Ti/Au contact. (c) Extraction of R_c for the same 4 nm $PtSe_2$ FETs using YFM for direct comparison. The threshold voltage and low-field mobility were estimated as 5.5 V and ~33 $cm^2/V{\cdot}s$ from the interception and slope of $\frac{I_{ds}}{\sqrt{G_m}}$ *vs.* V_{gs}, respectively.

(d) The mobility reduction coefficient (θ) *vs.* V_g plot. With, $\theta = R_c\mu_0 C_{ox} W/L$, R_c of 43 kΩ·μm was extracted from the strong inversion region. This result suggests that YFM overestimated R_c for the same device and yielded ~7 times higher R_c compared to TLM.

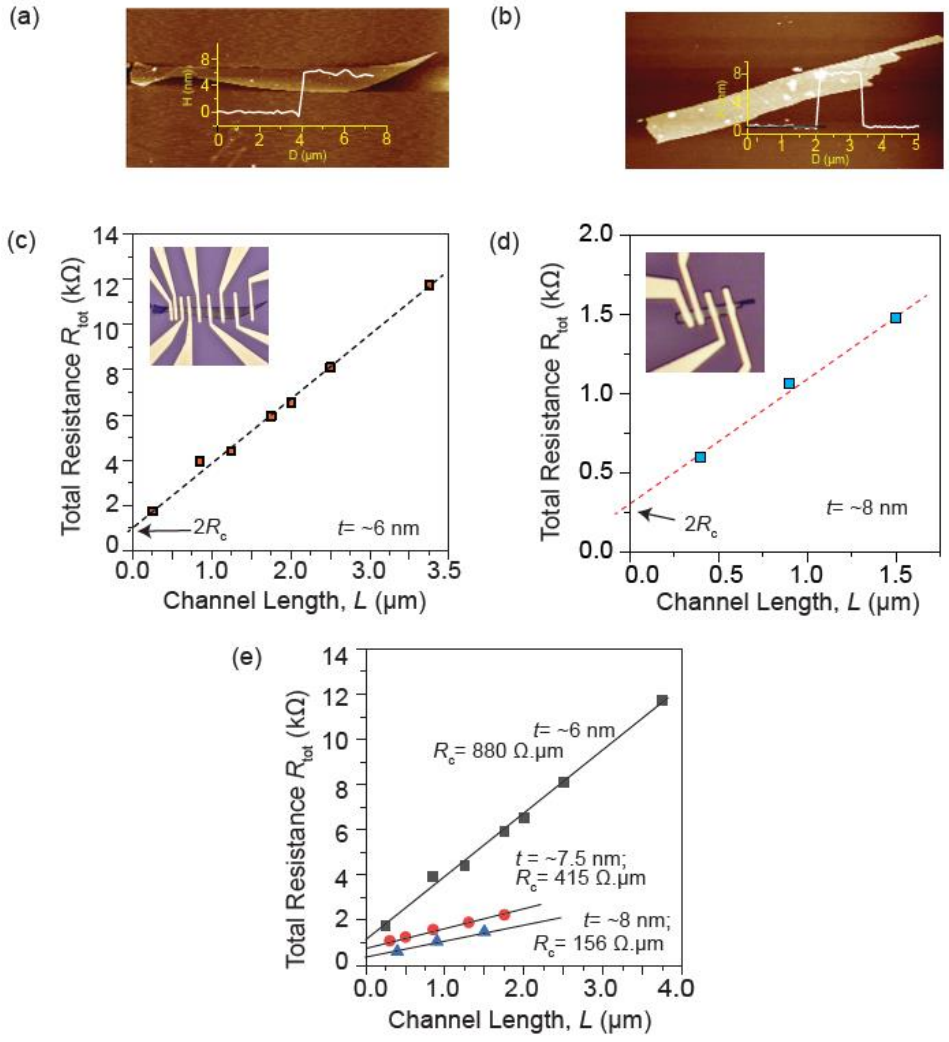

Figure S7. Contact resistance (R_c) extraction of $PtSe_2$ FETs with Ti/Au contact for various $PtSe_2$ channel thicknesses. (a, b) AFM images of various $PtSe_2$ flakes used for TLM measurement. Inset is the corresponding line profile of the particular flake, showing that the thickness of the $PtSe_2$ channel is ~6 and ~8 nm, respectively. (c, d) The results of TLM measurements for Ti/Au contact FETs. Corresponding OM images of the fabricated multilayer $PtSe_2$ TLM structure is shown in the inset. The contact resistance can be extracted from the *y*

intercept of the linear fit to the total resistance as a function of the channel length. As predicted theoretically, being metallic in nature, both the ~8 and ~6 nm thick $PtSe_2$ devices exhibit perfectly linear I_{ds}-V_{ds} behaviors without any gate dependence. (e) The extracted contact resistances from the various thicknesses of $PtSe_2$ flakes are summarized and the result shows that the contact resistance as low as ~150 Ω·μm for a ~8 nm thick $PtSe_2$ can be achieved.

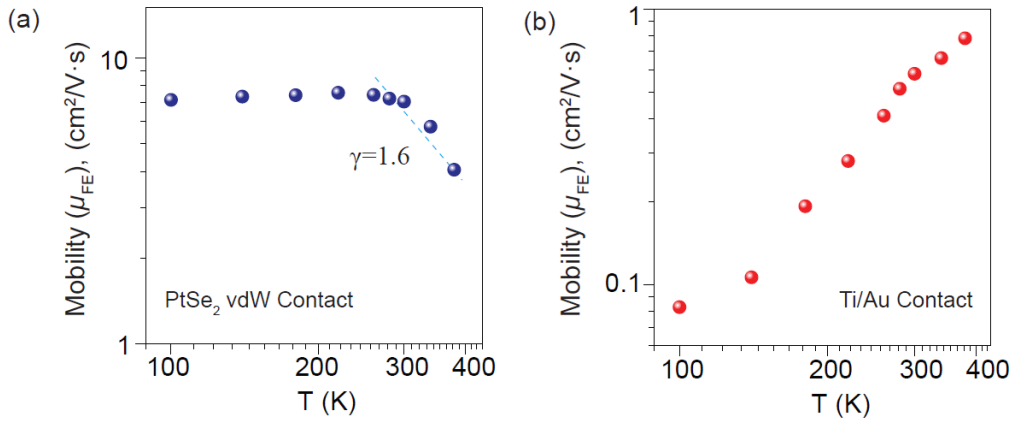

Figure S8. (a, b) Temperature-dependent field-effect mobility (μ_{FE}) of $PtSe_2$ vdW contact and Ti/Au contact devices. Mobility *vs.* temperature for $PtSe_2$ vdW contact reveals that calculated mobility remained almost saturated at low temperature due to charge impurity scattering. At high temperature (over 240 K), mobility started to decrease with the increasing temperature because of optical phonon scattering which can be fitted by a generic power law of $\mu_{FE} \sim T^{-\gamma}$ where $\gamma \approx 1.6$. This trend is consistent with the behavior of mobility limited by optical phonon scattering in other 2D TMDs [3]. On the contrary, mobility for conventional Ti/Au contact rapidly increased from 0.09 to 0.76 $cm^2/V{\cdot}s$ with the increasing temperature. The temperature-dependent increase of mobility implies a thermionic emission dominant carrier transport in Ti/Au contact possibly due to the existence of a higher SBH.

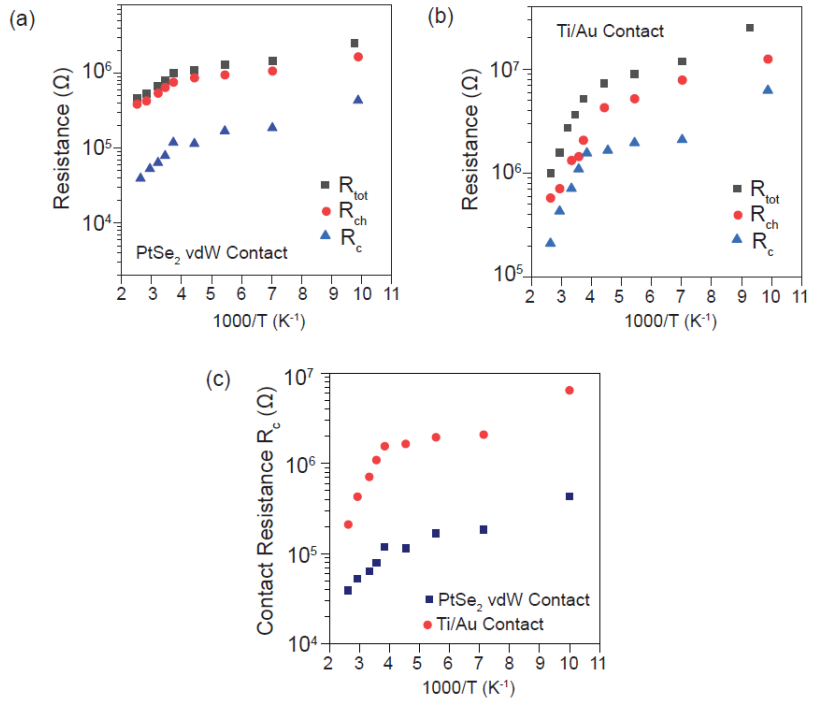

Figure S9. Extraction of temperature-dependent total resistance (R_{tot}), channel resistance (R_{ch}), and contact resistance (R_c) for $PtSe_2$ vdW contact and Ti/Au contact devices. (a, b) Total resistance (R_{tot}; squares), channel resistance (R_{ch}; circle) and contact resistance (R_c; triangle) as function of 1000/T for $PtSe_2$ vdW contact and Ti/Au contact devices, respectively. The channel resistance can be extracted from temperature-dependent I_{ds} measurement in Figure 5a and b, using following expression:

$$R_{\mathrm{ch}}(T) = \frac{1}{qn\mu(T)}\frac{L}{Wt}$$

where q is the elementary charge, $n = \left(\frac{C_{\mathrm{ox}}}{q}\right)(V_{\mathrm{gs}} - V_{\mathrm{th}})/t$ is the carrier density where t is the channel thickness, and μ(T) is the temperature dependent mobility of the device. The total resistance was calculated simply by using $R_{tot} = V_{ds}/I_{ds}$ at V_{ds} = 0.3 V and V_{gs} = 20 V, where channel resistance turns out to be insignificant. Henceforth, R_c is computed by (R_{tot}-R_{ch})/2 for each temperature. (c) Comparison of contact resistance for $PtSe_2$ vdW contact and Ti/Au contact FETs.

It was found that $PtSe_2$ vdW contact device shows one order magnitude lower contact resistance compared to the Ti/Au contact device.

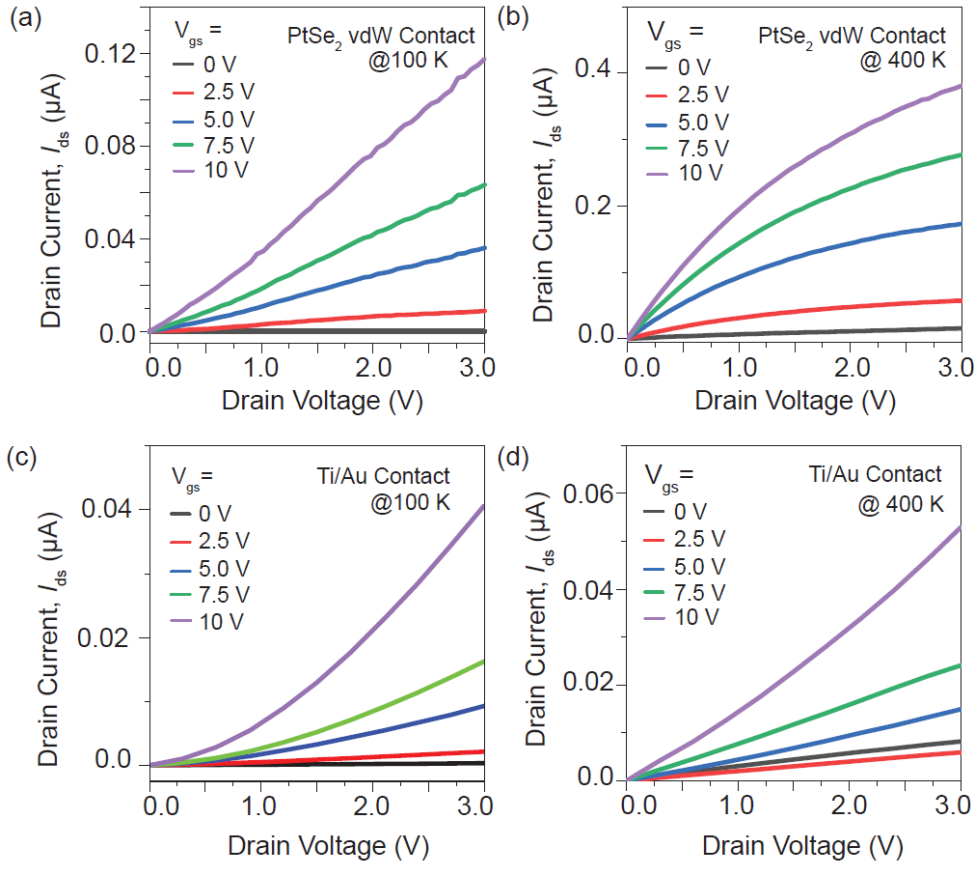

Figure S10. Comparison of temperature-dependent output (I_{ds}–V_{ds}) characteristics of $PtSe_2$ vdW contact and Ti/Au contact FETs. Output characteristics of the both devices were measured at 100 and 400 K, respectively. (a, b) Typical output characteristics in $PtSe_2$ vdW contact FETs at low temperature reveals that output curves maintained their linearity even at 100 K, suggesting the absence of a contact barrier whereas an excellent current saturation can be observed at 400 K which implies the true ohmic behavior. (c, d) In contrast, Ti/Au contact FETs clearly shows current crowding at low V_{ds} due to the large contact resistance and non-saturated output curve at high

temperature which further implies the existence of significant SB compared to the $PtSe_2$ vdW contact devices.

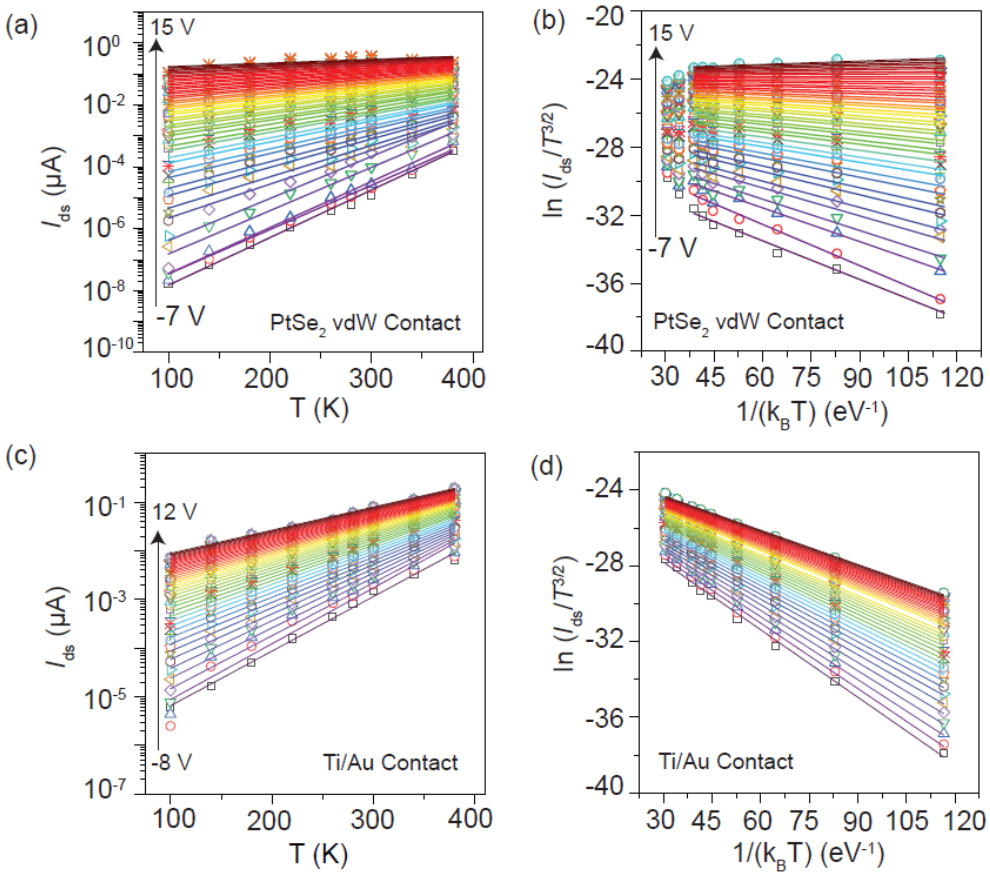

Figure S11. Temperature-dependent transport for $PtSe_2$ vdW contact and Ti/Au contact FETs in the thermionic emission model. The thermionic emission equation is simplified to $I_{ds} = \left[A^* T^{3/2} \exp\left(-\frac{q\Phi_{SB}}{k_B T}\right)\right]$ for $qV_{ds} \gg k_B T$. In the sub-threshold regime the transistor behavior can be expressed as $I_{ds} = \left[A^* T^{3/2} \exp\left(-\frac{q\Phi_{bi}}{k_B T}\right)\right]$, where Φ_{bi} is the built in potential. At the flat-band condition, $q\Phi_{bi}$ becomes equal to $q\Phi_{SB}$ [4]. (a, c) Temperature-dependent semi-logarithmic current I_{ds} *vs.* temperature T plot for $PtSe_2$ vdW contact and Ti/Au contact FETs. (b, d) Corresponding linear fit to the Arrhenius plot of $\ln(I_{ds}/T^{3/2})$ *vs.* $1/k_B T$ at various V_{gs} for $PtSe_2$ vdW contact and

Ti/Au contact FETs, respectively. The SBH estimated from the slope of a linear fit are shown in Figure 5e and f.

Table S1. Comparison of recently reported $PtSe_2$ FETs with different contact materials

Preparation Method	**$PtSe_2$ thickness (nm)**	**Electrode Material**	**Fabrication method**	**Carrier type**	**ON/OFF ratio**	**Mobility [$cm^2 V^{-1} s^{-1}$]**	**Rc**	**SBH [meV]**	**Ref.**
mechanical exfoliation	2-5	Pd	e-beam lithography	n	10^5	3	NA	NA	[5]
CVD	1.6	Au	direct laser write	p	40	5–9	600 kΩ.μm	NA	[6]
				n	25	6–12	200 kΩ.μm		
CVT	11	Ti/Au	e-beam lithography	n	200	210	NA	NA	[7]
TAC and transfer to secondary substrates	2.5−3	Ni/Au	e-beam lithography	p	230	0.3, 10 (after correction)	1.65×10^6 Ω	E_A=200 meV	[8]
Vapor-phase selenization	3	Ni/Au	shadow mask	p	30	3.5	184 kΩ.μm	NA	[9]
Plasma assisted selenization	2.5	Pt	Photo-lithography	p	16	0.7	NA	NA	[10]
Thermally assisted selenization	4	Al	Photo-lithography	p	1.9	3	3 kΩ.μm	NA	[11]
Mechanical exfoliation	3	$PtSe_2$	ICP RIE, e-beam lithography	p	93	150	0.3 kΩ.μm	NA	[12]
Mechanical exfoliation	1.5	$PtSe_2$	Dry Transfer, e-beam lithography	n	10^5	7.5	93 kΩ·μm	35	This Work

Missing values are represented by NA (not available). Data are from refs [5-12]

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