Supplementary Information

Ambipolar Deep-Subthreshold Printed-Carbon-Nanotube Transistors for Ultralow-Voltage and Ultralow-Power Electronics

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Supplementary Information

SI1. Subthreshold Swing and Gate Dielectric Capacitance

A gate dielectric with large areal capacitance is key to achieving a steep subthreshold swing in sc-SWCNTN TFTs. Indeed, from general TFT theory[1]:

$$SS = \frac{1}{\log_{10}(e)}\frac{kT}{q}\left(1 + \frac{D_{tr}q}{C_d}\right) \quad \text{(S1)}$$

Here, C_d is the effective areal capacitance of the gate dielectric, D_{tr} the interfacial trap density, k the Boltzmann's constant, T the absolute temperature, and q the elementary charge. It is noteworthy that in sc-SWCNTN TFTs the effective areal capacitance is given by[2,3]:

$$C_d = \Lambda_0^{-1}\left\{C_q^{-1} + \frac{1}{2\pi\epsilon_0\epsilon_r}\ln\left[\frac{\Lambda_0}{R\pi}\sinh\left(\frac{2\pi t_d}{\Lambda_0}\right)\right]\right\}^{-1} \quad \text{(S2)}$$

Here, C_q is the intrinsic quantum capacitance of the sc-SWCNTs (4.0 10^{-10} F m^{-1}), Λ_0 is the average distance between the sc-SWCNTs in the network, R is their mean radius, t_d is the gate dielectric thickness, and $\epsilon_0\epsilon_r$ is the permittivity of the gate dielectric. Equation S2 indicates that, for $2\pi t_d \gg \Lambda_0$ (limit of high intertube coupling), C_d approaches the parallel plate capacitance $\epsilon_0\epsilon_r/t_d$. Within this limit, Eq. S1 and S2 jointly illustrate the need to reduce the thickness of the gate dielectric as well as to boost its dielectric constant so as to achieve sc-SWCNTN TFTs with steep SS.

SI2. Nanodielectric Properties

The hybrid oxide/C_{18}-PA nanodielectric has an areal capacitance of $C_{ox\text{-}C18} \approx 0.63$ μF/cm^2 at 1 kHz (**Fig. SF2**). At the same frequency, the hybrid oxide/FC_{17}-PA counterpart has an areal capacitance of $C_{ox\text{-}FC17} \approx 0.54$ μF/cm^2 (**Fig. SF2**). A much higher areal capacitance can be obtained by not using a SAM atop the AlO_x surface ($C_{ox} \approx 1.83$ μF/cm^2 at 1 kHz) (**Fig. SF2**). However, such thin AlO_x layer alone does not provide sufficient insulation as gate dielectric, with leakage currents above the 10^{-5} A cm^{-2} range at an applied bias of 1 V (**Fig. SF2**). In fact, by grafting SAM molecules onto the AlO_x surface, the leakage is reduced approximately by two orders of magnitude.

In consideration that the geometric areal capacitance may differ from the effective areal capacitance in sc-SWCNTN TFTs (Eq. S2), we additionally characterized the capacitance of complete sc-SWCNTN TFTs. We found that the effective areal capacitance in the oxide/FC_{17}-PA/sc-SWCNTN case is ≈ 0.32 μF/cm^2, while in the oxide/C_{18}-PA/sc-SWCNTN case it amounts to 0.37 μF/cm^2 (**Fig. SF2.1**). It is noteworthy that the difference in effective capacitance values between the two types of nanodielectric matches the difference in their geometric capacitance (≈ 13% in both cases).

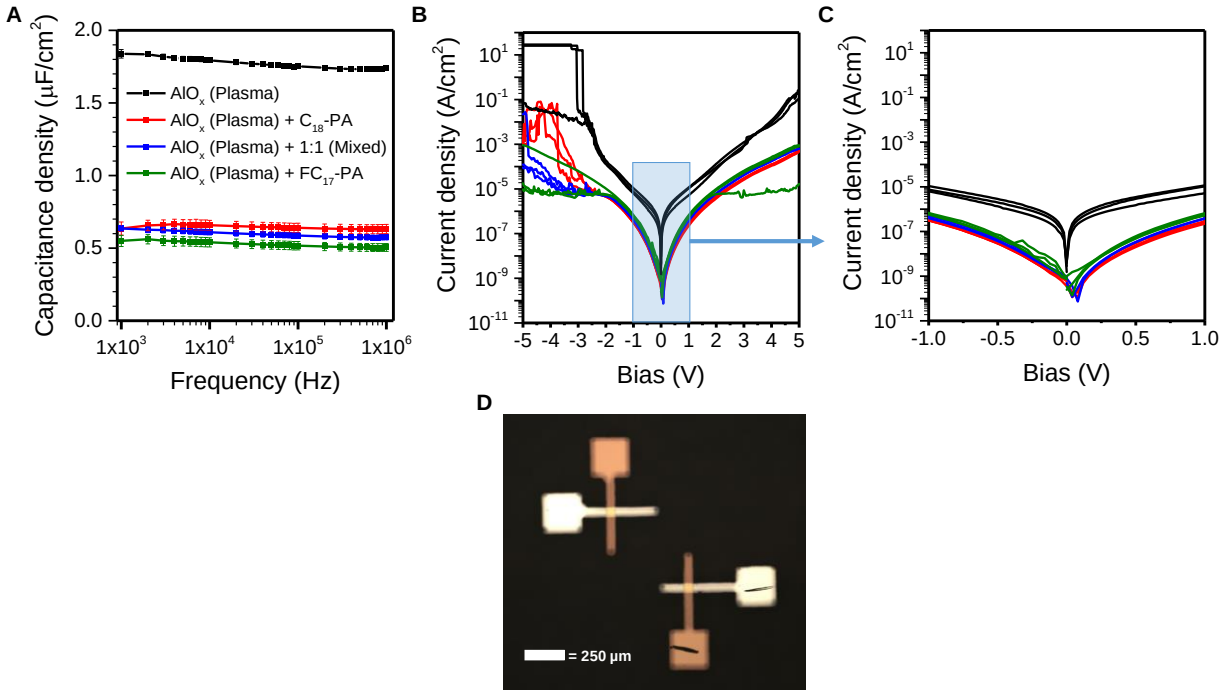


Fig. SF2. Capacitance and leakage current of SAM nanodielectrics. (**A**) Areal capacitance of bare AlO_x (plasma-generated) *vs.* AlO_x (plasma-generated) plus SAM (C_{18}-PA, 1:1 (Mixed), or FC_{17}-PA), the error bars represent the standard deviation. (**B**) Corresponding leakage current densities. (**C**) Magnified version of panel B. (**D**) Micrograph of the 50×50 μm^2 capacitor structures used for the characterization of the dielectric layers.

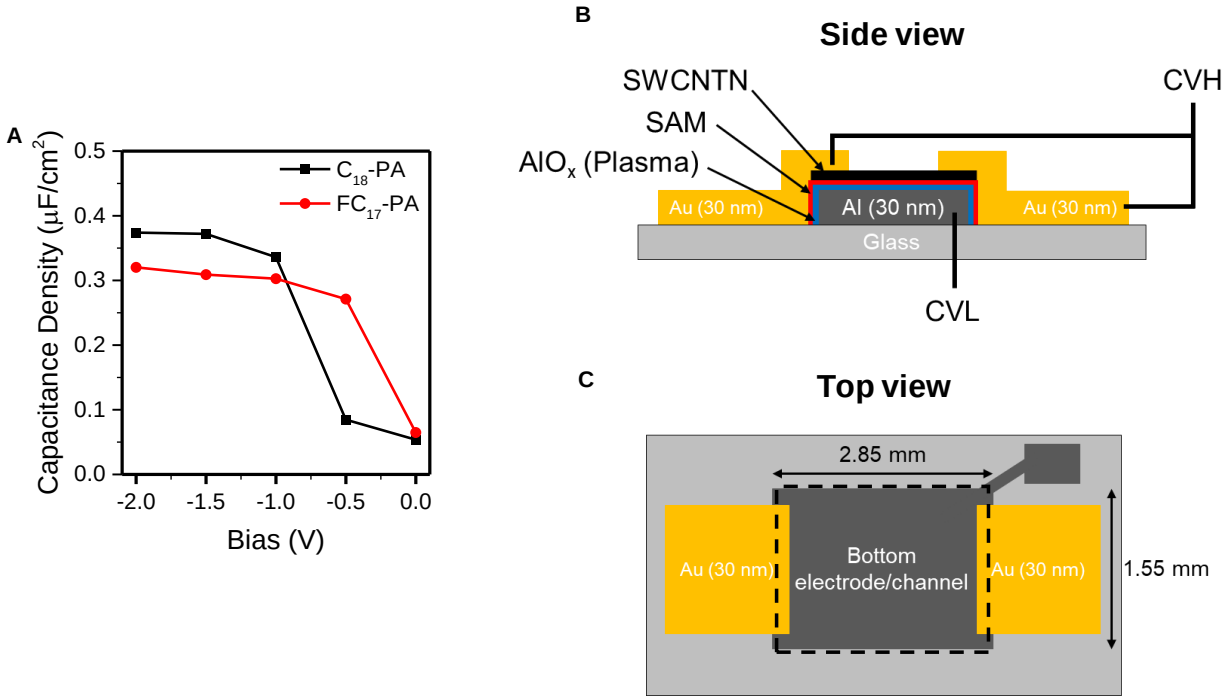


Fig. SF2.1. Effective capacitance of sc-SWCNTN-hybrid nanodielectrics. (**A**) Capacitance-voltage (C-V) curves from sc-SWCNTNs printed atop different SAM nanodielectrics (modulation frequency = 1 Hz). A frequency of 1 Hz is employed in this measurement because the SWCNTN channel must be allowed to fully accumulate in order to accurately determine the gate-SWCNTN capacitive coupling. This is made necessary by the long channel length employed in the device structure of this specific experiment, which sets a limit on the maximum frequency that can used to ensure full accumulation of the SWCNTN channel. (**B** and **C**) Schematic side and top views of the structure employed for the C-V measurements. The capacitance was measured between the terminals labelled CVH and CVL. The dashed line in C indicates the contour of the sc-SWCNTN.

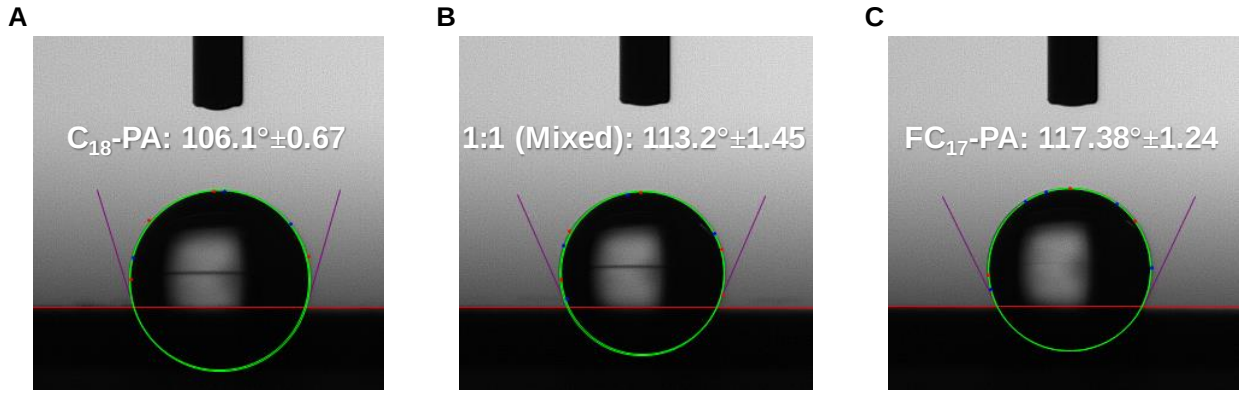


Fig. SF2.2. Static contact angles on SAM/AlO_x nanodielectrics. Deionized water static contact angle on (**A**) C_{18}-PA (**B**) 1:1 (Mixed) (**C**) FC_{17}-PA SAM-treated AlO_x. Static contact angle measurements were conducted at room temperature and in air with 20 µL droplets using a Kino SL150L goniometer (KINO, USA).

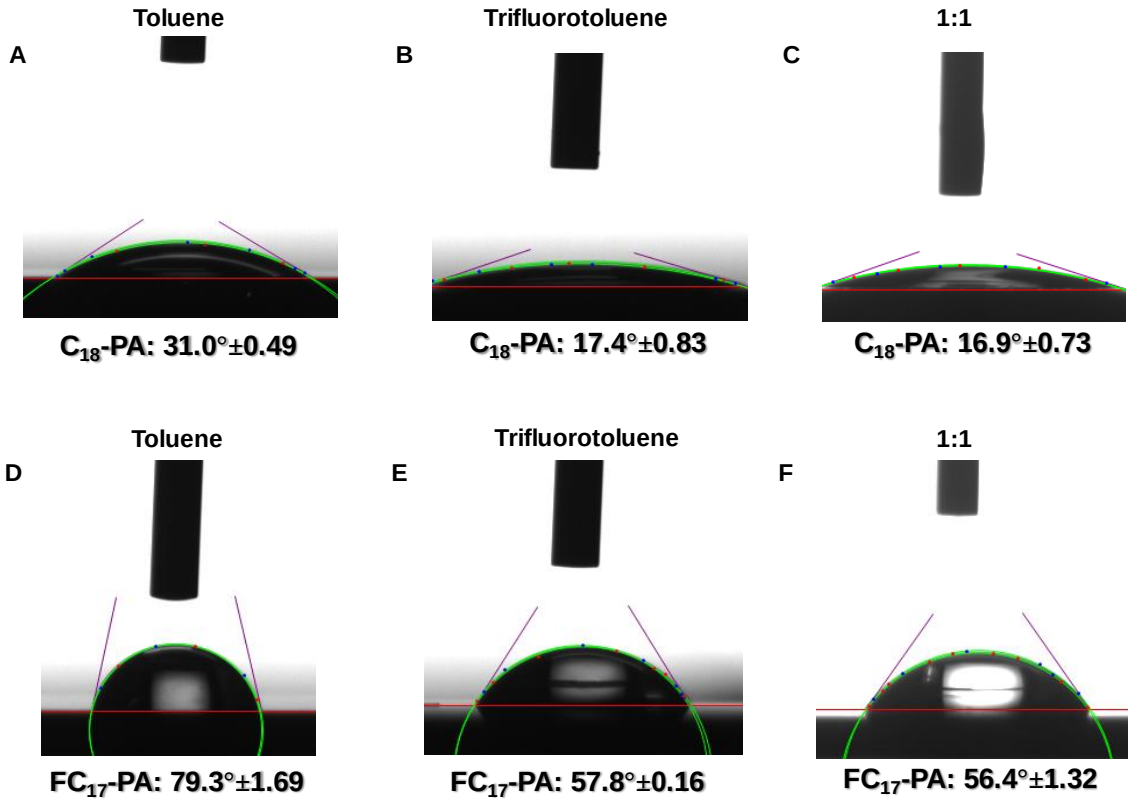


Fig. SF2.3. Static contact angles of toluene, trifluorotoluene and a 1:1 mixture of toluene and trifluorotoluene on SAM/AlO_x nanodielectrics. C_{18}-PA-SAM/AlO_x nanodielectric: contact angles of (**A**) toluene, (**B**) trifluorotoluene, and (**C**) a 1:1 mixture of toluene and trifluorotoluene. FC_{17}-PA-SAM/AlO_x nanodielectric: contact angles of (**D**) toluene, (**E**) trifluorotoluene, and (**F**) a 1:1 mixture of toluene and trifluorotoluene. Static contact angle measurements were conducted at room temperature and in air with 20 µL droplets using a Kino SL150L goniometer (KINO, USA).

SI3. Environmental stability

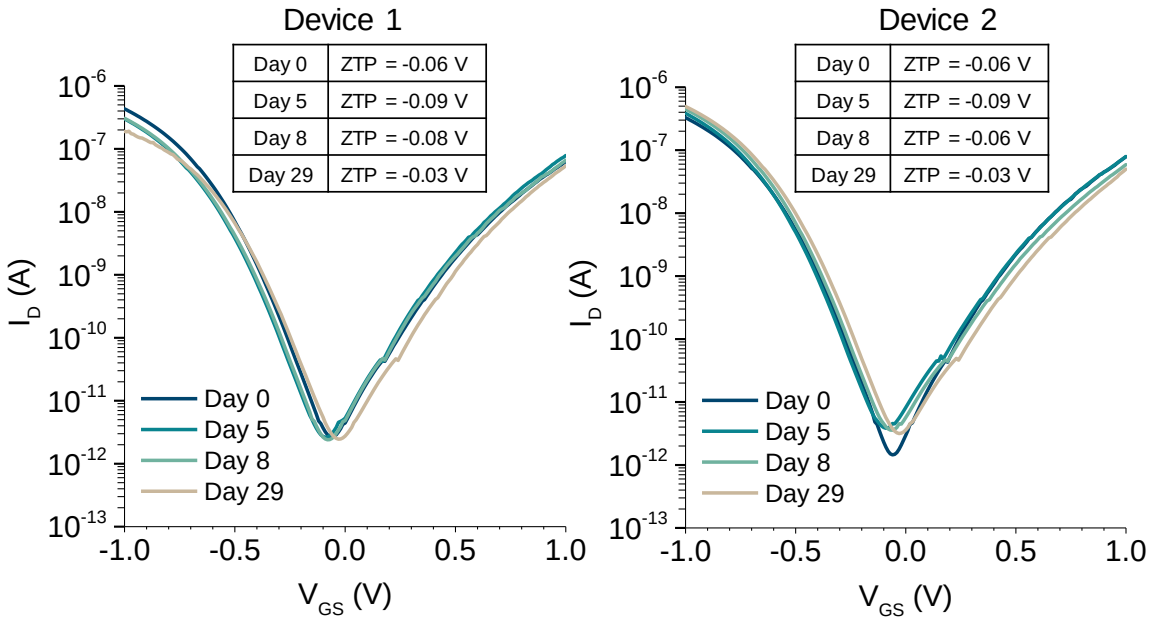


Fig. SF3. Air stability. Deep-subthreshold characteristics of two representative ambipolar sc-SWCNTN TFTs over a period of 1 month. Insets show the corresponding ZTP values. Both TFTs (W_{ch}/L_{ch} = 100 µm / 20 µm) were characterized at V_{DS} = -0.25 V, in air, and at the times specified in the legend. Between the measurements, the TFTs were stored in a closed container, in air and at room temperature. Over the course of one month, the total ZTP shift amounts to 30 mV. Firstly, this is negligible compared to the ZTP shift that occurs within minutes in a non-encapsulated device exposed to air (**SI9**). Additionally, a comparison with **Fig. 2e** reveals that such shift is inconsequential in terms of circuit functionality.

The encapsulation consists of a polymer bilayer of PMMA and Parylene-C. This bilayer was selected because: a) PMMA at the interface with the sc-SWCNTN is inert with respect to the electronic properties of the sc-SWCNTN, as detailed in SI. 9; b) the Parylene-C layer significantly improves on the barrier property of the 180-nm-thick PMMA layer, resulting in a bilayer that enables highly stable devices, as shown in **SF3**.

SI4. Mobility

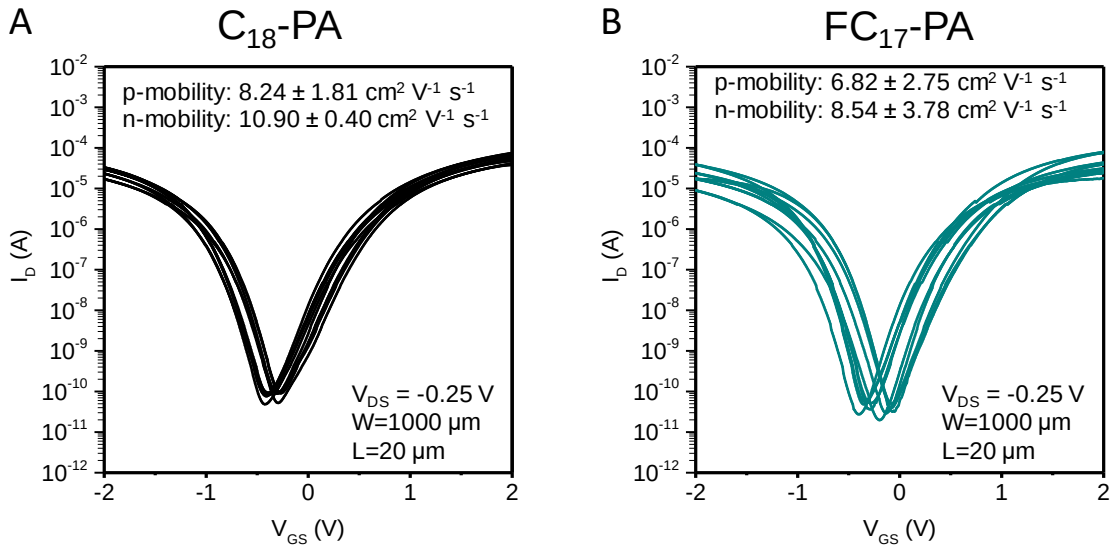


Fig. SF4. Device transfer curves. (A) Transfer characteristics of C_{18}-PA devices and their calculated average mobility and deviation. (B) Transfer characteristics of FC_{17}-PA devices and their calculated average mobility and deviation.

The mobility was calculated using the equation for calculating the linear mobility of field effect transistors $\mu_{lin} = (L/WC_dV_{DS}) \cdot (\partial I_D/\partial V_{GS})$, where L is the channel length, W is the channel width, C_d is the effective areal capacitance of the dielectric, V_{DS} is the drain to source voltage, I_D is the drain current and V_{GS} is the gate voltage. In regard to C_d, its value was obtained as described in **SF2.1**.

SI5. Threshold voltage extraction

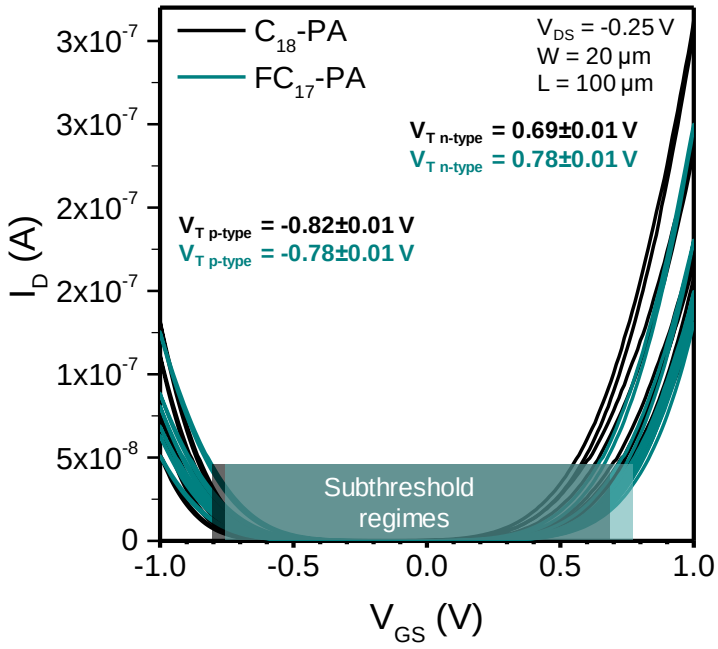


Fig. SF5. Threshold voltage extraction. Linear transfer characteristics of C_{18}-PA and FC_{17}-PA devices. The intersection points on the V_{GS} axis of lines tangent to the I_D curves were employed to extract the threshold voltage values. The shaded boxes indicate the subthreshold region.

SI6. Scanning kelvin probe (SKPM) measurements

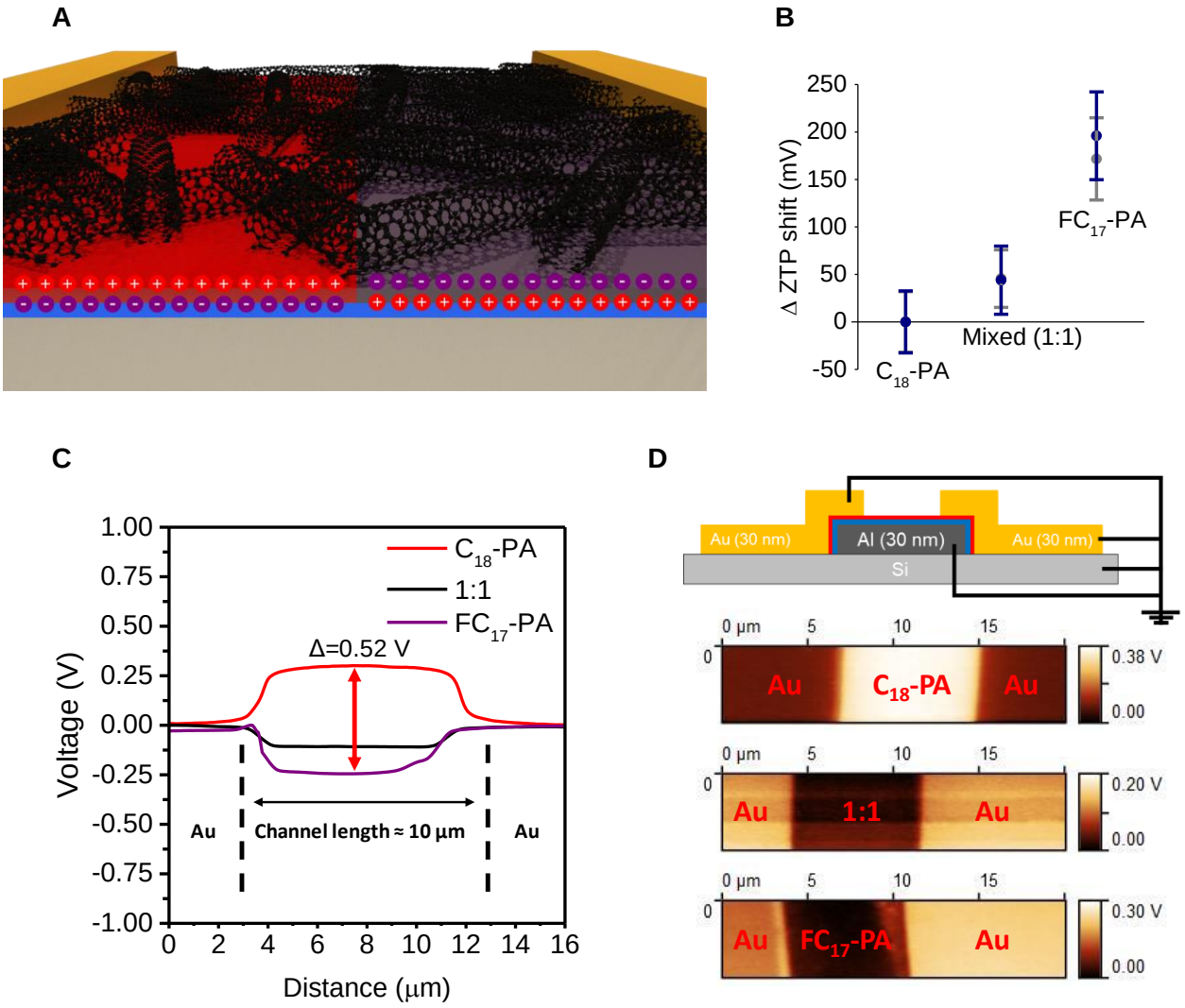


Fig. SF6. Evaluation of the effect of the SAMs in the nanodielectrics. (**A**) Schematic representation of the SAM-nanodielectric sc-SWCNTN TFTs and of the dipoles within the SAMs. (**B**) ZTP shifts of devices incorporating a 1:1 Mixed SAM and FC_{17}-PA SAM relative to C_{18}-PA devices the error bars represent the standard deviation. (**C**) Surface potential measured *via* Scanning Kelvin Probe Microscopy (SKPM) when moving the probe from source to drain over the nanodielectrics surface. Such measurements were carried out on nanodielectrics comprising a C_{18}-PA SAM, a FC_{17}-PA SAM, and a 1:1 SAM mixture. (**D**) Schematic illustration of the device structure and of the electrical connections (all electrodes connected to the SKPM ground) employed for the SKPM measurements (top). Surface potential maps obtained over different nanodielectrics when scanning the SKPM between source and drain electrodes (bottom).

SI7. ZTP Shift *versus* SAM Dipole Moments

C_{18}-PA and FC_{17}-PA SAM molecules were considered in this work because of their pronounced and opposed dipole moments along the longitudinal axis, and because of the general ability of phosphonic acid molecules to form highly ordered and dense monolayers on AlO_x surfaces[4]. These dipoles deliver a net electric field (hence, an electrostatic potential difference across) when aligned within a monolayer, which can potentially enable the fine-tuning of TFT characteristics (vide infra).

To gain insight into the workings of C_{18}-PA and FC_{17}-PA SAMs, we firstly calculated their dipole moments *via* Density Functional Theory (DFT). We found that C_{18}-PA and FC_{17}-PA molecules give dipole moments of 1.20 D and -0.75 D, respectively. This enabled us to estimate the electrostatic potential difference across the SAMs V_{SAM} by the Helmholtz equation (Eq. S3)[5], and the associated electric field E_{SAM} *via* Eq. S4, when these molecules assemble into an orderly monolayer[6] on an AlO_x substrate:

$$V_{SAM} = \frac{N\mu_{\perp}}{\epsilon_0 \epsilon_{SAM}} \quad \text{(S3)}$$

$$E_{SAM} = \frac{V_{SAM}}{t_{SAM}} = \frac{N\mu_{\perp}}{\epsilon_0 \epsilon_{SAM} t_{SAM}} \quad \text{(S4)}$$

Here N is the grafting density of the SAM molecules, $\mu_{\perp}$ and t_{SAM} are the dipole moment component and the thickness of the SAM along the substrate normal (respectively), and ϵ_0 and ϵ_{SAM} are the vacuum permittivity and the SAM relative permittivity (respectively).
If we take N = 4 molecules/nm^2, ϵ_{SAM} = 2.5 [7] and assume the molecules to be oriented along the AlO_x substrate normal, we obtain $V_{C18\text{-}PA}$ = 0.72 V and $V_{FC17\text{-}PA}$ = -0.46 V. This corresponds to a V_{SAM} difference between the two SAMs of 1.18 V. In fact, these estimates only represent an upper limit on the electrostatic potential difference across each SAM. This is because such molecules generally adopt a non-zero tilt angle within a SAM grafted onto AlO_x with respect to the substrate normal. Accounting for ≈ 30° – 50° tilt angles (as experimentally determined in previous reports)[8–10], more realistic estimates of the electrostatic potential differences across the two SAMs are obtained: $V_{C18\text{-}PA} \approx 0.4 – 0.6$ V and $V_{FC17\text{-}PA} \approx -0.3 – -0.4$ V. This corresponds to a V_{SAM} difference between the two SAMs of ≈ 0.8 V.

Further insight can be gained by experimentally evaluating the difference in surface potential of the AlO_x/SAM nanodielectrics *via* Scanning Kelvin Probe Microscopy (SKPM) (**SI6**). Specifically, the samples considered in these experiments feature the same structure utilized for the TFTs but without sc-SWCNTs (*i.e.*, Glass/Al/AlO_x/SAM/Au). In addition to C_{18}-PA and FC_{17}-PA SAMs, we also considered a SAM obtained from a stoichiometric 1:1 mixture of C_{18}-PA and FC_{17}-PA. By grounding the gate, source and drain electrodes and by scanning the probe along the path from source to drain, SKPM enabled us to experimentally determine the surface potential of the nanodielectrics with respect to the SKPM probe workfunction. C_{18}-PA and FC_{17}-PA nanodielectrics give surface potential values of 0.30 V and -0.25 V, respectively, while the mixed SAM nanodielectric leads to the intermediate value of -0.1 V (**SI6**). It is important to note that these SKPM surface potential values are referenced to the SKPM probe, hence they are not an

absolute measure of V_{SAM}. However, differences between SKPM surface potential values from different nanodielectrics are indeed a direct manifestation of V_{SAM} differences. Consequently, the SKPM experiments indicate that the V_{SAM} difference between C_{18}-PA and FC_{17}-PA nanodielectrics amounts to 0.55 V. Therefore, SKPM confirms to a good extent our DFT and electrostatic calculations, not only in terms of the direction of the V_{SAM} differences, but also in their magnitude. In fact, quantitative discrepancies between the measured V_{SAM} differences and the corresponding estimates likely arise from our assumptions on the tilt angles and densities of the different SAMs. Assuming that the SAMs affect the TFTs only in respect to their electrostatically-relevant parameters (*i.e.*, net dipole, dielectric constant, and finite thickness), it can be straightforwardly derived that they would determine a V_{FB} shift by an amount equal to their electrostatic potential difference across (V_{SAM}). Indeed, considering the model case of a parallel plate capacitor comprising our SAM nanodielectrics and with an applied voltage V across, the areal charge density σ on the plates can be expressed as:

$$\sigma = \frac{1}{\frac{1}{C_{AlO_x}} + \frac{1}{C_{SAM}}}(V - V_{SAM}) \tag{S5}$$

Here, $C_{AlO_x} = \epsilon_0 \epsilon_{AlO_x} / t_{AlO_x}$, ϵ_{AlO_x} and t_{AlO_x} are the relative permittivity and the thickness of the AlO_x layer, and $C_{SAM} = \epsilon_0 \epsilon_{SAM} / t_{SAM}$.

The flatband voltage shift derived from SKPM data is in fact consistent with the actual trend shown by the TFT characteristics, C_{18}-PA enhancing electron injection—*i.e.*, having a more negative ZTP—with respect the FC_{17}-PA counterpart in view of its positive V_{SAM}. However, the ZTP shift of ≈ 0.2 V between C_{18}-PA and FC_{17}-PA TFTs does not precisely match the SKPM-derived V_{SAM} difference of 0.55 V. As further detailed in **SI8b**, to a good extent this arises from the fact that the ZTP is only an approximate measure of V_{FB}. In fact, mismatches between electron and hole subthreshold parameters may have an impact on the difference between ZTP and V_{FB} (**SI8b**). Nonetheless, the matching trend and similar magnitude of ZTP and V_{SAM} shifts emerging not only from C_{18}-PA and FC_{17}-PA TFTs, but also from the mixed-SAM case (**SI6**) provide strong evidence that the SAM dipole moments are the primary factor enabling the fine-tuning of the sc-SWCNTN TFT characteristics. Consequently, other possible factors (*e.g.*, sc-SWCNTN morphology, charge transport properties, interfacial trapping, environmental factors) determine only an adjustment on the ZTP values primarily set by the SAM dipole moments.

SI8. Device Modeling and Simulations

SI8a. Phenomenological Model Equations for Ambipolar Deep-Subthreshold sc-SWCNTN TFTs

The most basic assumption of the phenomenological model equations pertaining to our sc-SWCNTN TFT operation in the deep-subthreshold region is that the channel current can be written as the superposition of an electron current and a hole current. The expressions for both contributions can then be derived from the experimental data obtained in electron-only conduction and hole-only conduction, respectively. Indeed, these two bias regions can be discriminated by identifying the zero transconductance point (ZTP), *i.e.*, the point at which $dI_D/dV_G = 0\ S$. For gate voltages V_G significantly greater than V_{ZTP}, an electron-only current flows through the channel in virtue of the gate modulation of the quasi-Fermi level towards the sc-SWCNTN conduction band edge (**Fig. 1d-e**). By contrast, for $V_G \ll V_{ZTP}$ a hole-only current flows in the channel. In view of the conceptual symmetry between electron and hole conduction, in the following we narrow down our focus to the electron-only channel current I_e, and we later extend the derivation to the hole-only current I_h and the total channel current I_{TOT}.

In virtue of their narrow bandgap ($E_G \cong 0.6\ eV$), electron injection into our sc-SWCNTNs is expected to increase rapidly as the gate voltage is raised above the flatband voltage V_{FB}. In terms of energy band diagram, this corresponds to the occurrence of the following: a) an upward shift of the electron quasi-Fermi level in the channel; b) greater band bending at the interface between the sc-SWCNTN and the source/drain electrode (*channel electrodes* in the following). The specific functional dependence of the channel current on the gate voltage can be inferred from **Fig. SF8A**, which shows the experimental channel current data in the electron-only bias region as a function of the gate voltage V_G and at different drain voltage values V_D. These curves appear as straight lines in this semilogarithmic plot, their slope being independent of the specific drain voltage applied. This indicates that the electron-only channel current can be written as an exponential function of V_G of the form $I_e = f_1(V_D) \cdot exp(V_G/S_G)$ ($f_1(V_D)$ being a function of the drain voltage alone). Here S_G is a constant (*i.e.*, a quantity independent of the particular bias point) and specifically corresponds to the slope of the traces in **Fig. SF8A**, while $f_1(V_D)$ is a function of the drain voltage. In fact, this conforms to the typical phenomenology of deep-subthreshold conduction observed in unipolar thin-film transistors[1]. Finally, considering that a finite electron channel current requires the gate voltage to be raised above V_{FB}, it becomes apparent that it is actually the difference $V_G - V_{FB}$ that controls the current magnitude. Therefore, the electron-only channel current more precisely conforms to the following expression: $I_e = f_2(V_D) \cdot exp((V_G - V_{FB})/S_G)$ ($f_2(V_D)$ being a function of the drain voltage alone).

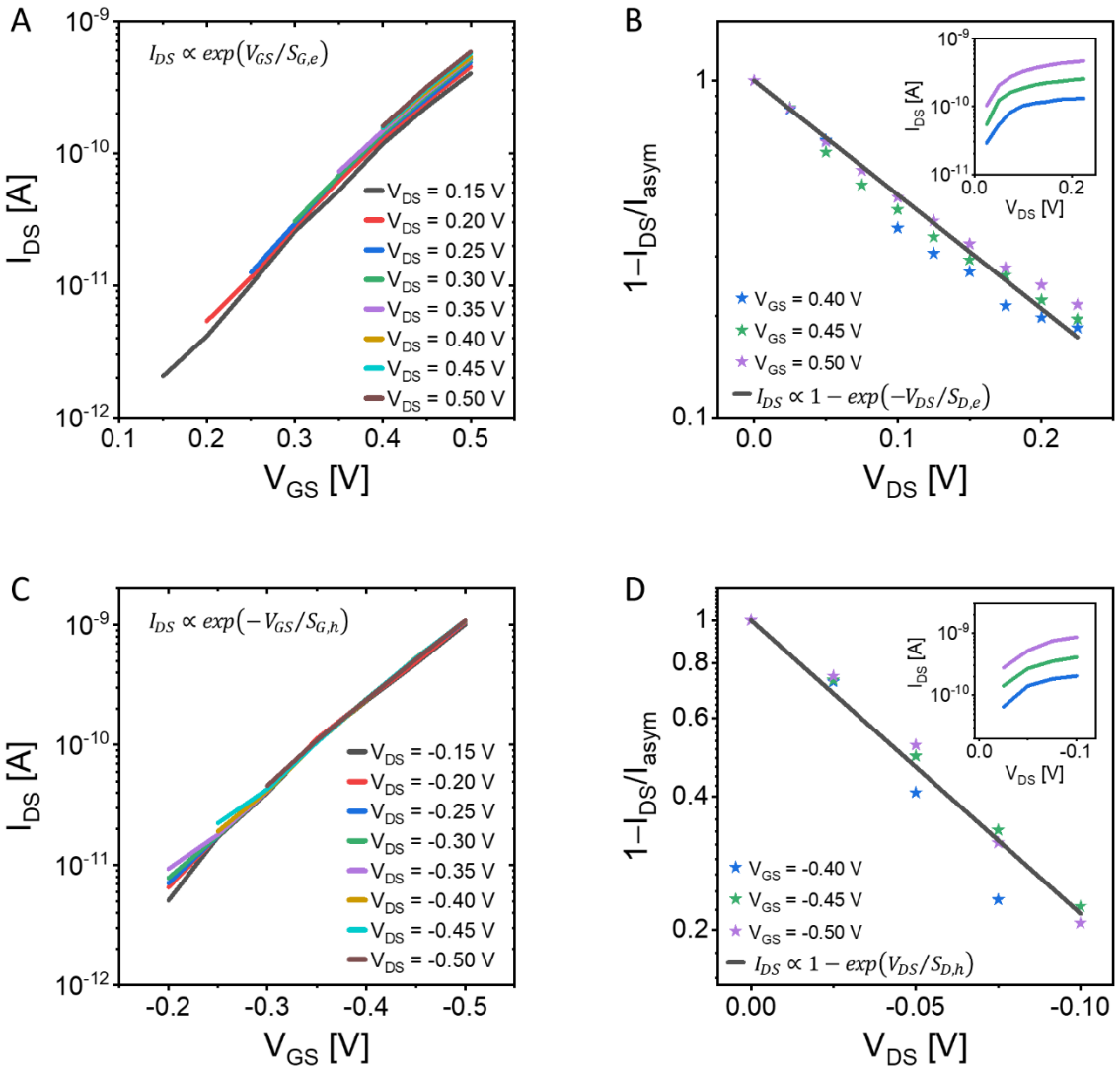


Fig. SF8. Experimental channel current (FC_{17}-PA TFTs) *versus* model equations. (**A**) Semilogarithmic plot of the experimental electron-only channel current *versus* gate-source voltage, manifesting a dependence of the type $I_{DS} \propto exp(V_{GS}/S_{G,e})$. (**B**) Plot derived from the experimental electron-only channel current (see inset) *versus* drain-source voltage, revealing a dependence of the type $I_{DS} \propto 1 - exp(-V_{DS}/S_{D,e})$. (**C**) Semilogarithmic plot of the hole-only channel current *versus* gate voltage, manifesting a dependence of the type $I_{DS} \propto exp(-V_{GS}/S_{G,h})$. (**D**) Plot derived from the experimental hole-only channel current (see inset) *versus* drain-source voltage, revealing a dependence of the type $I_{DS} \propto 1 - exp(V_{DS}/S_{D,h})$.

To ascertain the channel current dependence on the drain voltage, we now consider the inset of **Fig. SF8B** which shows the channel current as a function of V_D and at different V_G values. This plot indicates that the channel current rapidly rises with the drain voltage, and subsequently saturates to a value I_{sat} that depends on the applied V_G ($I_{sat} = I_{sat}(V_G)$). The specific dependence of the channel current on V_D becomes obvious when plotting the same characteristics as

$\ln(1 - I_e/I_{sat})$. All such curves collapse onto one another, appearing as straight lines, their slope independent of the specific gate voltage applied. This denotes that the electron-only channel current is an exponential function of V_D of the form $I_{sat}(V_G) \cdot \left(1 - exp(V_D/S_D)\right)$, where S_D is a constant (*i.e.*, a quantity independent of the particular bias point) and specifically corresponds to the slope of the traces in **Fig. SF8B**.

By combining the V_G and V_D dependences that have been separately assessed up to this point, we conclude that the deep-subthreshold electron-only channel current can be expressed as:

$$I_e = I_{0,e} \cdot \left(1 - e^{-\frac{V_{DS,e}}{S_{D,e}}}\right) \cdot e^{\frac{V_{GS,e} - V_{FB}}{S_{G,e}}} \qquad \text{for } V_{GS,e} \geq V_{FB} \qquad \text{(S6)}$$

where $I_{0,e}$ is a proportionality constant (referred to as *current prefactor* in the following), and an e has been introduced in all subscripts to denote that the respective quantities refer to electron-only conduction. For obvious reasons, we refer to $S_{D,e}$ as the drain subthreshold slope for electrons and to $S_{G,e}$ as the gate subthreshold slope for electrons. It is important to note that $S_{G,e}$ conceptually overlaps with the SS referred to in the main text, but only in the electron conduction region. Nonetheless, they quantitatively differ because of their different definitions. In particular, it can be straightforwardly derived that the SS in electron conduction is equal to $S_{G,e}/\log_{10}(e)$.

For the electron-only channel current to be completely specified, one must also find its expression for $V_{GS,e} < V_{FB}$. Unfortunately, this cannot be derived from experimental data, as hole conduction takes place for $V_{GS,e} < V_{FB}$ (vide infra), swamping the minute electron current in this region. From basic physical considerations, however, it can be expected that electrons can be injected into the carbon nanotubes even in this bias region. Indeed, large longitudinal fields (*i.e.*, large $V_{DS,e}$) could still allow electrons to overcome the unfavorable energy barrier at the interface between the sc-SWCNTN and the source/drain electrode. Additionally, for a given $V_{DS,e}$, electron injection is expected to be progressively reduced as the gate voltage moves farther below V_{FB}. Following this reasoning and in continuity with Eq. S6, we therefore postulate that the electron current for $V_{GS,e} < V_{FB}$ takes the same form as Eq. S6. Therefore, regardless of the specific $V_{GS,e}$ value, the electron-only deep-subthreshold current reads:

$$I_e = I_{0,e} \cdot \left(1 - e^{-\frac{V_{DS,e}}{S_{D,e}}}\right) \cdot e^{\frac{V_{GS,e} - V_{FB}}{S_{G,e}}} \qquad \text{(S7)}$$

While Eq. S7 for $V_{GS,e} < V_{FB}$ cannot be validated against experimental current-voltage data, it is important to note that, for $V_{GS,e} < V_{FB}$, the exponential factor $exp\left(\left(V_{GS,e} - V_{FB}\right)/S_{G,e}\right)$ becomes negligible, and simultaneously the hole-only current rises exponentially (vide infra). Therefore, any deviation of Eq. S7 from the actual electron current for $V_{GS,e} < V_{FB}$ is, in fact, inconsequential with respect to the overall current-voltage characteristics. This is in addition to the merits of Eq. S7 in terms of its close agreement with experimental data for $V_{GS,e} \geq V_{FB}$, its agreement with basic physical intuition for $V_{GS,e} < V_{FB}$, and its compactness and simplicity.

Following the same approach that has led to Eq. S7, it is possible to derive the model equation for hole-only deep-subthreshold conduction starting from the current-voltage plots in **Fig. SF8C-D.** Similar to the electron-only case, the hole-only current can be expressed as:

$$I_h = I_{0,h} \cdot \left(1 - e^{\frac{V_{DS,h}}{S_{D,h}}}\right) \cdot e^{-\frac{V_{GS,h} - V_{FB}}{S_{G,h}}} \quad \text{(S8)}$$

The quantities appearing here are defined similarly to the electron-only case, and the h in all subscripts indicates that the respective quantities refer to hole-only conduction.

Equations S6-S8 indicate that the gate-source and drain-source voltages of our ambipolar TFTs are not uniquely defined, as different labels have been employed to distinguish between their values in the electron-only and hole-only cases. This is due to the ambivalence of the channel electrodes with respect to their role in electron and hole conduction, especially considering that both conduction regimes can occur simultaneously in an ambipolar TFT. In fact, this ambivalence is easily resolved if one considers that electrons are bound to flow towards the channel electrode at higher potential, contrary to the hole case. Thus, if one indicates with X and Y the channel electrodes, it can be easily seen that:

$$V_{DS,e} = |V_X - V_Y|$$
$$V_{DS,h} = -|V_X - V_Y|$$
$$V_{GS,e} = V_G - min(V_X, V_Y)$$
$$V_{GS,h} = V_G - max(V_X, V_Y)$$

Assuming that an electron channel and a hole channel can be formed independently from each other under the appropriate bias conditions, one can then express the total channel current as

$$I_{TOT} = I_e + I_h \quad \text{(S9)}$$

This expression assumes that no significant recombination takes place that affects the carrier densities when both carrier types are present in the channel. While the model could be refined to include carrier recombination, we do not pursue this avenue here for the sake of simplicity and tractability. This is particularly in view of the need to manipulate the current-voltage equations so as to derive the salient properties of ambipolar subthreshold circuits. In fact, considering that the impact of recombination is only expected in a narrow region around the ZTP, the conclusions that will be derived on the basis of Eq. S7-S9 are not affected. As shown in **SI8c**, **SI8d**, **SI8e**, and **SI8f**, it is the electron-only and hole-only regimes that primarily determine the voltage transfer characteristics (VTCs) of high-performance ambipolar deep-subthreshold circuits, and that dictate their minimum supply voltage and their power dissipation. Therefore, the model equations presented here adequately match the purpose of this work, and simultaneously offer a good compromise between accuracy and simplicity.

Finally, we note that the model equations we have derived are in good agreement with the overall experimental deep-subthreshold characteristics of our sc-SWCNTN TFTs, *e.g.*, as shown in (**SI11**) for both C_{18}-PA and FC_{17}-PA devices. The ability of our model equations to follow experimental

deep-subthreshold current-voltage characteristics is also confirmed when building on such equations to simulate inverter VTCs and power consumption (**SI12**).

SI8b. V_{FB} versus ZTP

On the basis of our model equations (Eq. S7-S9), the ZTP of a sc-SWCNTN TFT can be estimated as the intersection point between the extrapolated electron-only and hole-only currents for a given drain-source bias $\overline{V_{DS}} = V_{DS,e} = -V_{DS,h}$. For instance, for $\overline{V_{DS}} > 0V$:

$$I_{TOT}\left(V_{DS,e} = \overline{V_{DS}}\right) \cong I_e\left(V_{DS,e} = \overline{V_{DS}}\right) = I_{0,e} \cdot \left(1 - e^{-\frac{\overline{V_{DS}}}{S_{D,e}}}\right) \cdot e^{\frac{V_G - V_{FB}}{S_{G,e}}} \tag{S10}$$

$$I_{TOT}\left(V_{DS,h} = -\overline{V_{DS}}\right) \cong I_h\left(V_{DS,h} = -\overline{V_{DS}}\right) = I_{0,h} \cdot \left(1 - e^{-\frac{\overline{V_{DS}}}{S_{D,h}}}\right) \cdot e^{-\frac{V_G - \overline{V_{DS}} - V_{FB}}{S_{G,h}}} \tag{S11}$$

The ZTP corresponds to the gate voltage at which the two currents are equal:

$$I_{0,e} \cdot \left(1 - e^{-\frac{\overline{V_{DS}}}{S_{D,e}}}\right) \cdot e^{\frac{ZTP - V_{FB}}{S_{G,e}}} = I_{0,h} \cdot \left(1 - e^{-\frac{\overline{V_{DS}}}{S_{D,h}}}\right) \cdot e^{-\frac{ZTP - \overline{V_{DS}} - V_{FB}}{S_{G,h}}} \tag{S12}$$

While Eq. S12 is generally applicable for $\overline{V_{DS}} > 0V$, it is insightful to consider the following two limiting cases, which lead to simple expressions for ZTP. Firstly, if $\overline{V_{DS}} \ll S_{D,e}, S_{D,h}$, then the following approximate expression is valid:

$$ZTP \cong V_{FB} + \frac{r}{1+r} \cdot \overline{V_{DS}} + S_{G,h} \frac{r}{1+r} ln\left(\frac{I_{0,h}}{I_{0,e}} \frac{S_{D,e}}{S_{D,h}}\right) \tag{S13}$$

where $r = S_{G,e}/S_{G,h}$.
Secondly, if $\overline{V_{DS}} \gg S_{D,e}, S_{D,h}$, then then following approximate expression is valid:

$$ZTP \cong V_{FB} + \frac{r}{1+r} \cdot \overline{V_{DS}} + S_{G,h} \frac{r}{1+r} ln\left(\frac{I_{0,h}}{I_{0,e}}\right) \tag{S14}$$

Equations S13 and S14 show that ZTP is bias dependent and not equal to V_{FB}. Consequently, when comparing TFTs that differ not only in V_{FB} but also in other device parameters (*i.e.*, current prefactors and subthreshold slopes), differences in ZTP between such transistors would not precisely match the differences in the corresponding V_{FB} values.

SI8c. ***Gain of Ambipolar Deep-Subthreshold sc-SWCNTN Inverters***

The gain of an ambipolar deep-subthreshold sc-SWCNTN inverter relates to the slope of its VTC for $V_{IN} = V_{OUT} = V_{TH}$, where V_{TH} is the switching threshold. For transistors with suitably balanced electron and hole subthreshold regimes, this occurs when the pull-down (PD) transistor (transistor with one of its channel electrodes connected to the lower power rail) operates in electron-only deep-subthreshold ($V_{GS,e} \gg V_{FB}$), and the pull-up (PU) transistor (transistor with one of its channel electrodes connected to the higher power rail) operates in hole-only subthreshold ($V_{GS,h} \ll V_{FB}$). Under such conditions, the currents in the two transistors read:

$$I_{PD} = I_{0,e} \cdot \left(1 - e^{-\frac{V_{DS,e}}{S_{D,e}}}\right) \cdot e^{\frac{V_{GS,e}-V_{FB}}{S_{G,e}}} \tag{S15}$$

$$I_{PU} = I_{0,h} \cdot \left(1 - e^{\frac{V_{DS,h}}{S_{D,h}}}\right) \cdot e^{-\frac{V_{GS,h}-V_{FB}}{S_{G,h}}} \tag{S16}$$

In order to derive an expression for the inverter gain, we shall firstly focus on the linearized current-voltage relationships for each of the two transistors. If subjected to a small change of its gate voltage, the PD transistor will deliver a current change proportional to its transconductance $g_{m,PD}$ ($g_{m,PD} := dI_{PD}/dV_{GS,e}$):

$$g_{m,PD} = I_{0,e} \cdot \frac{1}{S_{G,e}} \cdot \left(1 - e^{-\frac{V_{DS,e}}{S_{D,e}}}\right) \cdot e^{\frac{V_{GS,e}-V_{FB}}{S_{G,e}}} = \frac{I_{PD}}{S_{G,e}} \tag{S17}$$

If subjected to a small change of its drain voltage, the PD transistor will deliver a current change inversely proportional to its output resistance $r_{0,PD}$ ($r_{0,PD} := dV_{DS,e}/dI_{PD}$):

$$r_{0,PD} = \left(I_{0,e} \cdot \frac{1}{S_{D,e}} \cdot e^{-\frac{V_{DS,e}}{S_{D,e}}} \cdot e^{\frac{V_{GS,e}-V_{FB}}{S_{G,e}}}\right)^{-1} = \frac{S_{D,e}}{I_{PD}}\left(e^{\frac{V_{DS,e}}{S_{D,e}}} - 1\right) \tag{S18}$$

By applying the same definitions to the PU transistor, one can express its transconductance and output resistance as:

$$g_{m,PU} = \frac{I_{PU}}{S_{G,h}} \tag{S19}$$

$$r_{0,PU} = \frac{S_{D,h}}{I_{PU}}\left(e^{-\frac{V_{DS,h}}{S_{D,h}}} - 1\right) \tag{S20}$$

As the currents in the two transistors are equal to each other, the gain can then be expressed as

$$G = \left(g_{m,PD} + g_{m,PU}\right) \cdot \left({r_{0,PD}}^{-1} + {r_{0,PU}}^{-1}\right)^{-1} \tag{S21}$$

By plugging in Eq. S17-S20 into Eq. S21, and by taking into account that $V_{DS,e} = V_{TH}$, $V_{DS,h} = V_{TH} - V_{DD}$, and $V_G = V_{IN}$, the expression for the gain of an ambipolar inverter in deep-subthreshold can be found.

A noteworthy case is that in which $S_{G,e} = S_{G,h} = S_G$, $S_{D,e} = S_{D,h} = S_D$, $I_{0,e} = I_{0,h} = I_0$, and $V_{FB} = 0\ V$ (perfectly balanced deep-subthreshold ambipolarity), where S_G, S_D, and I_0 are constants. Under these conditions, $g_{m,PD} = g_{m,PU}$, and $r_{0,PD} = r_{0,PU}$, hence $G = g_{m,PD} r_{0,PD} = g_{m,PU} r_{0,PU}$. In other words, perfectly balanced deep-subthreshold ambipolarity leads to a gain equal to the intrinsic gain of the component transistors. In turn, the intrinsic gain can be expressed as

$$G_0 = \frac{S_D}{S_G}\left(e^{\frac{V_{TH}}{S_D}} - 1\right) \tag{S22}$$

Considering that $V_{TH} = V_{DD}/2$ for perfectly balanced deep-subthreshold ambipolarity, the corresponding gain can be further written as

$$G = \frac{S_D}{S_G}\left(e^{\frac{V_{DD}}{2S_D}} - 1\right) \tag{S23}$$

This evidences that the gain increases exponentially with the supply voltage, as this approaches the upper bound of the deep-subthreshold region. Additionally, this relationship shows that the inverter gain can be increased by reducing the subthreshold slopes. While this formula captures the case of perfectly balanced deep-subthreshold ambipolarity, in fact, the trends that emerge from Eq. S23 generally hold, as evidenced, *e.g.*, by inverter simulations at variable V_{DD} based on model fits of experimental data (**SI10**) and also by our experimental data (**SI18**).

SI8d. ***Minimum Supply Voltage of Ambipolar Deep-Subthreshold Circuits***

Transistor circuits of variable complexity may present different requirements on the minimum supply voltage at which they can operate. Notwithstanding, a fitting benchmark that enables the comparison of the supply voltage requirements across technologies is represented by the minimum supply voltage $V_{DD,min}^{(inv)}$ required by the most basic logic gate of all, the inverter. Indeed, the supply voltage required by circuits of a given transistor technology scale with $V_{DD,min}^{(inv)}$. Consequently, with the aim of assessing the supply voltage requirements of our ambipolar deep-subthreshold technology, in the following we focus our analysis on the inverter case.

Obtaining the $V_{DD,min}^{(inv)}$ of our ambipolar deep-subthreshold technology means determining the smallest V_{DD} at which one such inverter possesses positive noise margins (*minimum functionality criterion*). For these to be attained, first the key voltage levels underlying the definitions of noise margins must be well-defined. In turn, this translates into the requirement that the inverter VTC deliver a gain greater than unity. Provided that this condition is met, positive noise margins then immediately follow from a symmetric VTC, which can be realized through balanced ambipolar deep-subthreshold current-voltage (I-V) characteristics. The latter can be achieved to a great extent through a methodology that enables the fine-tuning of the symmetry of the I-V characteristics—*e.g.*, the SAM nanodielectrics presented in this study. All things considered, having a gain greater than unity is the absolute prerequisite that must be evaluated when determining $V_{DD,min}^{(inv)}$.

To determine $V_{DD,min}^{(inv)}$, the most direct route is to solve the inequality $G > 1$, with G expressed as a function of all relevant quantities. In general, this can be done by using the full gain expression in Eq. S21. However, in order to pinpoint the key trends, it is more insightful to carry out this analysis under the working assumption of perfectly balanced deep-subthreshold ambipolarity ($S_{G,e} = S_{G,h} = S_G$, $S_{D,e} = S_{D,h} = S_D$, $I_{0,e} = I_{0,h} = I_0$, where S_G, S_D, and I_0 are constants, and $V_{FB} = 0\ V$). This enables one to use Eq. S23 which translates the inequality $G > 1$ into

$$V_{DD} > 2 \cdot S_D \cdot \ln\left(\frac{S_G}{S_D} + 1\right) \tag{S24}$$

Considering that in many instances $S_D \cong S_G$, this implies that $V_{DD,min}^{(inv)}$ is of the order of S_D. Therefore, the key limit on the supply voltage of an ambipolar deep-subthreshold technology is set by its finite subthreshold slopes. This additionally implies that a reduction of the supply voltage can be achieved through the minimization of the TFT subthreshold slopes.

SI8e. ***VTC Endpoints of an Ambipolar Deep-Subthreshold Inverter***

In the following we derive the output voltages of an ambipolar inverter operating in deep subthreshold for $V_{IN} = V_{DD}$ ($V_{OUT} = V_{OUT,m}$) and $V_{IN} = 0\ V$ ($V_{OUT} = V_{OUT,M}$). These voltages closely relate to V_{OL} and V_{OH} (*i.e.*, the output voltage for low input and the output voltage for high input, respectively), which are key quantities underlying the noise margins[11]. As a working hypothesis, we consider the case such that $V_{FB} \ll S_{G,e}, S_{G,h}$ ($i.e., V_{FB} \cong 0\ V$), which enables us to develop simple analytical expressions for the quantities of interest.
Let us first consider the situation in which $V_{IN} = V_{DD}$. This implies that the transistors are operating in electron-only deep subthreshold, the pull-down transistor (see **SI8c** for definition) being traversed by a current

$$I_{PD} = I_{0,e} \cdot \left(1 - e^{-\frac{V_{OUT,m}}{S_{D,e}}}\right) \cdot e^{\frac{V_{DD}}{S_{G,e}}} \tag{S25}$$

and the pull-up transistor (see **SI8c** for definition) delivering a current

$$I_{PU} = I_{0,e} \cdot \left(1 - e^{-\frac{V_{DD}-V_{OUT,m}}{S_{D,e}}}\right) \cdot e^{\frac{V_{DD}-V_{OUT,m}}{S_{G,e}}} \tag{S26}$$

As the two currents must be equal, the following relationship holds:

$$\left(1 - e^{-\frac{V_{OUT,m}}{S_{D,e}}}\right) = \left(1 - e^{-\frac{V_{DD}-V_{OUT,m}}{S_{D,e}}}\right) \cdot e^{-\frac{V_{OUT,m}}{S_{G,e}}} \tag{S27}$$

Under the assumption (which can be verified a posteriori) that $V_{DD} - V_{OUT,m} \gg S_{D,e}$, Eq. S27 can be approximated as:

$$1 - e^{-\frac{V_{OUT,m}}{S_{D,e}}} \cong e^{-\frac{V_{OUT,m}}{S_{G,e}}} \tag{S28}$$

By solving this equation, one can therefore determine $V_{OUT,m}$. For an order-of-magnitude assessment, it is helpful to note that in many cases $S_{D,e} \cong S_{G,e}$, which allows us to further simplify Eq. S28. Indeed, by setting $S_e = S_{G,e} = S_{D,e}$, we find:

$$V_{OUT,m} \cong S_e \cdot \ln 2 \tag{S29}$$

Similar calculations applied to the situation in which $V_{IN} = 0\ V$ lead us to the following expression for $V_{OUT,M}$ (under the assumption that $V_{OUT,M} \gg S_{D,h}$):

$$1 - e^{-\frac{V_{DD}-V_{OUT,M}}{S_{D,h}}} \cong e^{-\frac{V_{DD}-V_{OUT,M}}{S_{G,h}}} \tag{S30}$$

Finally, an order-of-magnitude assessment of $V_{OUT,M}$ is enabled by considering $S_{G,h} \cong S_{D,h} = S_h$, which leads to:

$$V_{OUT,M} \cong V_{DD} - S_h \cdot \ln 2 \quad \text{(S31)}$$

Equations S29 and S31 indicate that $V_{OUT,M}$ and $V_{OUT,m}$ are about half a subthreshold slope away from the nearest power rail. Such estimates are consistent not only with simulations (**SI12**) but also with experimental inverter data (**Fig. 3**). Finally, Eq. S29 and Eq. S31 reinforce the attractiveness of steep subthreshold slopes so as to achieve ambipolar deep-subthreshold circuits approaching a rail-to-rail output swing.

SI8f. ***Static Power Dissipation of Ambipolar Deep-Subthreshold Circuits***

In order to assess the power dissipation limits of ambipolar deep-subthreshold circuits, it is insightful to refer to the inverter case, which represents a key benchmark circuit. In our analysis, we will consider the working assumption of perfectly balanced deep-subthreshold ambipolarity ($S_{G,e} = S_{G,h} = S_G$, $S_{D,e} = S_{D,h} = S_D$, $I_{0,e} = I_{0,h} = I_0$, and $V_{FB} = 0\ V$) so as to keep the equations compact and thus capture the key trends. Additionally, we shall consider $S_D \cong S_G = S$, as this approximately holds in many circumstances.

Due to the monotonic rise in the transistor current as the VTC endpoints are reached, the maximum static power dissipation of an ambipolar deep-subthreshold inverter occurs at $V_{IN} = V_{DD}$ ($V_{OUT} = V_{OUT,m}$) and $V_{IN} = 0\ V$ ($V_{OUT} = V_{OUT,M}$). Therefore, we can refer to our endpoint estimates (Eq. S29 and Eq. S31) to determine the power dissipation limits. For instance, at $V_{IN} = V_{DD}$, $V_{OUT} \cong S \cdot \ln 2$, while the inverter current can be approximated as:

$$I_{inv}(V_{IN} = V_{DD}) \cong \frac{1}{2} \cdot I_0 \cdot e^{\frac{V_{DD}}{S}} \tag{S32}$$

Along similar lines, it is straightforward to derive that the current flowing through the inverter at $V_{IN} = 0\ V$ ($V_{OUT} = V_{OUT,M}$) can be equally approximated as Eq. S32.

This yields the following estimate for the maximum static power dissipation in a perfectly balanced ambipolar deep-subthreshold inverter:

$$P_{s,MAX} \cong \frac{V_{DD}}{2} \cdot I_0 \cdot e^{\frac{V_{DD}}{S}} \tag{S33}$$

Consequently, static power dissipation relates to the supply voltage with a predominantly exponential relationship. Additionally, it grows exponentially as the subthreshold slope is reduced.

In view of the monotonic rise in static power dissipation with the supply voltage, the minimum power dissipation in an ambipolar deep-subthreshold inverter is achieved when operating at the lowest supply voltage possible. Returning to our estimate of $V_{DD,min}^{(inv)}$ (Eq. S24) and under the assumptions considered here, we find that

$$\min_{V_{DD}} P_{s,MAX} \cong 4 \ln 2 \cdot S \cdot I_0 \tag{S34}$$

This indicates that, within an ambipolar deep-subthreshold technology, power dissipation can be reduced by employing transistors with steep subthreshold slopes, provided that the supply voltage is scaled down accordingly. As an order of magnitude assessment of the power dissipation achievable with our FC_{17}-PA TFTs, substituting the fit parameter values (derived from experimental TFT data) in Eq. S34 leads to an estimated minimum power dissipation in the $10^{-15}\ W/\mu m$ range. In fact, this is in line with the simulated and experimental power dissipation data (**Fig. 2d** and **Fig. 3e**).

SI9. Device stability

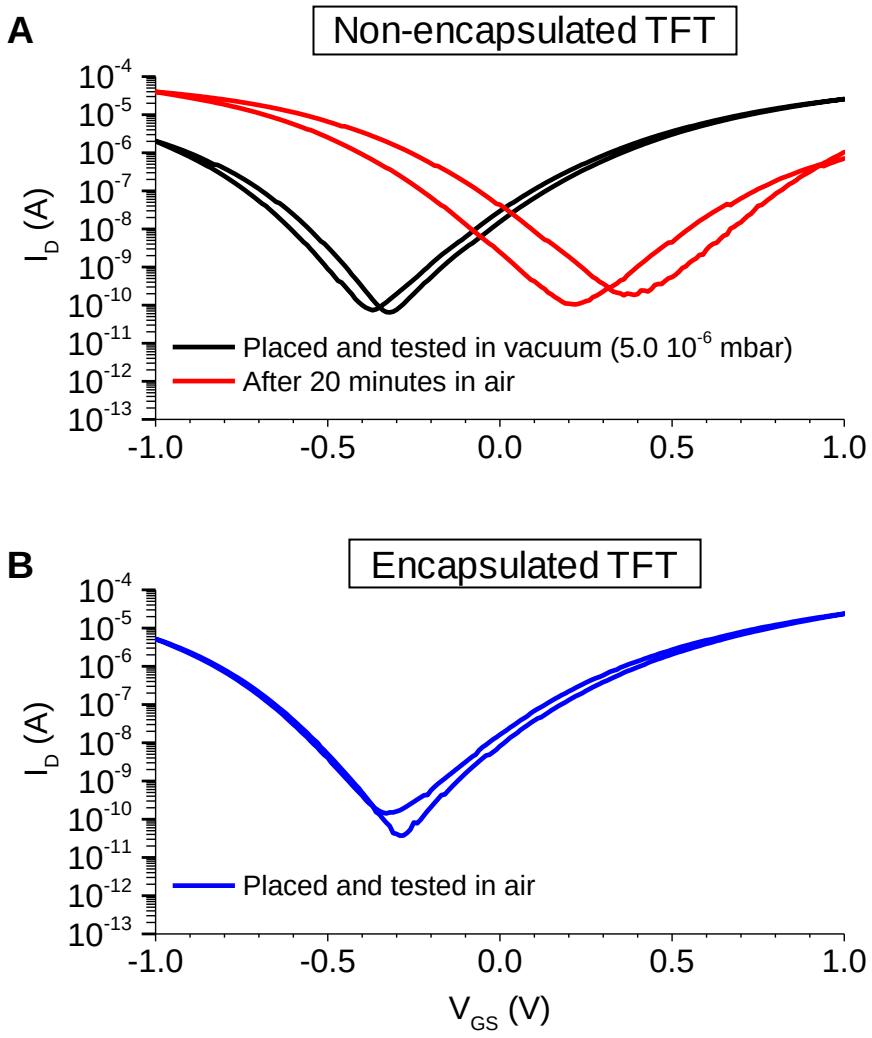


Fig. SF9. Impact of encapsulation on ambipolar deep-subthreshold sc-SWCNTN TFT performance. Here we compare the transfer characteristics of two TFTs (both featuring a C_{18}-PA SAM nanodielectric, W_{ch} / L_{ch} = 1000 μm/20 μm, V_{DS} = -0.25 V) that are nominally identical except for their encapsulation: the device in (**A**) is not encapsulated, while the device in (**B**) is coated with a polymer layer. Prior to testing, the non-encapsulated device was annealed inside a nitrogen-filled glovebox at 200 °C for 3 h. After annealing, the sample was loaded (within the glovebox) into a compact and portable UHV chamber. Upon sealing it, the UHV chamber was transferred outside the glovebox and was subsequently evacuated with a turbomolecular pump to a pressure of $5.0 \cdot 10^{-6}$ mbar. Transfer characteristics were then acquired from the non-encapsulated device in vacuum—black trace in (A). As this sample had undergone hard prolonged annealing in an inert atmosphere and had not been exposed to air before and during electrical testing, the corresponding transfer characteristic constitutes a reference on the inherent behavior of C_{18}-PA SAM TFTs. For the sake of comparison, the transfer characteristic of the encapsulated device, placed and tested in air after fabrication, is shown in (B). This trace exhibits an excellent match—within the reproducibility tolerances of our process—with the trace acquired from the non-

encapsulated device in vacuum. This evidences that our encapsulant has no effect on the inherent behavior of sc-SWCNTN TFTs. In fact, the encapsulant robustly protects the TFTs from air species, which would otherwise have a profound impact on their characteristics. This is shown by the red trace in (A) acquired 20 min after removing the non-encapsulated device from the UHV chamber. A dramatic shift in its transfer characteristic and a large hysteresis are observed, to an extent that it would prevent its use for ambipolar deep-subthreshold circuits. By contrast, notwithstanding its being placed and tested in air, the encapsulated device behaves just as the non-encapsulated counterpart in vacuum (B). This allows us to conclude that our encapsulant is not only inert but also essential to preserve the inherent properties of our sc-SWCNTN TFTs, which underlie their use in ambipolar deep-subthreshold circuits.

SI10. Simulation of an ambipolar deep-subthreshold inverter at variable V_{DD}

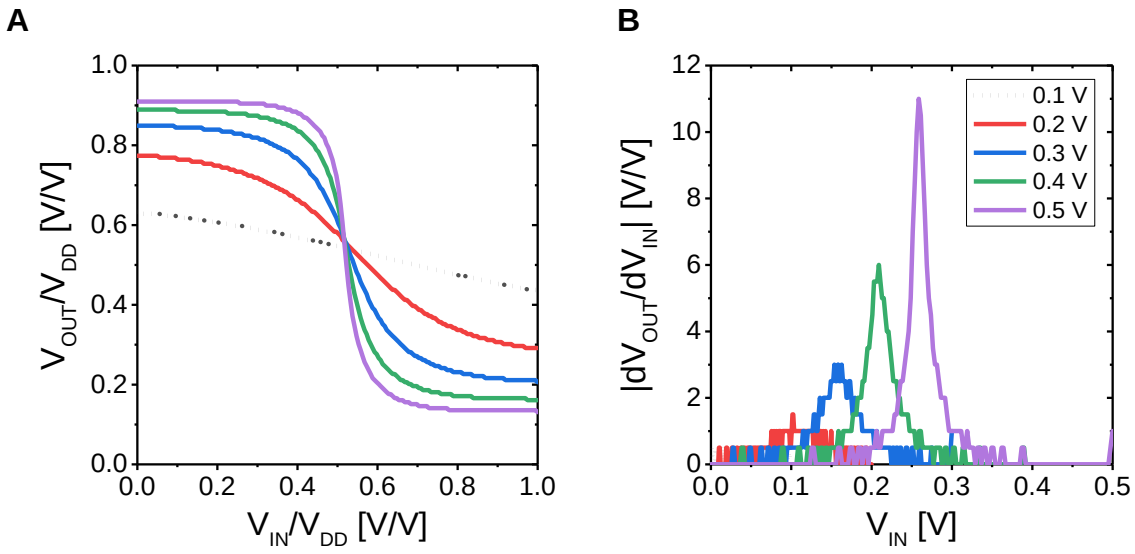


Fig. SF10. Simulation of an ambipolar deep-subthreshold FC_{17}-PA sc-SWCNTN inverter at variable V_{DD}. (**A**) Normalized VTCs of an FC_{17}-PA sc-SWCNTN inverter at variable V_{DD}. The simulation relies on model fits of experimental FC_{17}-PA sc-SWCNTN TFT characteristics (as per equations in **SI8a**). These simulations are able to capture the fact that the output swings as a fraction of V_{DD} drops as V_{DD} is reduced. This is consistent with our analytical derivation that the distance between the VTC endpoints and the voltage rails is approximately constant ($\approx S_{e,h}$, see **SI8e**). In particular, while all solid traces ($V_{DD} \geq 0.2$ V) give a gain greater than unity, the dotted trace ($V_{DD} = 0.1$ V) corresponds to a non-functional inverter (gain < 1). (**B**) Gain at variable V_{DD} as a function of V_{IN}, as calculated from the VTCs in (A). This plot is consistent with our analytical derivation that the gain increases exponentially with V_{DD} (**SI8c**). Additionally, this plot shows that the gain becomes smaller than unity below $V_{DD} = 0.2$ V. This is consistent with our experimental finding that our ambipolar deep-subthreshold inverters can function down to approximately $V_{DD} = 0.2$ V (**Fig. 3e**).

SI11. Experimental and modeled ambipolar deep-subthreshold characteristics

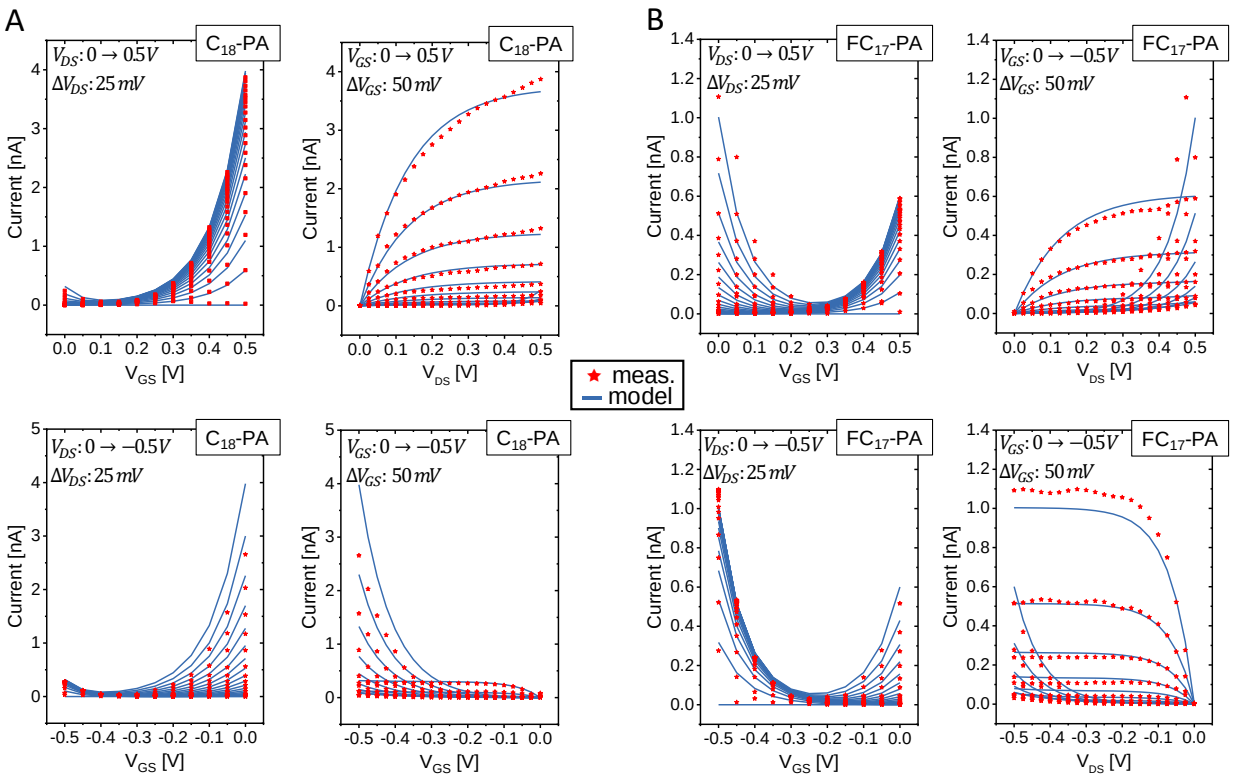


Fig. SF11. Experimental and modeled ambipolar deep-subthreshold characteristics of a C_{18}-PA TFT and a FC_{17}-PA TFT. (**A**) Transfer and output characteristics of a C_{18}-PA TFT. (**B**) Transfer and output characteristics of an FC_{17}-PA TFT. In both cases, model fits (as per equations in **SI8a**) of the transfer and output characteristics (solid lines) are overlaid on representative experimental data points (stars). The good agreement between measured data and model fits evidences that our model equations are able to capture with good accuracy the key dependences of the deep-subthreshold channel current on the terminal voltages. Consequently, these plots can be regarded as a validation of our analytical derivation of ambipolar deep-subthreshold sc-SWCNTN TFT and circuit behavior (**SI8a**, **SI8b**, **SI8c**, **SI8d**, **SI8e** and **SI8f**).

SI12. Experimental *versus* simulated VTCs

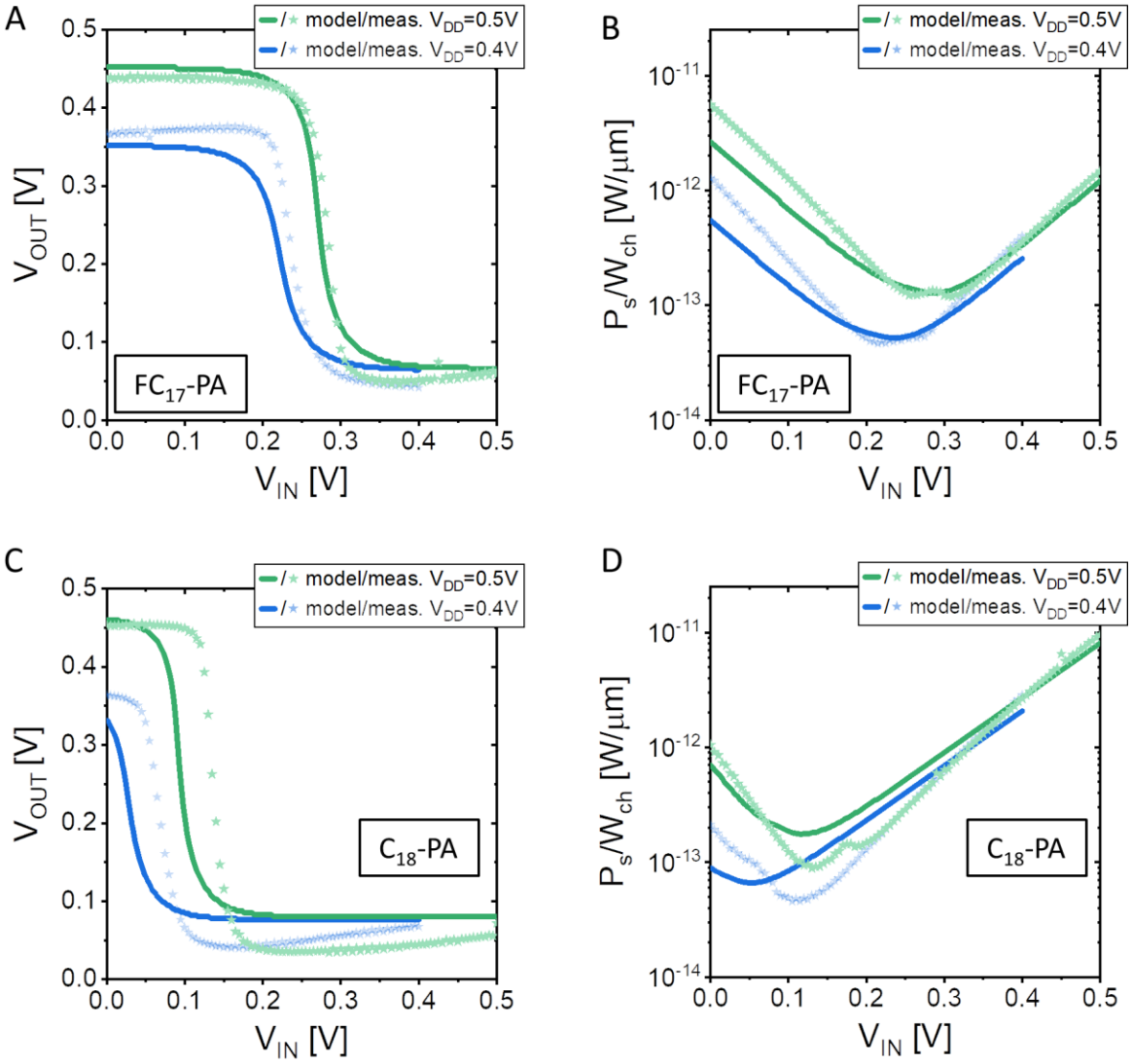


Fig. SF12. Experimental *versus* simulated VTCs and power consumption of ambipolar deep-subthreshold sc-SWCNTN inverters. (**A**) VTCs of a CF_{17}-PA inverter. (**B**) Power consumption of a CF_{17}-PA inverter. (**C**) VTCs of a C_{18}-PA inverter. (**D**) Power consumption of a C_{18}-PA inverter. In all cases, simulations based on model fits of experimental TFT data (as per model equations in **SI8a**) are compared with representative experimental inverter characteristics measured at V_{DD} = 0.4 V and V_{DD} = 0.5 V. The corresponding power consumption is then derived from the simulated inverter current. These plots show that the model equations can capture the observed circuit behavior with good accuracy—indeed, discrepancies are traceable to TFT process parameter variations (see **SI15**). Consequently, this result can be regarded as a validation of the analytical derivations of key circuit performance parameters presented in **SI8c**, **SI8d**, **SI8e** and **SI8f**.

SI13. Impact of a mismatch in the VFB values

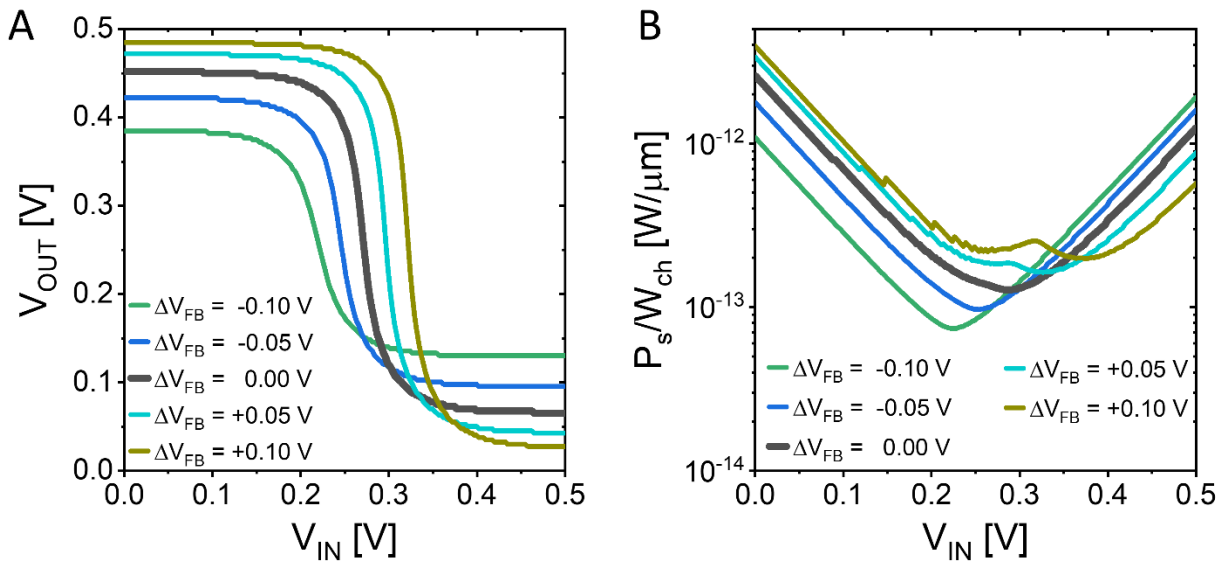


Fig. SF13. Impact of a mismatch in the V_{FB} values of the pull-up and pull-down transistors in an ambipolar deep-subthreshold sc-SWCNTN inverter. Here we show the outcome of the simulation of an inverter based on FC_{17}-PA sc-SWCNTN TFT parameters except for the flatband voltage of the pull-up TFT, which is allowed to vary between -0.1 V and +0.1 V. (**A**) The resulting VTCs show that symmetric behavior is obtained for equal flatband voltages. By contrast, appreciable differences in flatband voltage result in significant VTC asymmetry, which is detrimental to the corresponding noise margins. (**B**) Power dissipation at different values of the V_{FB} mismatch. This plot shows that a large mismatch may also result in an increase in static power dissipation. The findings derived from this simulation relate to the ideal of perfectly balanced deep-subthreshold ambipolar technology (see **SI8c**, **SI8d**, **SI8f**), which comprises the condition V_{FB} = 0 V for all of its transistors.

SI14. Impact of a mismatch in gate subthreshold slopes

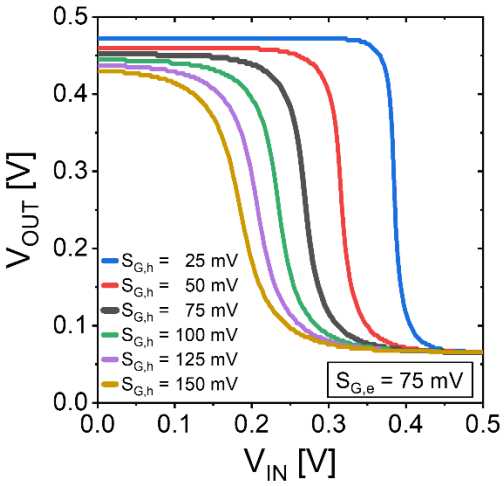


Fig. SF14. Impact of a mismatch in gate subthreshold slopes for electrons and holes on the VTC of an ambipolar deep-subthreshold sc-SWCNTN inverter. Here we show the outcome of the simulation of an inverter based on FC_{17}-PA sc-SWCNTN TFT parameters except for the gate subthreshold slope for holes, which is allowed to vary between 25 mV and 150 mV. The resulting VTCs show that symmetric behavior is obtained for approximately equal gate subthreshold slopes for electrons and holes. By contrast, appreciable differences in gate subthreshold slopes result in significant VTC asymmetry, which inevitably has a negative impact on the corresponding noise margins. Considering that the gate subthreshold slopes for electron and hole in our sc-SWCNTN TFTs are significantly close to each other, this simulation provides insight into their ability to deliver well-conditioned inverters. More generally, the need for balanced deep-subthreshold parameters emerging here relates to the ideal of perfectly-balanced deep-subthreshold ambipolarity, whose attractiveness is discussed in **SI8c** and **SI8d**.

SI15. Impact of gate subthreshold slope variability

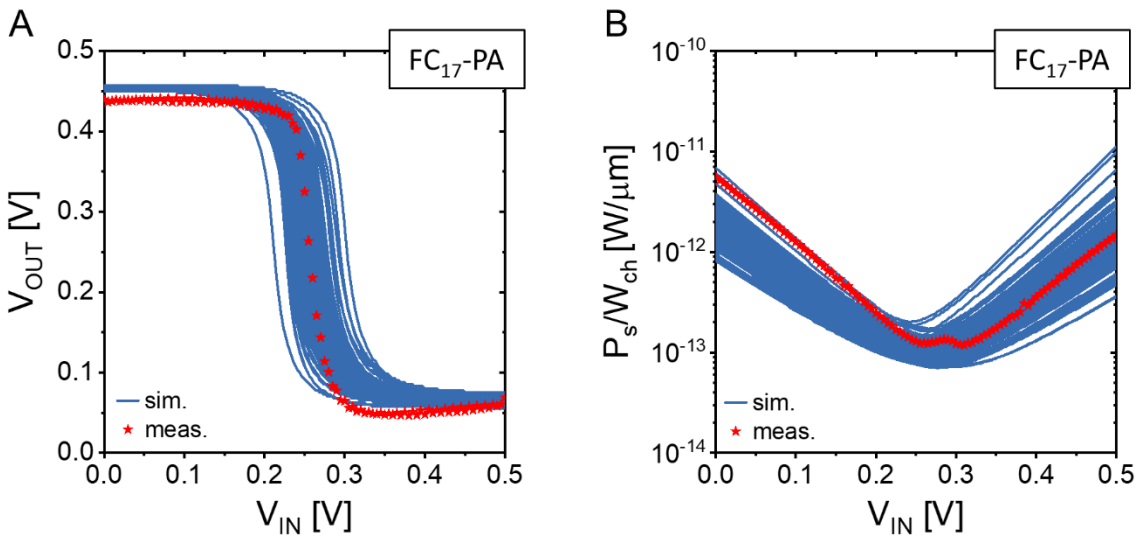


Fig. SF15. Monte Carlo simulation of the impact of gate subthreshold slope variability on the VTCs and power consumption of ambipolar deep-subthreshold sc-SWCNTN inverters. (**A**) VTCs of simulated CF_{17}-PA inverters (blue traces), along with a representative experimental VTC (red trace). (**B**) Power consumption of simulated CF_{17}-PA inverters (blue traces), along with representative experimental power consumption data (red trace). The simulation is based on model fits (as per model equations in **SI8a**) of experimental CF_{17}-PA TFT data, and is conducted at V_{DD} = 0.5 V. The gate subthreshold slopes for electrons and holes of both pull-up and pull-down transistors are allowed to vary randomly according to a Gaussian distribution with standard deviation consistent with experimental data (*e.g.*, see **Fig. 4e**). The resulting characteristics presented here derive from 100 iterations. These plots show that the simulated characteristics are in agreement with experimental data. Additionally, they indicate that the device-to-device variability of our TFTs—inevitable when conducting device fabrication in an academic laboratory—does not impinge on their ambipolar deep-subthreshold circuit operation with ultralow-power characteristics.

SI16. Experimental inverter VTCs at VDD of variable magnitude and polarity

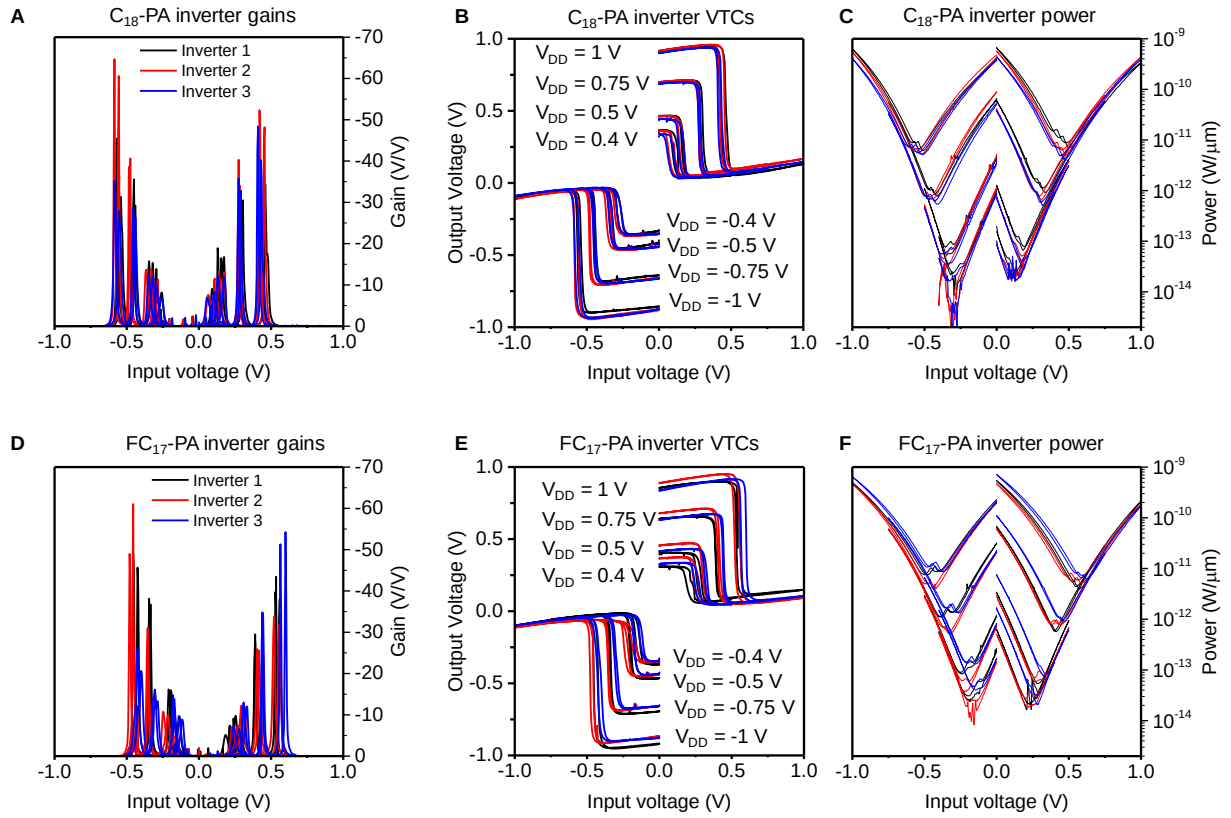


Fig. SF16. Experimental inverter VTCs at V_{DD} of variable magnitude and polarity. These plots display the experimental characteristics of 3 C_{18}-PA inverters and 3 FC_{17}-PA inverters operated at different V_{DD} values. (**A**) Gain of three C_{18}-PA inverters at different V_{DD} values. (**B**) VTCs of the three C_{18}-PA inverters. (**C**) Power consumption of the three C_{18}-PA inverters. (**D**) Gain of three FC_{17}-PA inverters at different V_{DD} values. (**E**) VTCs of the three FC_{17}-PA inverters. (**F**) Power consumption of the three FC_{17}-PA inverters.

SI17. Normalized inverter VTCs at different V_{DD}s

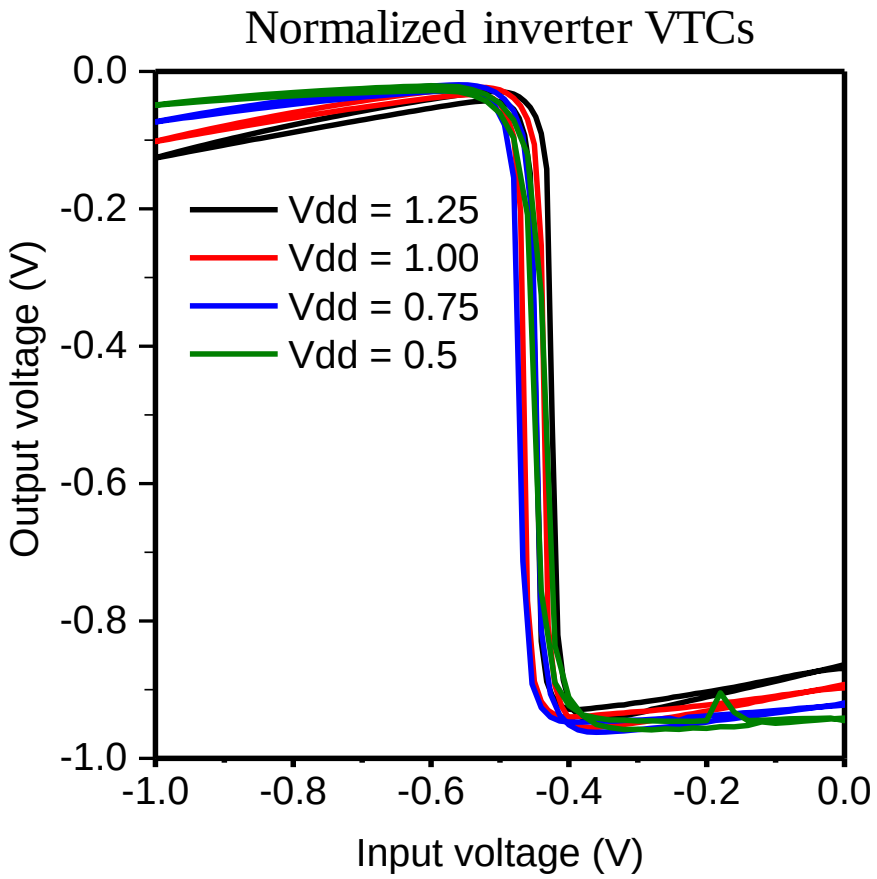


Fig. SF17. Normalized VTCs of a sc-SWCNTN inverter at V_{DD} in the range of 0.5 V to 1.25 V. This plots displays the measured VTCs of an inverter at different V_{DD} values. As the V_{DD} is lowered, the Z-shape feature characteristic of the VTCs of ambipolar inverters is diminished, resulting in VTCs closer to ideal and effectively incrementing the noise margins.

SI18. Experimental VTC, power consumption and gain of an inverter

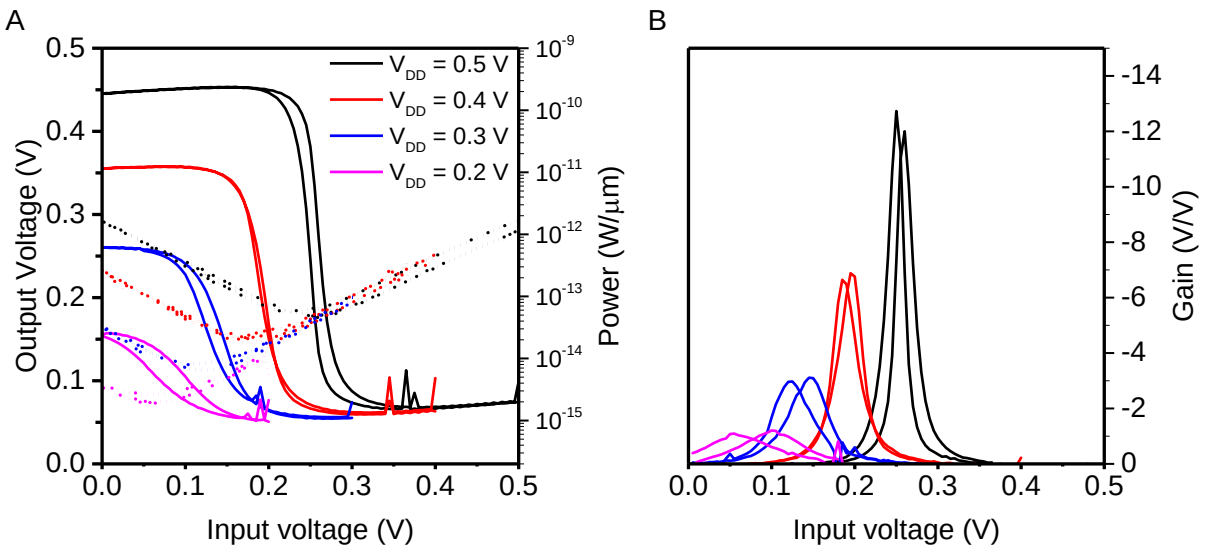


Fig. SF18. VTCs, power dissipation, and gain of an experimental ambipolar deep-subthreshold inverter operated at variable V_{DD}. (**A**) VTCs and power consumption at different V_{DD} values. (**B**) Corresponding gain. This example evidences the importance of VTC symmetry so as to maintain circuit functionality (*i.e.*, gain > 1) down to particularly low supply voltages V_{DD} (0.2 V in this case).

SI19. Impact of the gate subthreshold slope

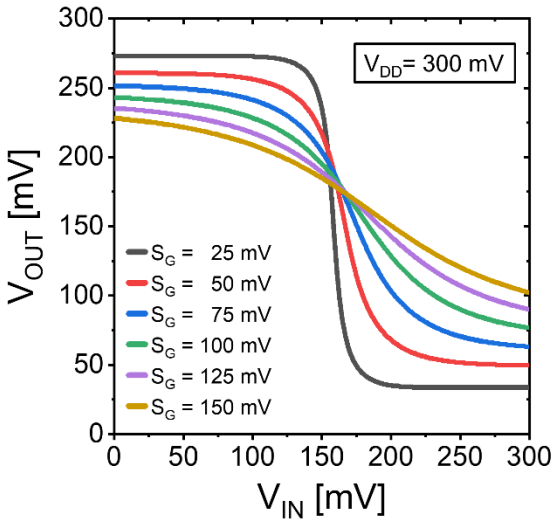


Fig. SF19. Impact of the gate subthreshold slope on VTCs and gain of an ambipolar deep-subthreshold sc-SWCNTN inverter. The simulation is run with V_{DD} set to 0.3 V. The resulting VTCs shown here evidence that a reduction in subthreshold slope delivers an increase in output swing and larger gain, consistently with our analysis in **SI8c** and **SI8e**.

SI20. Scanning electron microscopy

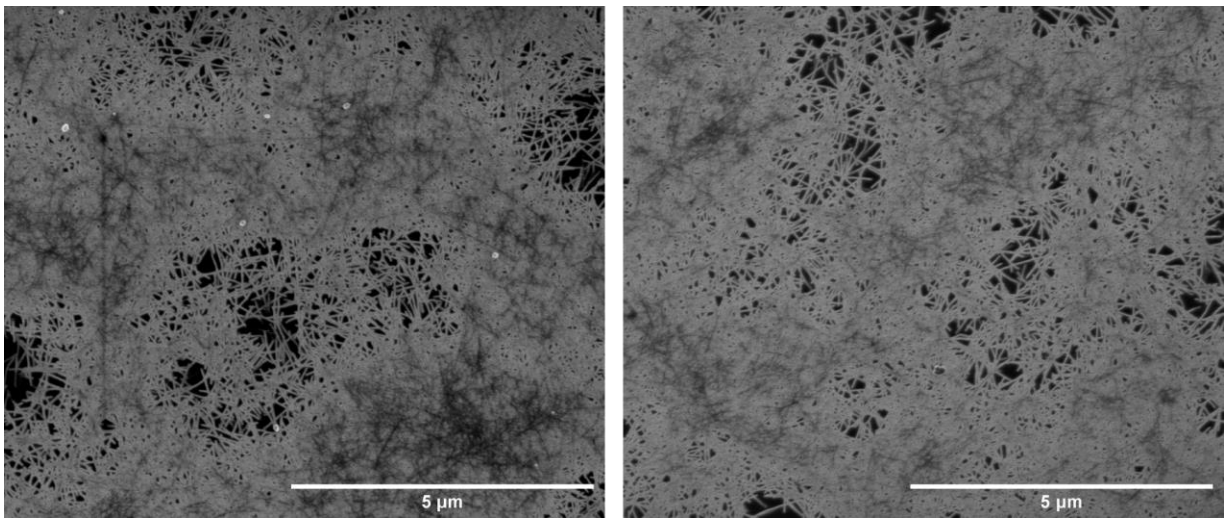


Fig. SF20. SEM images of carbon nanotubes atop a SAM nanodielectric. A dense sc-SWCNT network can be observed after the deposition of the sc-SWCNTN atop SAM-modified nanodielectrics.

SI21. Bias stress

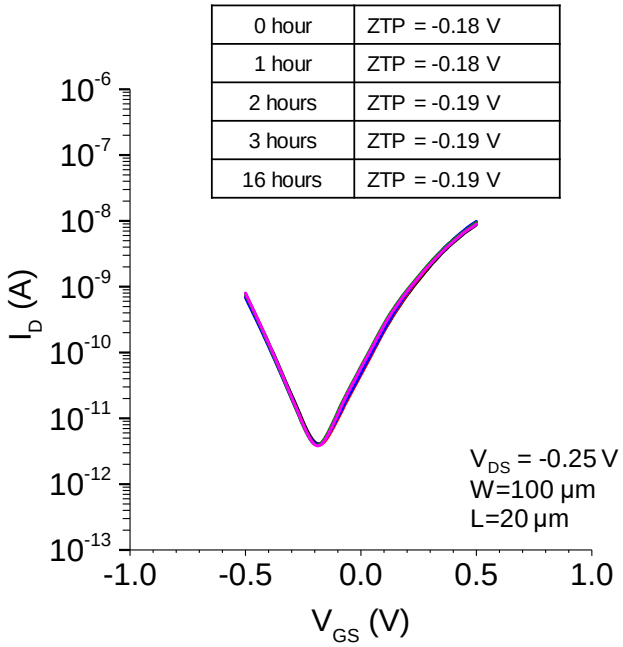


Fig. SF21. Impact of bias stress on TFT characteristics. Transfer curves of a TFT subjected to bias stress (V_{GS} = 0.5 V, V_{DS} = -0.25 V) over a period of 16 hours (inset: corresponding ZTP values).

The stress condition adopted herein was selected in order to reproduce the stress condition that our TFTs experience within a digital gate operating at the maximum proposed V_{DD} of 0.5 V for deep-subthreshold operation. The resulting transfer characteristics are indistinguishable from one another. This is also confirmed by the corresponding ZTP shift, which amounts to only 10 mV. As demonstrated by our detailed study of the effect of device parameter variations on circuit characteristics (SI15), our bias stress experiment shows that the stability of our devices is not expected to hinder the realization of logic circuits based on such devices.

SI.22 Unipolar-like configurations

We have simulated the case of inverters based on two identical transistors of ours connected in unipolar logic manner. In particular, such gates had their load transistors connected in either one of the following configurations, as typical of gates realized in unipolar logic manner: a) diode-connected configuration; b) zero-V_{GS} configuration.
The resulting voltage transfer characteristics and power consumption are shown in the figure below for the case of $V_{DD} = 0.5\ V$. It is apparent that their VTCs do not have any resemblance whatsoever to that of a working inverter. The corresponding power dissipation figures are in the same range as those of our inverters connected in CMOS-like fashion. However, as inverters realized in unipolar manner are not functional, their power dissipation values are not particularly meaningful.

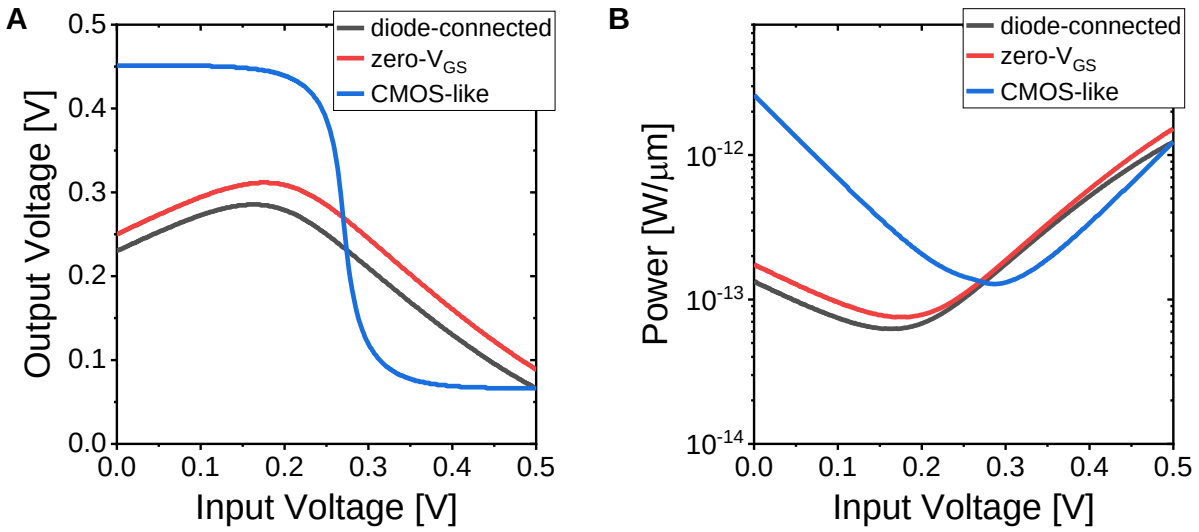


Fig. SF22. Inverters based on TFTs connected in a unipolar logic manner. We have simulated the case of circuits featuring two identical transistors of ours connected in a unipolar logic manner: with a diode-connected load and with a zero-V_{GS} load. **(A)** Simulated VTCs. **(B)** Calculated power consumption. The corresponding case of a complementary-like inverter is also shown here for the sake of comparison.

Table S1.
Summary of the sc-SWCNT TFT performance parameters.

	C_{18}-PA TFTs		FC_{17}-PA TFTs	
	n-channel	*p*-channel	*n*-channel	*p*-channel
Mobility ($cm^2\ V^{-1}\ s^{-1}$)	10.90±0.40	8.24±1.81	8.54±3.78	6.82±2.75
On current (A) (V_{GS} = 2 V or -2 V) (V_{DS} = -0.25 V)	$5.2\cdot10^{-5}$±$9.9\cdot10^{-6}$	$2.6\cdot10^{-5}$±$5.6\cdot10^{-6}$	$3.8\cdot10^{-5}$±$1.9\cdot10^{-5}$	$2.1\cdot10^{-5}$±$9.9\cdot10^{-6}$
Threshold voltage (V)	0.69±0.01	-0.82±0.01	0.78±0.01	-0.78±0.01
On/Off ratio (V_{GS} = 2 V or -2 V) (V_{DS} = -0.25 V)	5.8±0.05	5.5±0.04	6.0±13	5.7±0.1
SS (mV/decade)	138±17	114±7	171±17	150±11
ZTP (V)	-0.30±0.03		-0.13±0.04	
Trap density ($10^{12}\ eV^{-1}\ cm^{-2}$)	3.9	2.5	5.1	3.9

For mobility calculations, please refer to **SI4**.

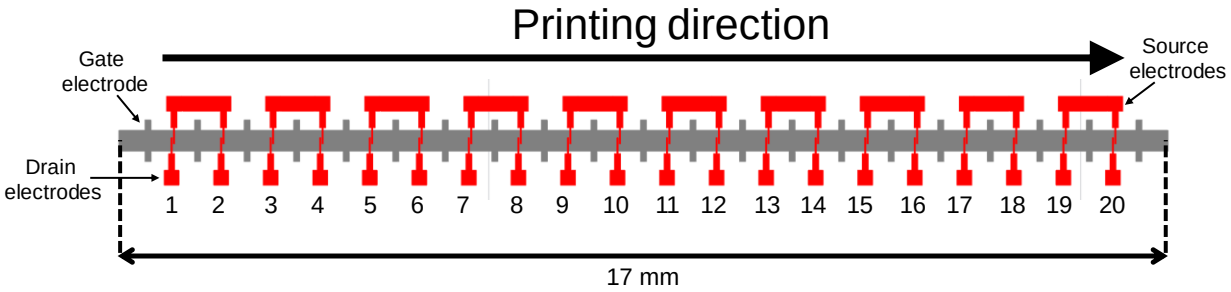
Calculated trap densities as per Eq. S38 for C_{18}-PA and FC_{17}-PA devices.

$$D_{tr} = \frac{C_d}{q}\left(SS\frac{\log(e)}{kT/q} - 1\right) \quad \text{(S38)}$$

Here C_d is the effective capacitance (**Fig. SF2.1**), q is the elementary charge, SS is the average subthreshold swing, k is the Boltzmann's constant, and T is the absolute temperature.

Table S2.

Transistor layout and summary of performance parameters of each transistor based on their physical position and printing order of the sc-SWCNTN. The listed parameters were extracted from transistors based on a FC_{17}-PA nanodielectric.



	Mobility (V_{GS} = 1 V or -1 V) ($cm^2\ V^{-1}\ s^{-1}$)		On current (A) (V_{GS} = 1 V or -1 V) (V_{DS} = -0.25 V)		Threshold voltage (V)		On/Off ratio (V_{GS} = 1 V or -1 V) (V_{DS} = -0.25 V)		SS (mV/decade)		ZTP (V)
	n	*p*	*n*	*p*	*n*	*p*	*n*	*p*	*n*	*p*	
1	$6.5\cdot10^{-2}$	$4.7\cdot10^{-2}$	$2.6\cdot10^{-7}$	$1.8\cdot10^{-7}$	0.76	-0.72	4.7	4.6	148	131	-0.16
2	$5.5\cdot10^{-2}$	$4.4\cdot10^{-2}$	$2.1\cdot10^{-7}$	$1.7\cdot10^{-7}$	0.88	-0.77	4.5	4.4	216	142	-0.16
3	$1.3\cdot10^{-2}$	$4.0\cdot10^{-2}$	$0.5\cdot10^{-7}$	$1.6\cdot10^{-7}$	0.84	-0.63	4.3	4.7	207	133	-0.05
4	$4.7\cdot10^{-2}$	$1.6\cdot10^{-2}$	$1.8\cdot10^{-7}$	$0.6\cdot10^{-7}$	0.76	-0.75	4.6	4.1	172	156	-0.1
5	$6.2\cdot10^{-2}$	$1.3\cdot10^{-2}$	$2.4\cdot10^{-7}$	$0.5\cdot10^{-7}$	0.75	-0.77	5.1	4.4	140	142	-0.17
6	$3.6\cdot10^{-2}$	$2.2\cdot10^{-2}$	$1.4\cdot10^{-7}$	$0.8\cdot10^{-7}$	0.79	-0.81	4.5	4.3	173	159	-0.06
7						Defective					
8						Defective					
9	$3.7\cdot10^{-2}$	$1.6\cdot10^{-2}$	$1.4\cdot10^{-7}$	$0.6\cdot10^{-7}$	0.79	-0.76	4.5	4.2	195	166	-0.13
10	$3.5\cdot10^{-2}$	$2.0\cdot10^{-2}$	$1.3\cdot10^{-7}$	$0.8\cdot10^{-7}$	0.80	-0.76	5.0	4.7	158	136	-0.1
11	$4.5\cdot10^{-2}$	$1.7\cdot10^{-2}$	$1.8\cdot10^{-7}$	$0.6\cdot10^{-7}$	0.77	-0.70	4.7	4.3	171	141	-0.14
12	$3.3\cdot10^{-2}$	$3.1\cdot10^{-2}$	$1.3\cdot10^{-7}$	$1.2\cdot10^{-7}$	0.80	-0.73	4.4	4.4	174	150	-0.04
13	$3.5\cdot10^{-2}$	$2.2\cdot10^{-2}$	$1.4\cdot10^{-7}$	$0.9\cdot10^{-7}$	0.80	-0.73	4.4	4.2	175	156	-0.03
14	$2.3\cdot10^{-2}$	$7.5\cdot10^{-2}$	$0.9\cdot10^{-7}$	$3.0\cdot10^{-7}$	0.84	-0.76	4.7	5.2	162	107	-0.11
15	$3.5\cdot10^{-2}$	$2.0\cdot10^{-2}$	$1.41\cdot10^{-7}$	$0.7\cdot10^{-7}$	0.77	-0.74	4.8	4.6	147	142	-0.06
16	$2.3\cdot10^{-2}$	$7.5\cdot10^{-2}$	$0.9\cdot10^{-7}$	$3.0\cdot10^{-7}$	0.81	-0.77	4.6	5.1	168	118	-0.11
17	$5.6\cdot10^{-2}$	$2.7\cdot10^{-2}$	$2.2\cdot10^{-7}$	$1.0\cdot10^{-7}$	0.79	-0.74	4.9	4.6	146	138	-0.08
18						Defective					
19	$5.4\cdot10^{-2}$	$2.8\cdot10^{-2}$	$2.15\cdot10^{-7}$	$1.1\cdot10^{-7}$	0.75	-0.77	4.6	4.3	170	137	-0.18

20	$3.0\cdot10^{-2}$	$1.4\cdot10^{-2}$	$1.2\cdot10^{-7}$	$0.5\cdot10^{-7}$	0.72	-0.77	4.4	4.1	173	175	-0.14

Table S3.

List of literature works reporting inverter gates (with gain ≥ 1 and with switching threshold between V_{DD} and ground) made with organics, amorphous metal oxides, or sc-SWCNTNs, and that expressly characterize static power consumption. The number of semiconductors and dopants, as well as the number of metals for the injecting electrodes, are also listed here, due to their relevance to material complexity. The listed power consumption figures are the lowest reported in each work.

Ref.	No. of semiconductors and dopants	Source and drain electrode materials	Technology	Lowest V_{DD} (V)	Lowest static power consumption (W)
This work	1	1	Ambipolar CNT	0.2	$1\cdot10^{-12}$
[12]	1	1	Ambipolar CNT	1.5	$1.6\cdot10^{-3}$
[13]	1	1	Ambipolar CNT	0.5	$1\cdot10^{-7}$
[14]	1	1	Ambipolar CNT	2	$2\cdot10^{-4}$
[15]	2	1	Ambipolar CNT	0.25	$9\cdot10^{-9}$
[16]	1	1	Ambipolar CNT	5	$2\cdot10^{-4}$
[17]	1	1	Ambipolar CNT	1	$3\cdot10^{-7}$
[18]	1	2	CMOS CNT	0.1	$4\cdot10^{-12}$
[19]	3	1	CMOS CNT	1	$1.3\cdot10^{-8}$
[20]	2	1	CMOS CNT	0.5	$5\cdot10^{-10}$
[21]	2	1	CMOS CNT	0.8	$5\cdot10^{-11}$
[22]	1	2	CMOS CNT	0.2	$2.4\cdot10^{-10}$
[23]	1	1	Unipolar CNT	2	$2.5\cdot10^{-13}$
[24]	1	1	Unipolar Organic	2	$7\cdot10^{-10}$
[25]	1	1	Unipolar Oxide	2	$3\cdot10^{-10}$
[26]	1	1	Ambipolar Organic	40	$3.6\cdot10^{-4}$
[27]	2	1	CMOS Organic	1.5	$1.5\cdot10^{-10}$
[28]	2	1	CMOS Organic	2	$2\cdot10^{-11}$
[26]	1	1	CMOS Organic	40	$4\cdot10^{-9}$
[29]	2	1	CMOS Organic	0.7	$1\cdot10^{-13}$
[30]	2	1	CMOS Organic	0.9	$2.5\cdot10^{-9}$
[31]	2	1	CMOS Organic	0.6	$6\cdot10^{-10}$
[17]	2	1	CMOS CNT hybrid	1	$2\cdot10^{-9}$
[32]	2	1	CMOS CNT hybrid	0.9	$2.5\cdot10^{-10}$
[33]	2	1	CMOS Organic/Oxide	30	$500\cdot10^{-9}$

Data availability statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References:

(1) Brotherton, S. D. Insulated Gate Field Effect Transistors, IGFETs. In *Introduction to Thin Film Transistors*; Springer International Publishing: Heidelberg, 2013; pp 46–68.

(2) Schießl, S. P.; Gannott, F.; Etschel, S. H.; Schweiger, M.; Grünler, S.; Halik, M.; Zaumseil, J. Self-Assembled Monolayer Dielectrics for Low-Voltage Carbon Nanotube Transistors with Controlled Network Density. *Adv. Mater. Interfaces* **2016**, *3*, 1600215.

(3) Cao, Q.; Xia, M.; Kocabas, C.; Shim, M.; Rogers, J. A.; Rotkin, S. V. Gate Capacitance Coupling of Singled-Walled Carbon Nanotube Thin-Film Transistors. *Appl. Phys. Lett.* **2007**, *90*, 023516.

(4) Khassanov, A.; Steinrück, H.-G.; Schmaltz, T.; Magerl, A.; Halik, M. Structural Investigations of Self-Assembled Monolayers for Organic Electronics: Results from X-Ray Reflectivity. *Acc. Chem. Res.* **2015**, *48*, 1901–1908.

(5) Gholamrezaie, F.; Andringa, A. M.; Roelofs, W. S. C.; Neuhold, A.; Kemerink, M.; Blom, P. W. M.; De Leeuw, D. M. Charge Trapping by Self-Assembled Monolayers as the Origin of the Threshold Voltage Shift in Organic Field-Effect Transistors. *Small* **2012**, *8*, 241–245.

(6) Cahen, D.; Naaman, R.; Vager, Z. The Cooperative Molecular Field Effect. *Adv. Funct. Mater.* **2005**, *15*, 1571–1578.

(7) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. Ultralow-Power Organic Complementary Circuits. *Nature* **2007**, *445*, 745–748.

(8) Nie, H.-Y. Revealing Different Bonding Modes of Self-Assembled Octadecylphosphonic Acid Monolayers on Oxides by Time-of-Flight Secondary Ion Mass Spectrometry: Silicon *vs* Aluminum. *Anal. Chem.* **2010**, *82*, 3371–3376.

(9) Thissen, P.; Valtiner, M.; Grundmeier, G. Stability of Phosphonic Acid Self-Assembled Monolayers on Amorphous and Single-Crystalline Aluminum Oxide Surfaces in Aqueous Solution. *Langmuir* **2010**, *26*, 156–164.

(10) Himmelhaus, M.; Eisert, F.; Buck, M.; Grunze, M. Self-Assembly of n -Alkanethiol Monolayers. A Study by IR−Visible Sum Frequency Spectroscopy (SFG). *J. Phys. Chem. B* **2000**, *104*, 576–584.

(11) Jaeger, R. C.; Blalock, T. N. Introduction to Digital Electronics. In *Microelectronic Circuit Design*; McGraw-Hill: New York, NY, USA, 2011; pp 287–366.

(12) Ha, M.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks. *ACS Nano* **2010**, *4*, 4388–4395.

(13) Xu, W.; Liu, Z.; Zhao, J.; Xu, W.; Gu, W.; Zhang, X.; Qian, L.; Cui, Z. Flexible Logic Circuits Based on Top-Gate Thin Film Transistors with Printed Semiconductor Carbon Nanotubes and Top Electrodes. *Nanoscale* **2014**, *6*, 14891–14897.

(14) Ha, M.; Seo, J. W. T.; Prabhumirashi, P. L.; Zhang, W.; Geier, M. L.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Aerosol Jet Printed, Low Voltage, Electrolyte Gated Carbon Nanotube Ring Oscillators with Sub-5 Ms Stage Delays. *Nano Lett.* **2013**, *13*, 954–960.

(15) Xiao, H.; Xie, H.; Robin, M.; Zhao, J.; Shao, L.; Wei, M.; Portilla, L.; Pecunia, V.; Chen,

S.; Lee, C.; Mo, L.; Cui, Z. Polarity Tuning of Carbon Nanotube Transistors by Chemical Doping for Printed Flexible Complementary Metal-Oxide Semiconductor (CMOS)-Like Inverters. *Carbon* **2019**, *147*, 566–573.

(16) Kim, B.; Geier, M. L.; Hersam, M. C.; Dodabalapur, A. Inkjet Printed Circuits Based on Ambipolar and *P*-Type Carbon Nanotube Thin-Film Transistors. *Sci. Rep.* **2017**, *7*, 39627.

(17) Kim, B.; Jang, S.; Geier, M. L.; Prabhumirashi, P. L.; Hersam, M. C.; Dodabalapur, A. High-Speed, Inkjet-Printed Carbon Nanotube/Zinc Tin Oxide Hybrid Complementary Ring Oscillators. *Nano Lett.* **2014**, *14*, 3683–3687.

(18) Yang, Y.; Ding, L.; Han, J.; Zhang, Z.; Peng, L. M. High-Performance Complementary Transistors and Medium-Scale Integrated Circuits Based on Carbon Nanotube Thin Films. *ACS Nano* **2017**, *11*, 4124–4132.

(19) Schneider, S.; Brohmann, M.; Lorenz, R.; Hofstetter, Y. J.; Rother, M.; Sauter, E.; Zharnikov, M.; Vaynzof, Y.; Himmel, H. J.; Zaumseil, J. Efficient N-Doping and Hole Blocking in Single-Walled Carbon Nanotube Transistors with 1,2,4,5-Tetrakis(Tetramethylguanidino)Ben-Zene. *ACS Nano* **2018**, *12*, 5895–5902.

(20) Zhang, X.; Zhao, J.; Dou, J.; Tange, M.; Xu, W.; Mo, L.; Xie, J.; Xu, W.; Ma, C.; Okazaki, T.; Cui, Z. Flexible CMOS-Like Circuits Based on Printed *P*-Type and *N*-Type Carbon Nanotube Thin-Film Transistors. *Small* **2016**, *12*, 5066–5073.

(21) Geier, M. L.; Prabhumirashi, P. L.; McMorrow, J. J.; Xu, W.; Seo, J. W. T.; Everaerts, K.; Kim, C. H.; Marks, T. J.; Hersam, M. C. Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control. *Nano Lett.* **2013**, *13*, 4810–4814.

(22) Zhang, H.; Xiang, L.; Yang, Y.; Xiao, M.; Han, J.; Ding, L.; Zhang, Z.; Hu, Y.; Peng, L. M. High-Performance Carbon Nanotube Complementary Electronics and Integrated Sensor Systems on Ultrathin Plastic Foil. *ACS Nano* **2018**, *12*, 2773–2779.

(23) Xiang, L.; Zhang, H.; Dong, G.; Zhong, D.; Han, J.; Liang, X.; Zhang, Z.; Peng, L. M.; Hu, Y. Low-Power Carbon Nanotube-Based Integrated Circuits That Can Be Transferred to Biological Surfaces. *Nat. Electron.* **2018**, *1*, 237–245. https://doi.org/10.1038/s41928-018-0056-6.

(24) Jiang, C.; Choi, H. W.; Cheng, X.; Ma, H.; Hasko, D.; Nathan, A. Printed Subthreshold Organic Transistors Operating at High Gain and Ultralow Power. *Science* **2019**, *363*, 719–723.

(25) Lee, S.; Nathan, A. Subthreshold Schottky-Barrier Thin-Film Transistors with Ultralow Power and High Intrinsic Gain. *Science* **2016**, *354*, 302–304.

(26) Nakano, M.; Osaka, I.; Takimiya, K. Control of Major Carriers in an Ambipolar Polymer Semiconductor by Self-Assembled Monolayers. *Adv. Mater.* **2017**, *29*, 1602893.

(27) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. Ultralow-Power Organic Complementary Circuits. *Nature* **2007**, *445*, 745–748.

(28) Zschieschang, U.; Ante, F.; Schlörholz, M.; Schmidt, M.; Kern, K.; Klauk, H. Mixed Self-Assembled Monolayer Gate Dielectrics for Continuous Threshold Voltage Control in Organic Transistors and Circuits. *Adv. Mater.* **2010**, *22*, 4489–4493.

(29) Zschieschang, U.; Bader, V. P.; Klauk, H. Below-One-Volt Organic Thin-Film Transistors with Large on/off Current Ratios. *Org. Electron.* **2017**, *49*, 179–186.

(30) Ke, T. H.; Myny, K.; Chasin, A.; Müller, R.; Heremans, P.; Steudel, S. Ultralow Power Transponder in Thin Film Circuit Technology on Foil with Sub - 1V Operation Voltage. In *Technical Digest - International Electron Devices Meeting, IEDM*; IEEE, 2015; Vol. 2015-February, pp 26.1.1-26.1.4. https://doi.org/10.1109/IEDM.2014.7047110.

(31) Herlogsson, L.; Crispin, X.; Tierney, S.; Berggren, M. Polyelectrolyte-Gated Organic Complementary Circuits Operating at Low Power and Voltage. *Adv. Mater.* **2011**, *23*, 4684–4689.
(32) Shulga, A. G.; Derenskyi, V.; Salazar-Rios, J. M.; Dirin, D. N.; Fritsch, M.; Kovalenko, M. V.; Scherf, U.; Loi, M. A. An All-Solution-Based Hybrid CMOS-Like Quantum Dot/Carbon Nanotube Inverter. *Adv. Mater.* **2017**, *29*, 1701764.
(33) Pecunia, V.; Banger, K.; Sou, A.; Sirringhaus, H. Solution-Based Self-Aligned Hybrid Organic/Metal-Oxide Complementary Logic with Megahertz Operation. *Org. Electron.* **2015**, *21*, 177–183.