Supporting Information

Surface Dependent Performance of Ultrathin TiN Films as Electrically Conducting Li Diffusion Barrier for Li-Ion Based Devices

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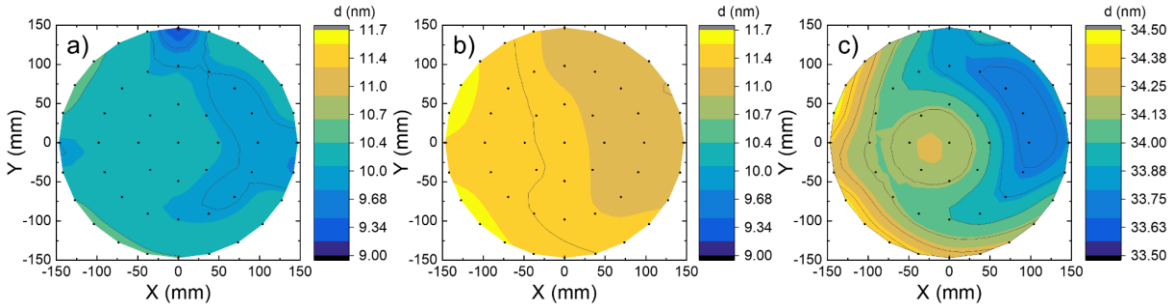

Figure S1. Full wafer maps of the film thickness measured via SE with 3 mm edge exclusion for expected a) 10 nm ALD, b) 10 nm pCVD, and c) 35 nm pCVD TiN films. The average values are 10.1 nm (ALD) and 11.3 and 34.1 nm (pCVD) and in good agreement with targeted values.

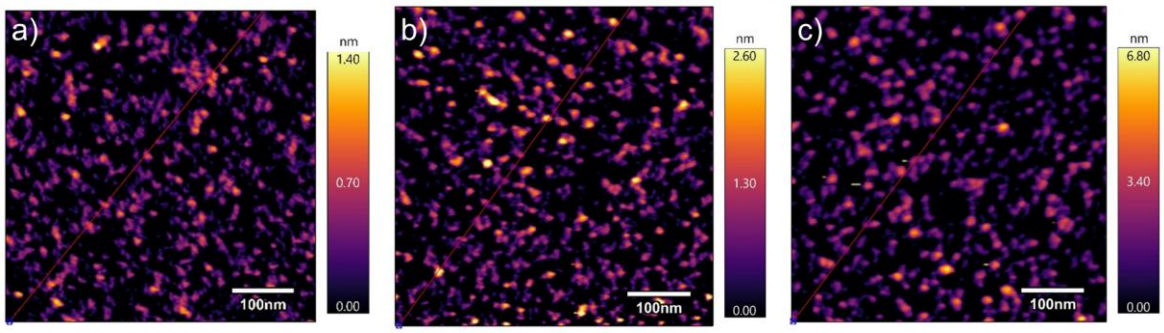

Figure S2. AFM visualization of the surface topography of a) 10 nm ALD, b) 10 nm pCVD, and c) 35 nm pCVD TiN films. *10 nm ALD* reveals the lowest roughness with an rms of 0.35 nm.

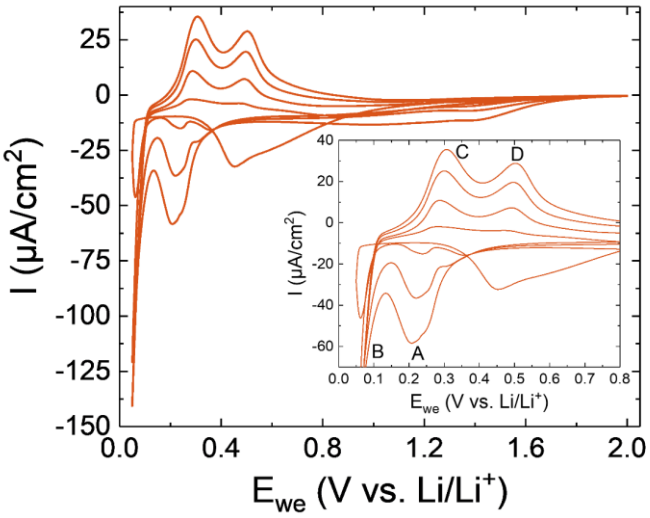

Figure S3. CV at 1 mV/s in the potential range of 0.05-2 V vs. Li/Li+ of a bare Si reference sample. Typical de-/lithiation peaks of Si are visible. In particular, cathodic peaks at 0.2 V (A) and 0.05 V (B), and anodic peaks at 0.3 V (C) and 0.5 V (D). The peak heights increase with continuous cycling, indicating enhanced insertion of Li-ions into the Si substrate.

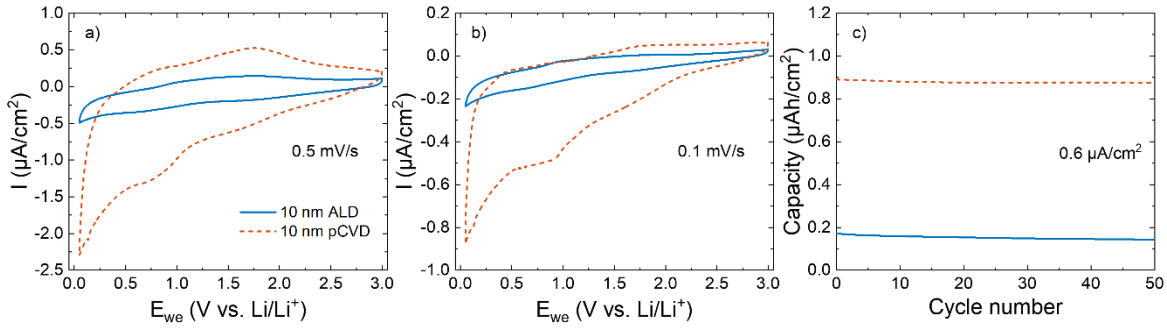

Figure S4. CV graphs at a) 0.5 mV/s and b) 0.1 mV/s and c) GCPL for 50 cycles at 0.6 µA/cm^2 in the potential range of 0.05-3 vs. Li/Li$^+$ of *10 nm ALD* and *10 nm pCVD*.

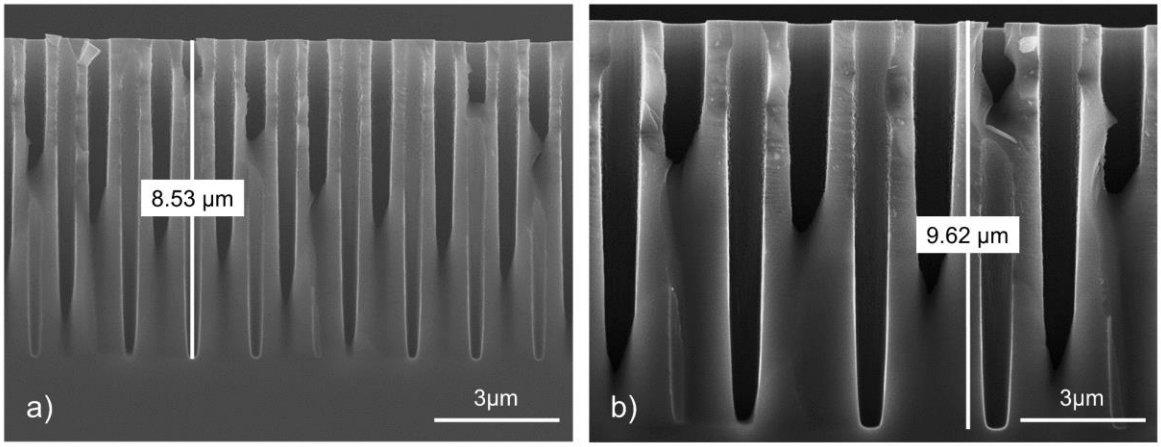

Figure S5. SEM micrograph of the 3D structured substrates with high aspect ratios of a) 20:1 and b) 10:1 for step coverage tests. The extracted values of the hole diameter are 0.45 µm and 0.98 µm and the depths values are 8.53 and 9.62 µm, respectively. This is in good agreement with the aimed aspect ratios.

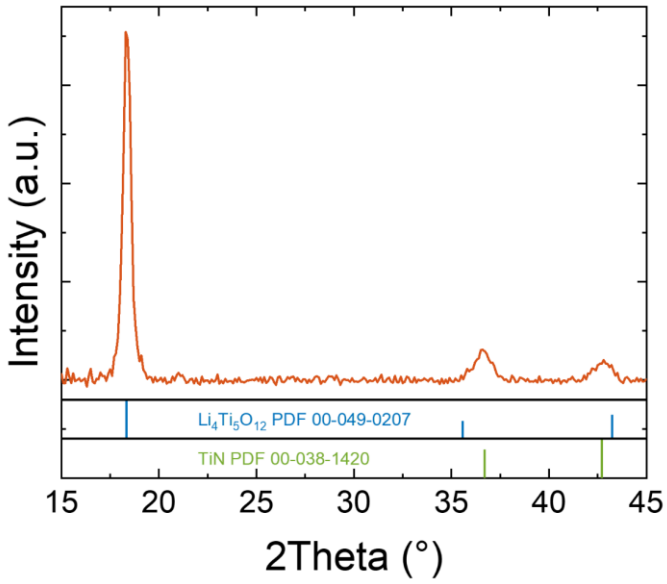

Figure S6. GI-XRD diffractogram of a layer stack compromising a $Li_4Ti_5O_{12}$ layer and a 10 nm ALD TiN film on a Si substrate after a heat treatment at 700 °C for 30 s. The peaks match with their references and no difference compared to single layers is noticed.

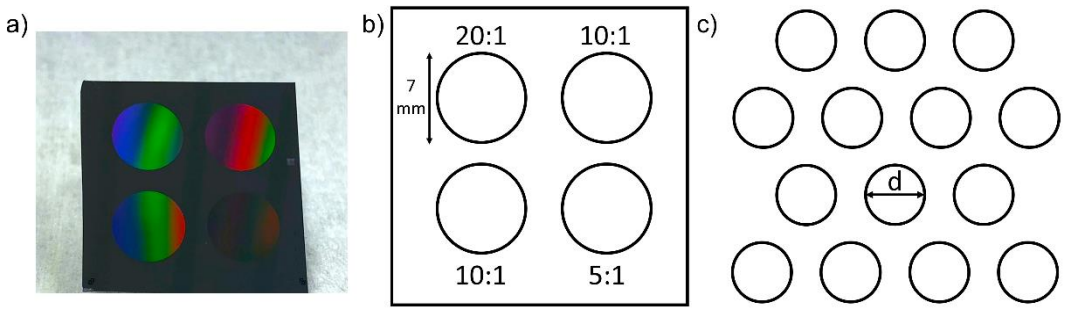

Figure S7. a) Photograph of the fully processed 3D test chip manufactured by electron beam lithography and reactive ion etching. b) Schematic of the test design with various circular areas with 7 mm diameter comprising hexagonal arrays of holes with aspect ratios of either 5:1, 10:1, or 20:1. c) Schematic of the hexagonal arrays with hole diameters d of 0.5, 1, or 2 µm and a depth of 10 µm.