Supporting Information for

Surface States Modulated High-performance InAs Nanowire Phototransistor

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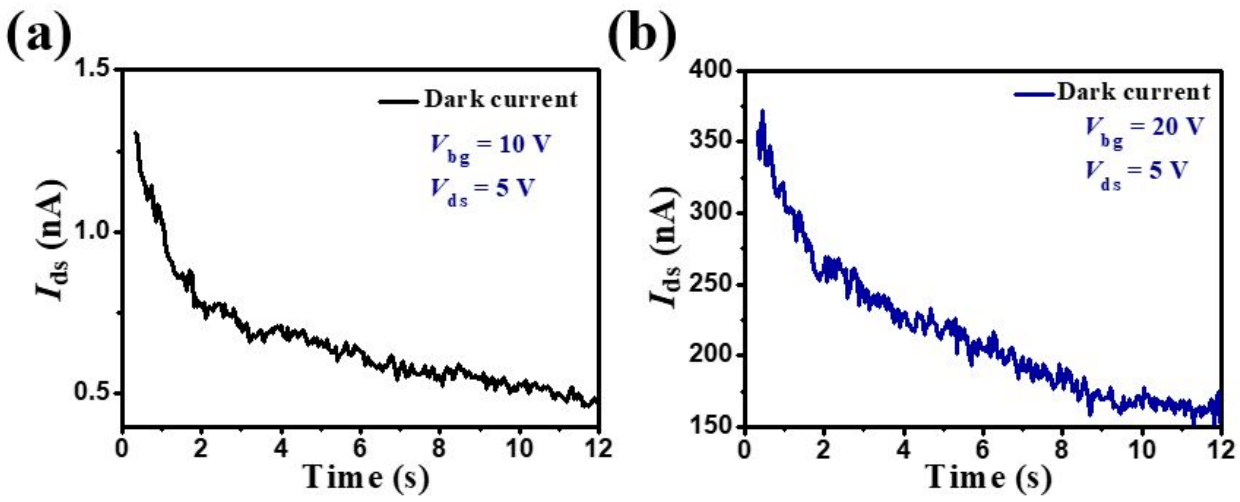

Figure S1. Linear I_{ds}- time curves of InAs NW FET in dark and under (a) V_{bg} = 10 V and (b) V_{bg} = 20 V, respectively (Temperature, 77 K). When the V_{bg} = 10 V, the current dropped from 1.3 nA to 0.48 nA in 12 seconds, resulting in a total reduction of 0.82 nA. When the V_{bg} changed from 10 V to 20 V, the current dropped from 357.8 nA to 155.2 nA in 12 seconds, resulting in a total reduction of 202.6 nA. This means that more electrons are trapped in the surface charge trapping state at larger gate voltages.

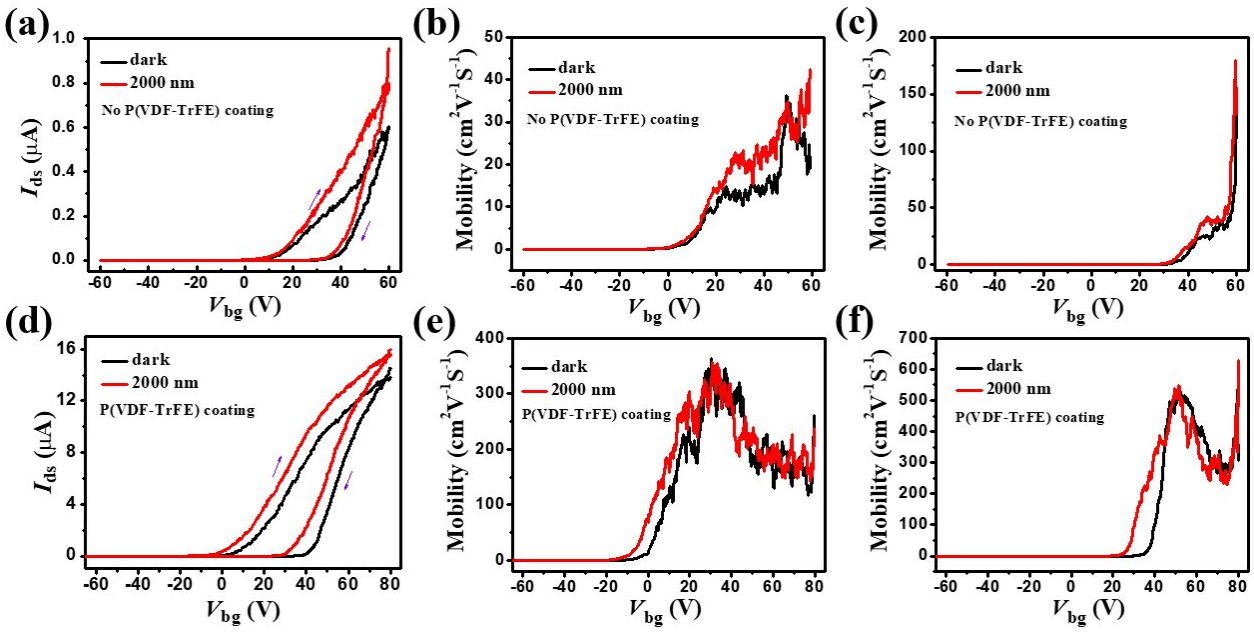

Figure S2. (a) I_{ds}-V_{bg} transfer curves of InAs NW FET under dark and illuminated conditions without P(VDF-TrFE) coating. Gate voltage-dependent carrier mobility characterization calculated from the up sweep (b) and down sweep (c) of transfer characteristic curve in (a). (d) Linear I_{ds}-V_{bg} transfer curves of InAs NW FET under dark and illuminated conditions with P(VDF-TrFE) coating. Gate voltage-dependent carrier mobility characterization calculated from the up sweep (e) and down sweep (f) of transfer characteristic curve in (c).

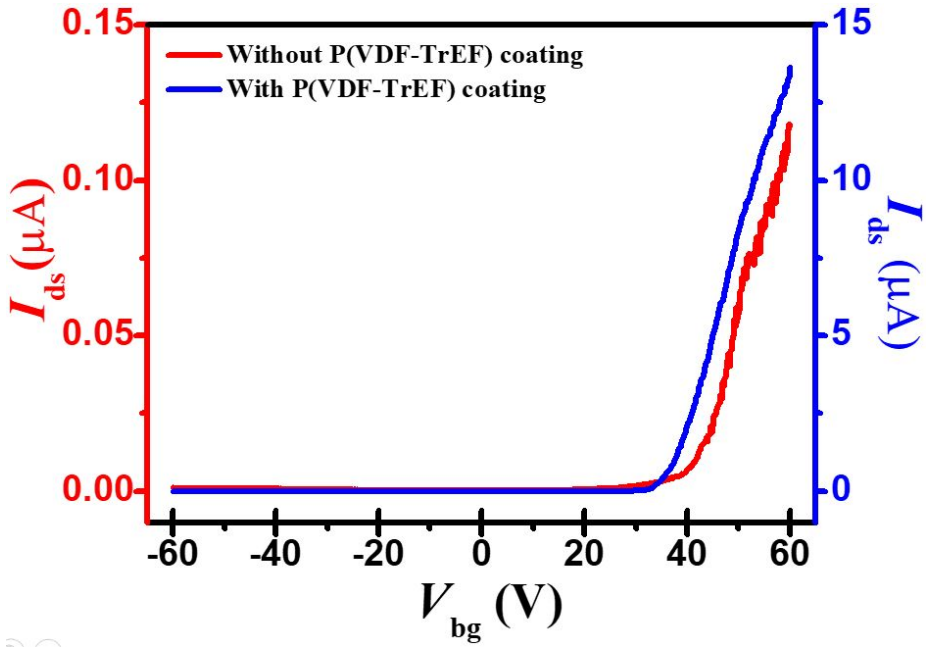

Figure S3. I_{ds}-V_{bg} transfer curves of InAs NW FET with and without P(VDF-TrFE) coating in dark at V_{ds} = 1 V (Temperature, 77 K). The on-state current increases from 0.12 μA before passivation to 13.4 μA afterward. The threshold voltage is shifted negative after deposition of 100 nm P(VDF-TrFE), indicating an increase in the mobile carrier density after deposition of 100 nm P(VDF-TrFE).[1]

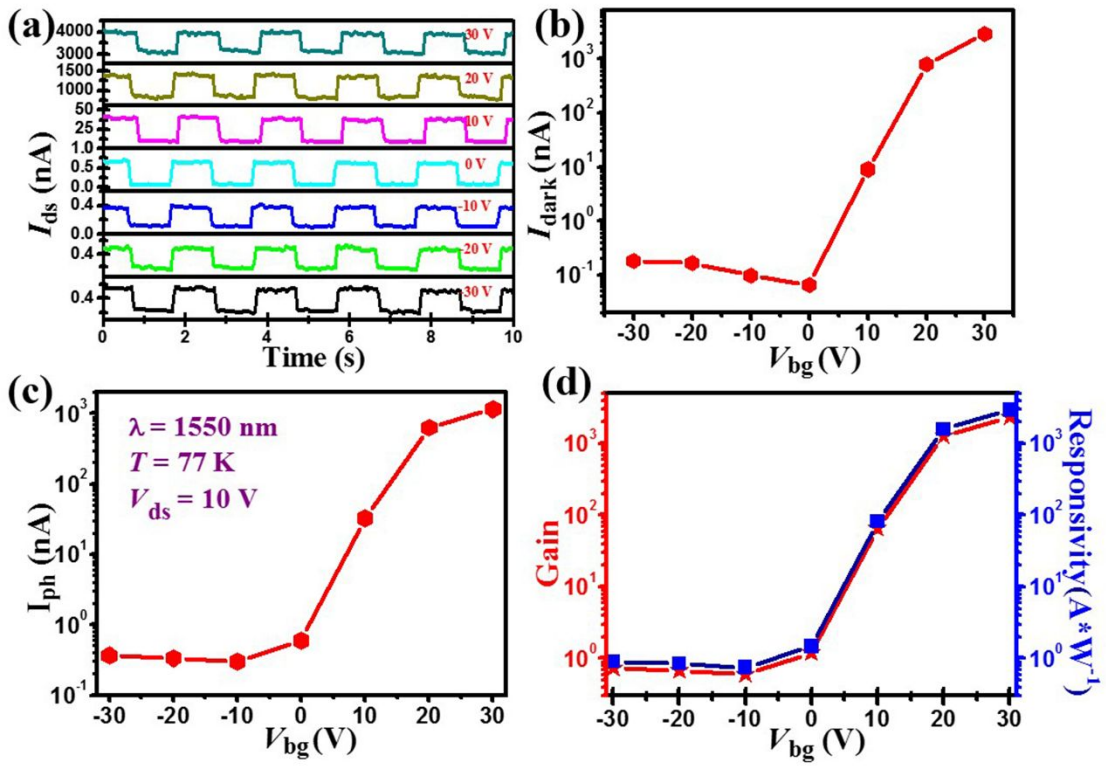

Figure S4. Photoresponse measurement of the InAs NW phototransistor after deposition of 100 nm P(VDF-TrFE) under 1550 nm, 1mW/mm^2 light illumination. (a) The family of photoelectrical response properties of the InAs NW for various back-gate voltage at V_{ds} = 10V and T = 77 K. (b) I_{dark} versus temperature curves of InAs NW FET. (c) The net photocurrent I_{ph} versus V_{bg} characteristics for before and after deposition of 100 nm P(VDF-TrFE). (d) Logarithmic Gain-V_{bg} characteristics and Responsivity-V_{bg} characteristics respectively. Figure S4(b-c) shows the dark current/net photocurrent back gate voltage relation extracted from Figure S4(a), respectively. The variation curve in Figure S4(b) is consistent with the transfer characteristics of the device. The tendency of the device's photoresponse changed with gate voltage is the same as the previous phenomenon under 2000 nm illumination. Furthermore, a high G of 2300 was achieved for the 1550 nm wavelength at a back gate of 30 V with the corresponding R of as much as 2900 A/W,

as shown in Figure S4 (d).

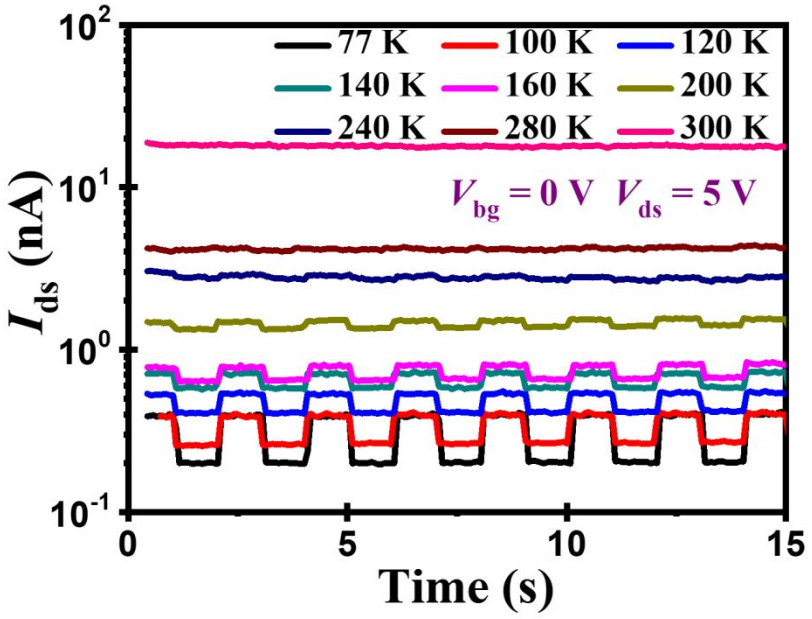

Figure S5. Family of time-resolved current rise and decay curves obtained by the application and removal of 2000 nm light illumination for the various temperature at V_{ds} = 5 V, V_{bg} = 0 V, without P(VDF-TrFE) coating.

Experimental Section

Mobility: The field-effect mobility μ can be estimated from the following equation:

$$\mu = g_m L^2/(V_{ds} C_i),$$

where g_m is the transconductance ($g_m = dI_{ds}/dV_{bg}$), L is the channel width of the device (4.5 μm). Using the 'metallic cylinder on an infinite metal plate model', the gate capacitance C_i can be obtained as described by the equation below[2-3]:

$$C_i = 2\pi\varepsilon_0\varepsilon_r L/\cosh^{-1}(1 + h/r),$$

where h is the thickness of the dielectric SiO_2 layer (300 nm), r is the averaged NW radius (~40 nm), ε_0 is the vacuum dielectric constant (8.85×10^{-12} F m^{-1}), and ε_r is the relative dielectric constant of SiO_2 ($\varepsilon_r = 2.25$).

Gain and Responsivity: The photoconduction gain (G) and responsivity (R) are two key parameters to evaluate the sensitivity of nanoscale photodetectors.[4-5] G is defined as the ratio between the number of charges collected by the electrodes per unit time and the number of photons absorbed by the NW per unit time ($G = N_e/N_{ph}$). The photoconductive gain can be expressed as:

$$G = (I_{ph}/e)/(PA/hv),$$

In addition, R of a photodetector is defined as:

$$R = I_{ph} / (PA),$$

where I_{ph} is the photocurrent, P is the incident power density, and A is the effective irradiated area on the NW, hv is the energy of an incident photon, and e is the electron charge. Note that the cross-sectional area of the NW, $A = L \times d$ is an estimation of the effective irradiated area (L is the channel length, d is the NW diameter).

Growth information: Epitaxial InAs nanowires were grown on GaAs $(111)_B$ substrates using Au as catalysts in a Riber 32 MBE system. After a GaAs $(111)_B$ substrate was degassed and deoxidized to remove any contaminants in the growth chamber, GaAs buffer layer was grown on

the substrate to ensure atomically flat surface for the nanowire growth. Subsequently, the substrate was transferred to the preparation chamber, where an Au thin film was deposited directly on the top of the GaAs buffer layer. The Au-coated substrate was then transferred back to the growth chamber and annealed at 550 °C for 5 min under As ambient (As source was switched on throughout the nanowire growth) in which the Au thin film aggregates into nanoparticles. After annealing, the substrate temperature was dropped to 230 °C, where In and Ga vapor sources were introduced to induce the nanowire growth with the respective beam equivalent pressures of $\sim 2.5 \times 10^{-7}$ and As vapor pressure of $\sim 4.4 \times 10^{-6}$ Torr to obtain a V/III (As/In) ratio of ~18.

Fabrication and Characterization: Field effect transistors (FETs) of individual InAs nanowires were transferred mechanically to pre-cleaned p^+-Si/SiO_2 (300 nm) substrates. Then, the Ti/Au (10/60 nm) source/drain (*S*/*D*) electrodes were fabricated by electron beam lithography (JEOL 6510, equipped with a nanometer pattern generation system) and electron beam evaporation. Before metallization, each nanowire was immersed in a 2% HF solution for 10 s to remove any oxides in order to ensure the Ohmic contact between the metal electrodes and nanowires. The optoelectronic properties of the prototype nanowire devices were measured using a Lake Shore TTPX probe station and a KEITHLEY 4200-SCS semiconductor parameter analyzer.

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