Supporting information

An experimental investigation of Pulsed Laser Deposition of ferroelectric Gd:HfO_2 in a CMOS BEOL compatible process

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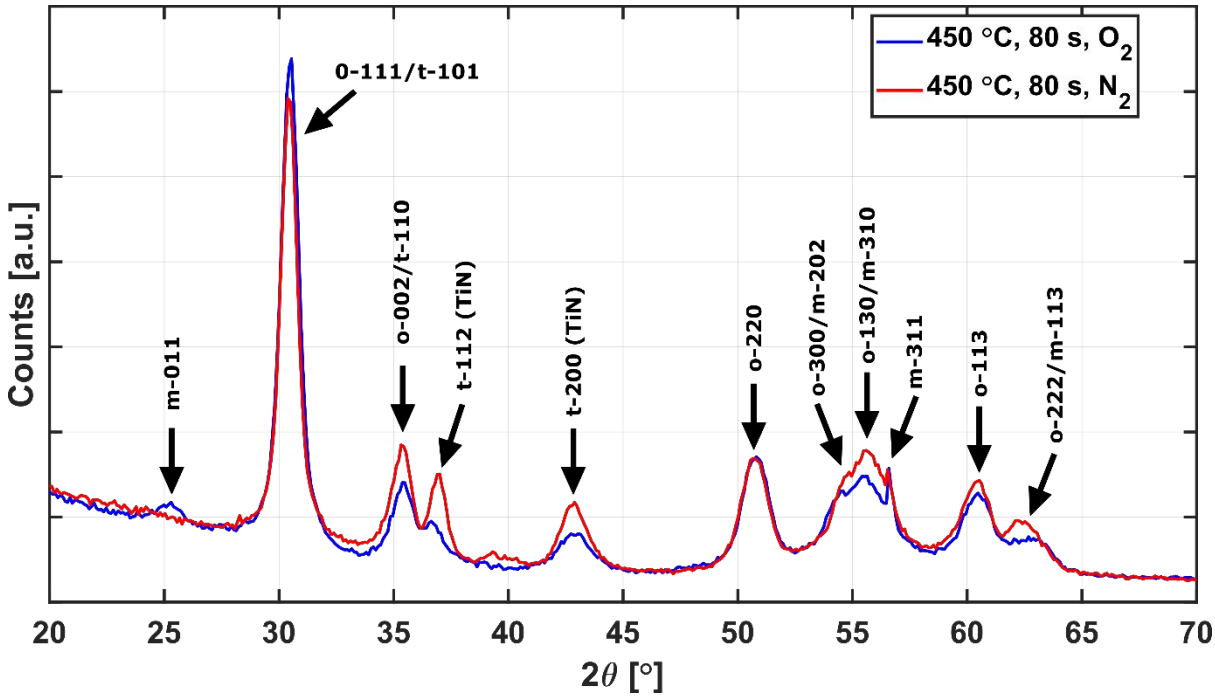

Fig. S1 – GIXRD spectra comparing two TiN/Gd:HfO_2/TiN/Si structures exposed to the same thermal budget of 450 °C for 80 s, one in O_2 and the other in N_2 environment.

In Fig. S1 GIXRD spectra are presented with 2θ angles ranging from 20° to 70°. Over this wider scan range, more peaks attributable to orthorhombic (o-HfO_2), monoclinic (m-HfO_2) and tetragonal (t-HfO_2) hafnium oxide phases can be detected. In addition, tetragonal TiN is detected (t-TiN). The main differences between the two annealing environments appear to be a small peak at 2θ = 25.4° for the O_2 annealed sample that could be attributable to the monoclinic phase, and the fact that in general there is a higher crystallization in the case of N_2 annealing for the same thermal budget. Notice that for angles 2θ > 53° it is very difficult to unequivocally identify the peaks, since higher order planes give diffraction patterns very close to one another within one phase and even among different phases. The reference patterns used for the identification are ICDD 04-003-6960 (o-HfO_2), 00-034-0104 (m-HfO_2), 04-011-8820 (t-HfO_2) and 04-018-2321 (t-TiN).

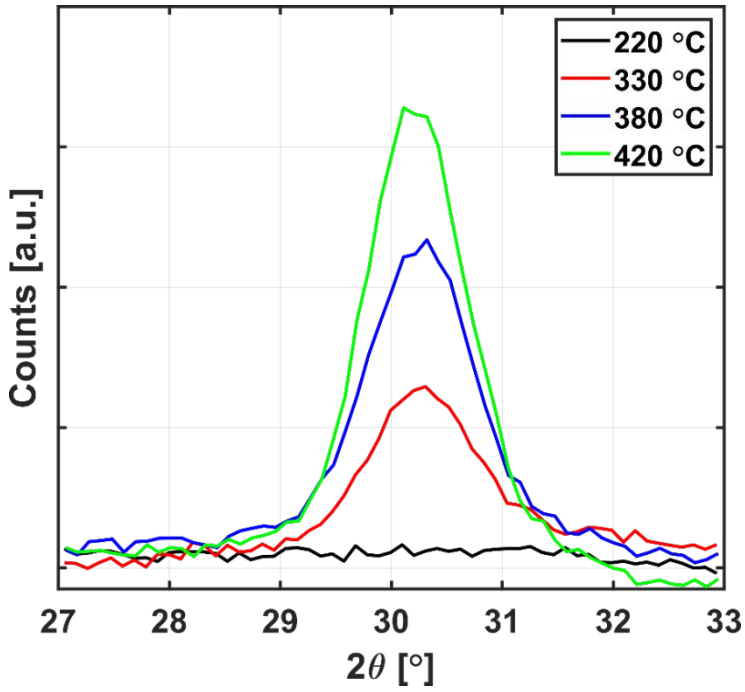

Fig. S2 – GIXRD plot of as-deposited samples for different deposition temperatures. All other deposition conditions were identical.

In Fig. S2 GIXRD spectra are presented to compare the evolution of the peak ~ 30.5° with increasing PLD deposition temperature. This data was measured on as-deposited films with no subsequent anneal step. It is clear that the deposition at 220 °C resulted in no measurable crystallization, meaning that a higher thermal budget was necessary in the subsequent annealing in order to obtain the desired crystalline phase. This is not in line with the purpose of this investigation which focused on demonstrating a BEOL CMOS compatible thermal budget. On the other hand, depositions at higher temperatures (380 °C and 420 °C) resulted in higher film crystallization but no P-E loops were observed for the as-deposited samples and, after annealing, the MIM characteristics were dominated by leakage. Therefore the deposition temperature of 330 °C was chosen in our work because it facilitated a lower temperature post-anneal step to form the ferroelectric phase and the resulting leakage current density was also within a reasonable range.

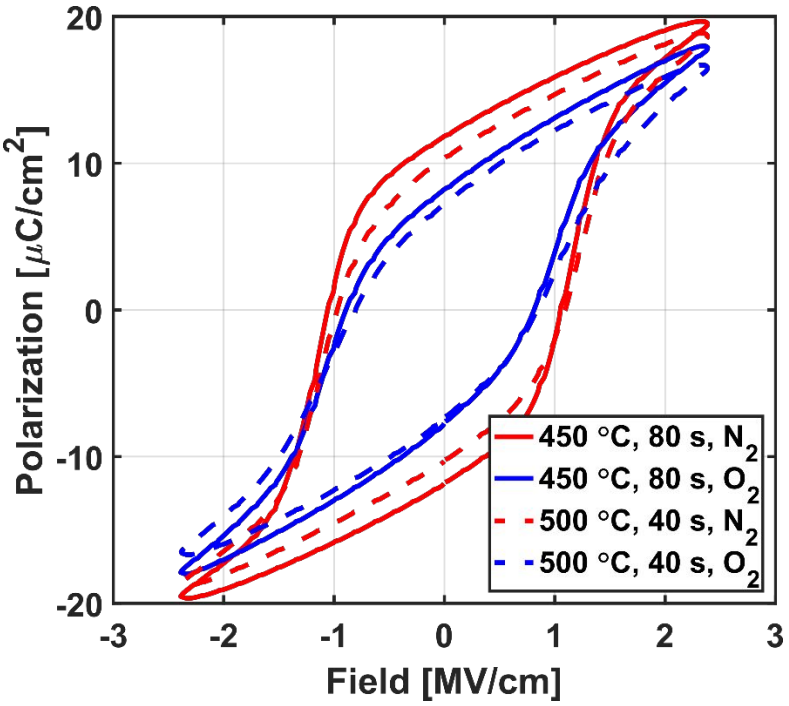

Fig. S3 – P-E loops of Gd:HfO_2 thin films showing a comparison between 450 °C and 500 °C annealing, both in O_2 and in N_2.

In Fig. S3 it is observed that for annealing in both N_2 and O_2 ambient an increase in temperature up to 500 °C (dashed lines) leads to a small reduction of P_r. Therefore the 450 °C annealing step (full lines) is the optimum among the conditions investigated in order to maintain a CMOS-compatible temperature and to obtain the optimal P_r for this particular material.

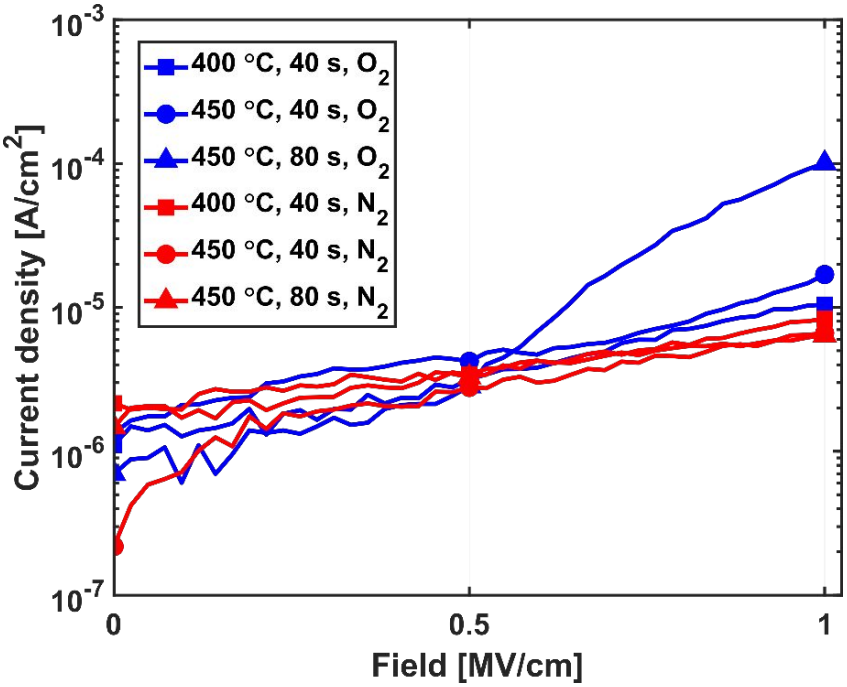

Fig. S4 – Leakage current density versus electric field (up to 1 MV/cm) for various annealing annealing conditions.

Fig. S4 plots the measured leakage at 1 MV/cm for all the samples discussed in the main manuscript. The leakage was evaluated after the same wake-up procedure adopted for P-E and ε_r-E measurements of Fig. 3, i.e. 1000 cycles at 1 kHz at 2.6 MV/cm. When comparing to other studies on ferroelectric hafnia films it is noted that these leakage current densities appear reasonable and lie within the range commonly reported in literature (see references in the main manuscript). A similar level of leakage is observed for all samples, except for the sample annealed at 450 °C for 80 s in O_2. While higher leakage is observed for this sample it still remains within the range frequently observed for ferroelectric hafnia. Further it is noted that leakage was not an issue for measuring reliable P_r characteristics on the sample set reported in the main manuscript.