Supporting Information

Forming-Less Compliance-Free Multi-State Memristors as Synaptic Connections for Brain-Inspired Computing

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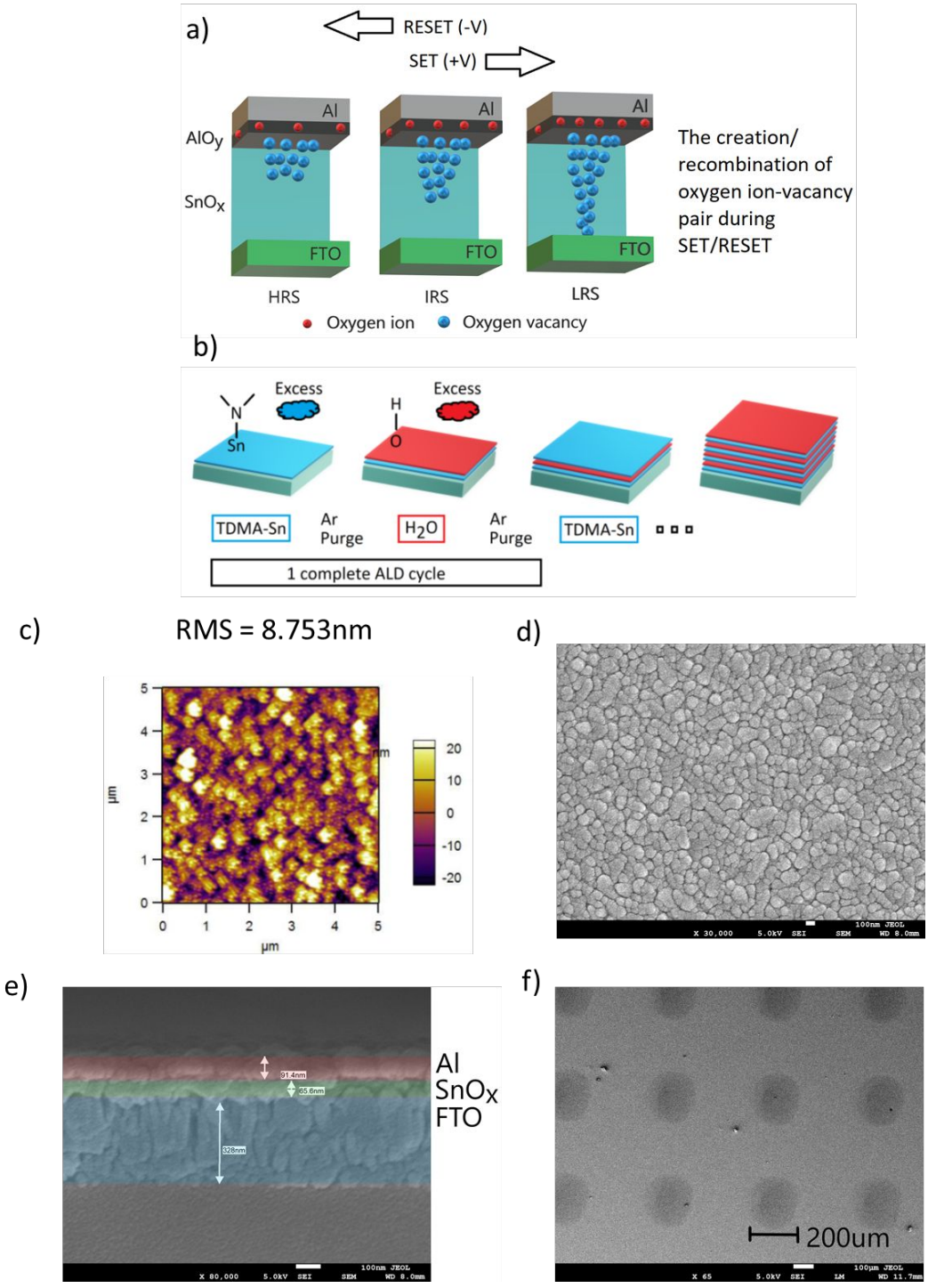

Figure S1. Memristor device structure and fabrication. (a) The device structure and schematics of switching mechanism involving a possible filamentary conduction during SET operation and the recombination of ion-vacancy during RESET operation. (b) Self-limiting half-reactions involved in the conformal and uniform ultrathin SnO_x thin film atomic layer deposition (ALD). (c) Atomic force microscopy (AFM) height retrace image of the deposited SnO_x thin film on FTO substrate shows an RMS roughness of ~9nm. (d) Top-down scanning electron microscopy image of pinhole-free SnO_x thin film. (e) Cross-sectional scanning electron microscopy image of Al/SnO_x/FTO. (f) Top-down scanning electron microscopy image of Al electrode area of device.

Aluminium with a high standard reduction potential was chosen as the top electrode overlaying the active SnO_x switching matrix grown on a highly conductive FTO substrate. The presence of an oxygen getter electrode readily captures oxide ions during the SET operation of the memristor, preventing an abrupt switching transition. As a result, a self-compliance phenomenon followed by gradual switching characteristics is observed in the multi-level memristor. During the RESET operation, the recombination of the oxygen vacancies with the oxide ions close to the interface results in the reduction of filamentary length (Figure S1a).

To improve the reliability of the memristor device fabrication, atomic layer deposition (ALD) process was selected to ensure a uniform and conformal thin film. The ALD process involves self-limiting half-reactions which are the initial chemisorption of Sn precursor molecules and the subsequent oxidation of the chemisorbed Sn species (Figure S1b). Such layer-by-layer deposition ensures conformal growth along the rough FTO polycrystalline surface. FTO glass was chosen as the bottom electrode due to its chemical inertness, temperature stability and high conductivity. The AFM image indicates the conformality of the SnO_x across the FTO substrate (Figure S1c). In Figure 1e, we can observe the thicknesses of individual layers from the cross-sectional image.

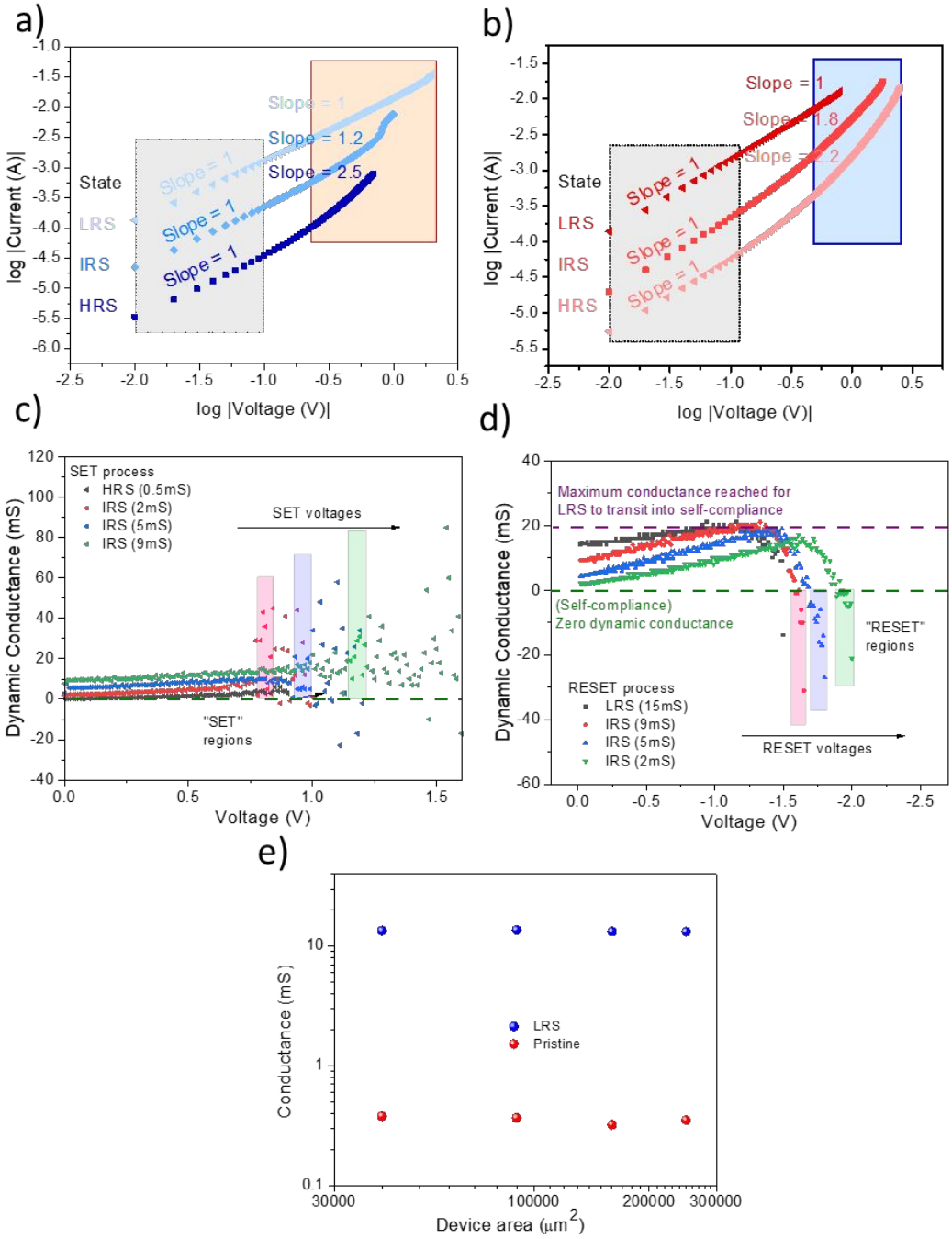

Figure S2. Electrical behaviour of high and low resistance states. Double logarithm I-V plots with calculated slopes for gradual (a) potentiation and (b) depression operation. Dynamic conductance with respect to applied voltage for (c) SET operation and (d) RESET operation, comparing transition points between various conductance states. (e) Areal independency of programming the conductance states, indicating the possible filamentary nature of conduction.

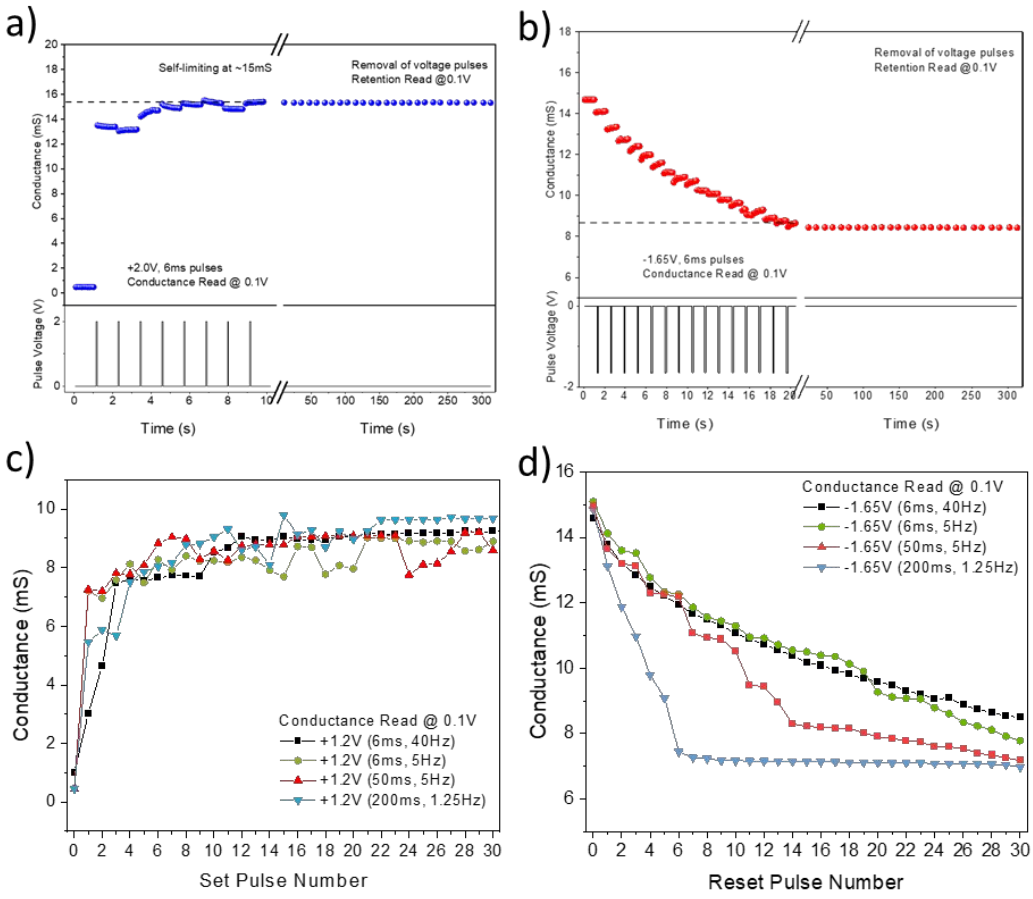

Figure S3. Pulse measurements for long-term plasticity. (a) Potentiation pulses of +2V to reach 15mS self-limit and non-volatile state. (b) Depression pulses of -1.65V to reach 9mS non-volatile state. The effect of duty cycle (Pulse width and frequency for (c) +1.2V potentiation and (d) -1.65V depression.

In addition to varying pulse voltage, we also studied the effect of stimulation duty cycle (pulse width and frequency) on the conductance updates. With increasing pulse width, the conductance update is expected to increase in magnitude and digital character. However, in Supporting Figure S3a, changing the pulse width from 6ms to 200ms does not affect the conductance update significantly for the potentiation operations, suggesting that 6ms is long pulse for potentiation. In contrast, the depression operation underwent a transition from analogue to digital regime. Increasing the pulse width resulted in less programmable states for the depression operations. Interestingly, increasing the pulse width did not significantly lower the conductance soft boundary for -1.65V depression pulses. The conductance for all duty

cycles slowly approach the conductance of approximately 7mS. However, the frequency of stimulation did not significantly affect the conductance updates in both potentiation and depression."

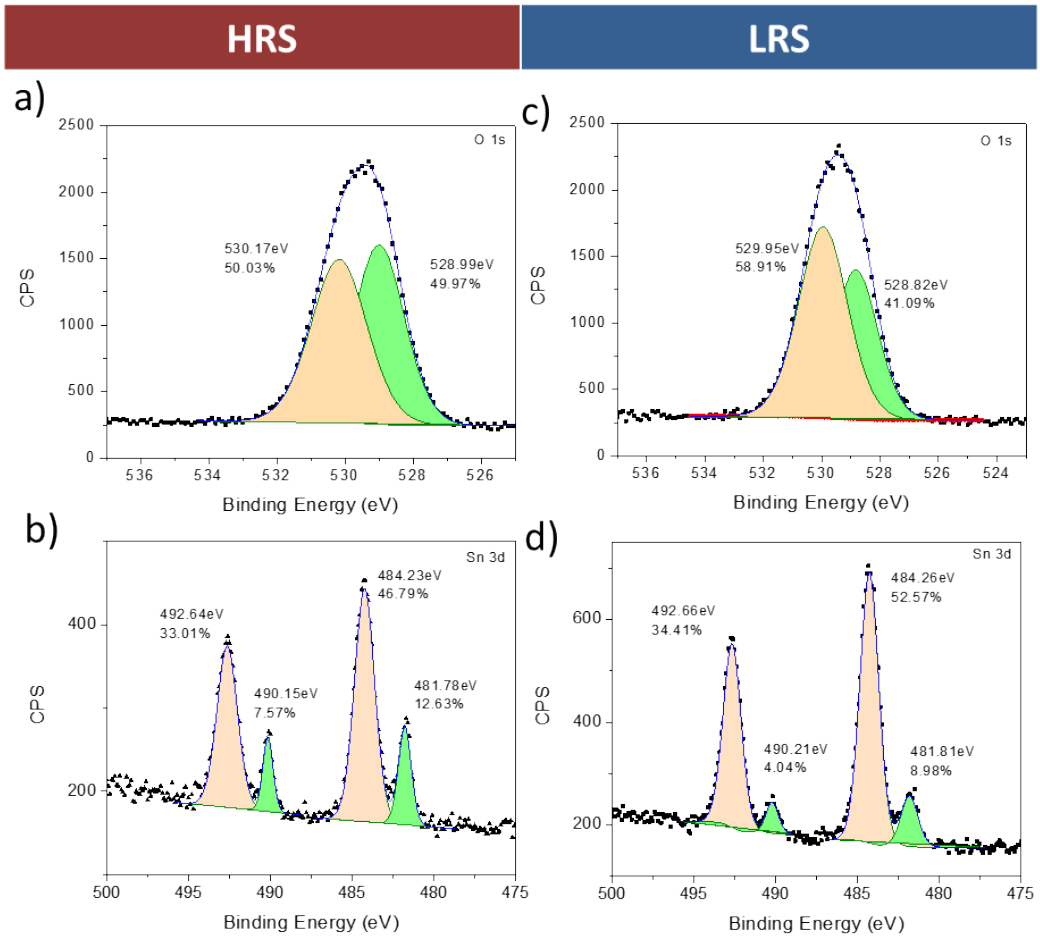

Figure S4. The XPS spectra for HRS (a, b) and LRS (c, d) detailing the O 1s and Sn 3d peaks. (a and c) O 1s peaks- the signal at ~529.0eV is attributed to the low binding energy of fully coordinated lattice oxygen of SnO_2, while the left-shifted signal at ~530.0eV is attributed to the oxygen vacancies with higher binding energy. (b and d) Sn 3d peaks- the doublets are visible with a doublet shift of ~8.4eV and an aerial ratio of 2:3. Metallic Sn is identified at ~490.2eV with the oxidised Sn^{2+}/Sn^{4+} at 2.5eV shifted to the left.

A thin layer of Al (~5nm) was evaporated specifically for the XPS measurement. The thin layer of Al electrode allows for both electrical stimulation and SnO_2 chemical signals to be picked up. Monochromatic Al Kα is used as X-ray source and helps to reduce FWHM and improve resolution of the signals. Selective area mode is used with a small aperture at the collector. This

allows an analysis area of 55µm, which is within our electrode size of 200µm. The take-off angle is selected to be ~60° for optimum signal collection. The interaction depth is expected to be 7 to 11nm based on excitation wavelength of Al Kα and the photoelectron take-off angle.

2 devices each for LRS and HRS are electrically SET/RESET prior to XPS measurements and loaded into the ultra-high vacuum (10^{-8} torr) chamber. The evolution of metallic Sn peak could arise from the reduction of SnO_2 thin film by the reactive Al electrode during the deposition process (Figures S3b and d). Such a reduction can be observed at metal/ metal-oxide interfaces where the metal is of higher reduction potential than the oxide. The reduction potential differences can be determined from the thermodynamic series used in metallurgy such as Ellingham diagram[1]. This correlation allows for further modulation of the memristive characteristics in future by adopting active electrodes with the desired oxygen-gettering ability, paving way for novel memristive devices and architectures. To investigate the composition ratio of SnO_x, we performed a chemical analysis using X-ray photoelectron spectroscopy. In this analysis, the Sn $3d_{5/2}$ peaks (deconvoluted into 2 peaks at 484.23eV and 481.78eV corresponding to Sn^{4+} and Sn^0 respectively) were chosen. By comparing the ratio of integral area under each peak, we have calculated the ratio between the 2 valence states and deduced the analysed film to be $SnO_{1.57}$ which is similar to previous reports[2] regarding thermal oxidation of TDMASn with temperature lower than 150ºC and using water as the oxidant. These films are shown to be a mixture of SnO and SnO_2 phases.

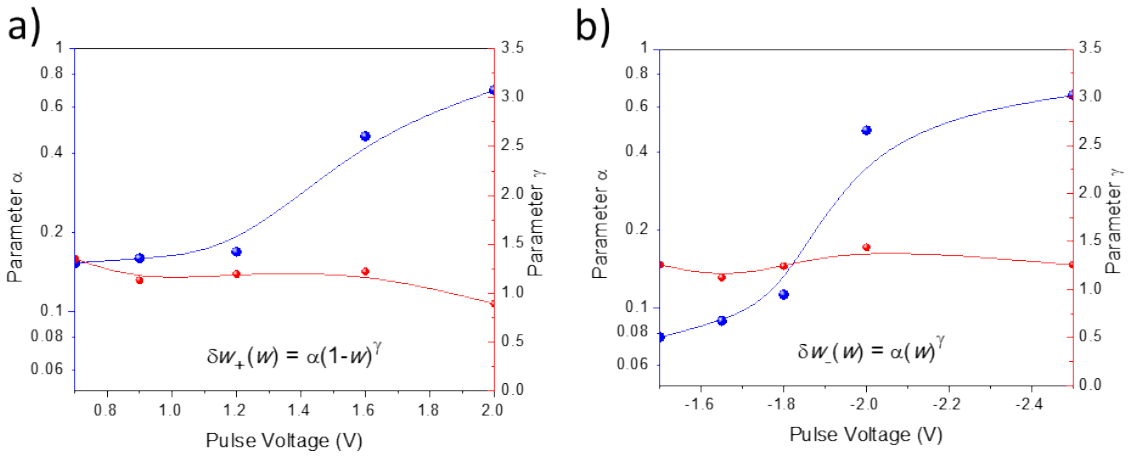

Figure S5. A multiplicative update scheme featuring weight-dependent rules is adopted to account for the state-dependent weight modulation feature in our devices. The above graphs represent the variation in the multiplicative parameter "α" and state dependency factor "γ", indicating the soft boundaries for weight updates during (a) set and (b) reset operations.

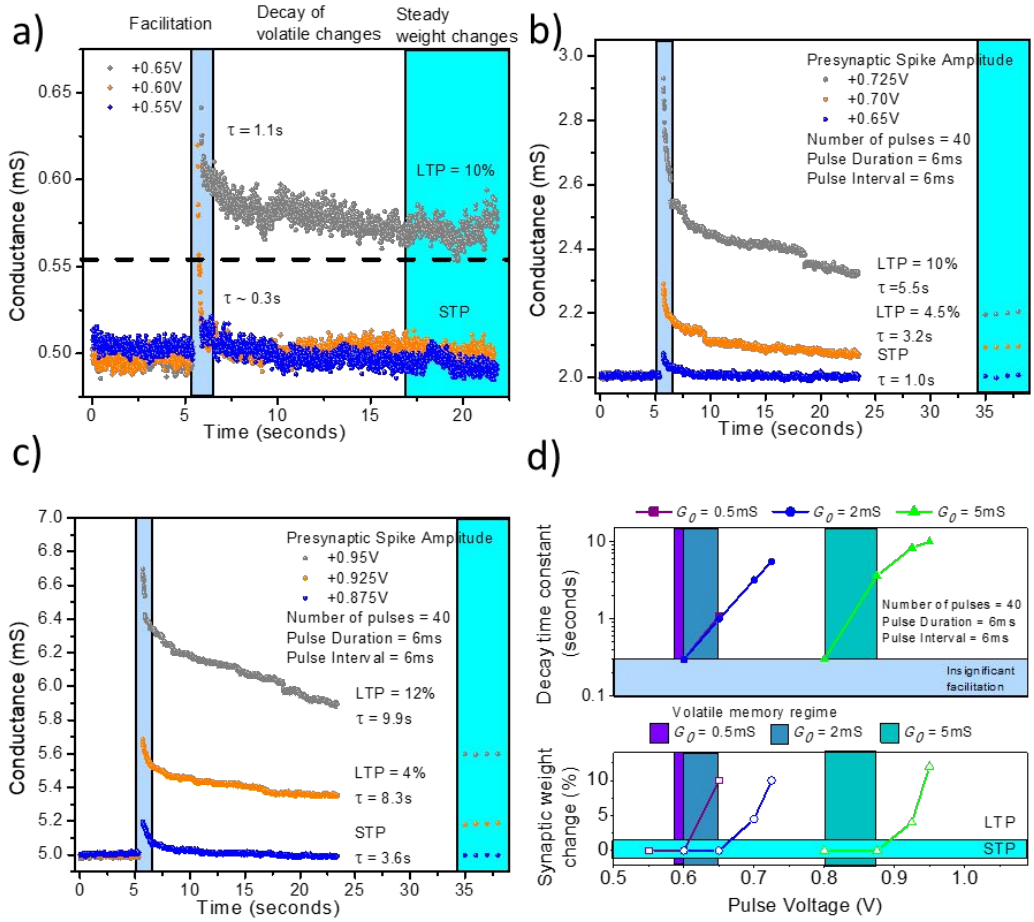

Figure S6. Volatile memory operation and its state dependency. Short-term potentiation and consolidation of the device conductance subjected to a pulse train of amplitude=0.5 to 0.875V, number=40 and pulse width= 6ms. Device is pre-programmed to an initial state of (a) 0.5mS, (b) 2mS and (c) 5mS. (d) The relation between the short-term memory characteristics and the pre-programmed conductance state 0.5mS, 2mS and 5mS respectively.

The devices depict a volatile or short-term memory when stimulated with small voltages. Input voltages below the LTP threshold (close to the soft boundaries of the memristor) results in temporary strengthening of EPSCs as shown in Figure S6a. Modelling the transient currents, the decay constant 'τ' is extracted and plotted against the pulse voltages. At higher voltages (above the LTP threshold), the synaptic weight changes depict a transition from short (volatile) to long-term (non-volatile) memory. This phenomenon known as consolidation[3,4] is illustrated in Figure S6. Similar to the state-dependent LTP measurements[5], the short-term memory characteristics also depict a dependency on the initial state of the device. To study this effect, the device is pre-programmed or initialized to 0.5mS, 2mS and 5mS states and the current transients are recorded as shown in Figures S6a-c. As evident from these figures, the volatile

memory regime is observed to lie very close to the LTP threshold at all three measured states. Figure S5d summarizes the results of Figures S6a-c, clearly depicting the variation of the decay constant 'τ' and the threshold for consolidation with input voltage and initial conductance state.

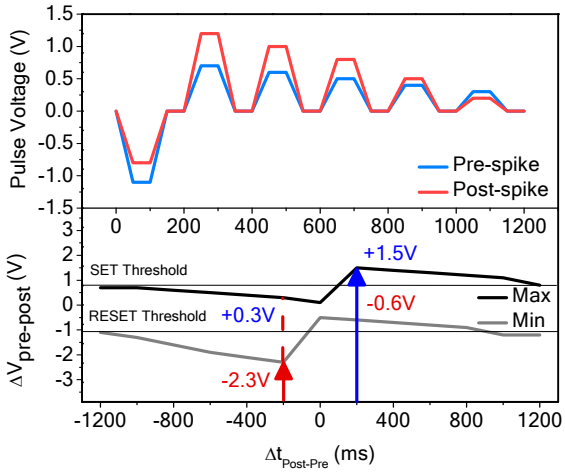

Figure S7. Applied STDP input pulse waveforms at the pre- and post-synaptic terminals and the effective potential difference with respect to the time delay between the pulses. A read pulse of + 0.1 V is applied at the post-synaptic terminal to read the conductance states before and after the STDP write operations.

The applied STDP waveforms are optimized in congruence with the switching characteristics of the device. The SET/ RESET thresholds are established to be approximately +0.65V/ -1.10V at low/high conductance states from the long-term plasticity measurements. These thresholds are indicated in Figure S7 in the plot illustrating the effective voltage developed across the device (ΔV) against time interval between the pre- and post-synaptic spikes (Δt). The asymmetry between the SET and RESET voltages are also taken into account to accentuate the LTD side of the asymmetric Hebbian characteristics. For $\Delta t > 0$, where LTP is expected, the minimum ΔV is below the RESET threshold to avoid unintended LTD effects. For example, at $\Delta t = +200$ms, V_{pre}-$V_{post} = (+0.70) - (-0.80) = 1.5$V (LTP), while $V_{min} = -0.6$V which is below the reset threshold, hence not affecting LTP. For $\Delta t < 0$, where LTD is expected, the maximum ΔV is below the SET threshold to avoid unintended LTP effects. For example, at $\Delta t = -200$ms

V_{pre}-V_{post} = (-1.10) – (+1.20) = -2.3 V (LTD), while V_{max} = +0.3V, which is below the set threshold, hence not affecting LTD.

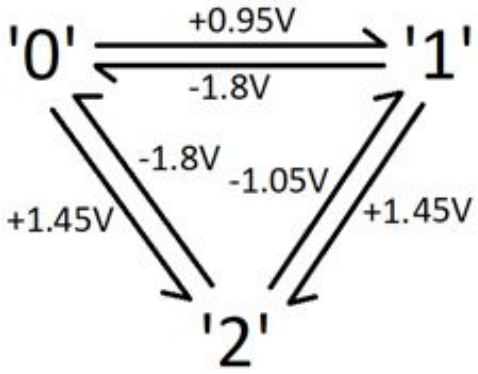

Figure S8. Modulation paths for transition between 3 states '0', '1' and '2'.

Table S1. Comparison table for state-of-the-art multi-state memristors.

Performance parameters	$Pt/TiO_2/Al_2O_3/Pt$ Sci. Rep. 2017, 7(1), 17532.	$Pt/KNbO_3/TiN$ ACS Appl. Mater. Interfaces 2018, 10, 25673−25682	RIR-Ir/Ta/TaO_x/AlO_y/W ACS Appl. Mater. Interfaces 2018, 10, 29757-29765.	$TiN/ZrO_2/ZrO_{2-x}/ZrO_2/TiN$ Nanoscale Research Letters 2017, 12, 384.	$Ti/AlHfO_x/TiN$ Nanotechnology 2019, 30, 445205.	Pt/FeOx/Pt Nanotechnology 2018, 29, 495201.	$Pt/a\text{-}CO_x/ta\text{-}C/Ag$ Nanoscale 2018, 10, 20272.	$Al/SnO_x/FTO$ [this work]
Size	Sub-µm 40nm TiO_2 4nm Al_2O_3	280µm diameter 35nm $KNbO_3$	1-30µm diameter 25nm TaO_x 1nm AlO_y	100µm diameter 50nm SiN_x 1.5nm AlO_y	20µm crossbar $HfO_x/AlO_x/HfO_x$ 2.5nm/1nm/2.5nm	1 – 5µm crossbar 10nm FeO_x	40µm diameter 40nm $a\text{-}CO_x$	200µm diameter 65nm SnO_x
Dynamic range	> 3	> 10	> 100	400	< 10	> 10	> 2 in DC I-V cycles	> 10 in DC I-V ~ 30 with multiple pulses
Endurance cycles	No DC / AC data shown	DC - 200 cycles (stability not shown)	AC - 10^{12} Cycles Only for bi-stable mode	DC – 100 Cycles Only for bi-stable mode	No endurance data shown	AC – 100 pulses Only for bi-stable mode	DC – 100 cycles Only for bi-stable mode	DC – 100 Cycles >200 ternary transitions
Multi-state retention	8 hours for all states	> 10^4 s for all 5 states	> 10^4 s for all 4 states	Not available	85ºC, 10^3 s for all 6 states	Not available	Not available	>5000s for 6 distinct programmable states
Number of States	92 distinct programmable states with low variance and window > 3	5 distinct programmable states, Programmed via different RESET voltage	4 distinct programmable states	No distinct programmable states	6 distinct states, in a window of ~2	No distinct states demonstrated	No distinct states demonstrated	**6 distinct programmable states in a window of ~ 30** **Ternary switching with all 6 permutation transitions in a window of ~5**
Forming Voltage	A series of -8V to 1µs pulses till 25 to 200 kΩ	No high voltage forming required	5V for 1nm Al_2O_3 device	> 5V	4 to 5V	-1V, no high voltage forming	>3.5V, CC=5mA	**No high voltage forming required**
Compliance current	1kΩ resistor in series	No compliance current for multi-level operation	No compliance limits required	CC=1mA for SET operations	CC=0.1mA for SET operations	CC=5mA for SET operations	No compliance limits required	**No compliance limits required**

References:

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